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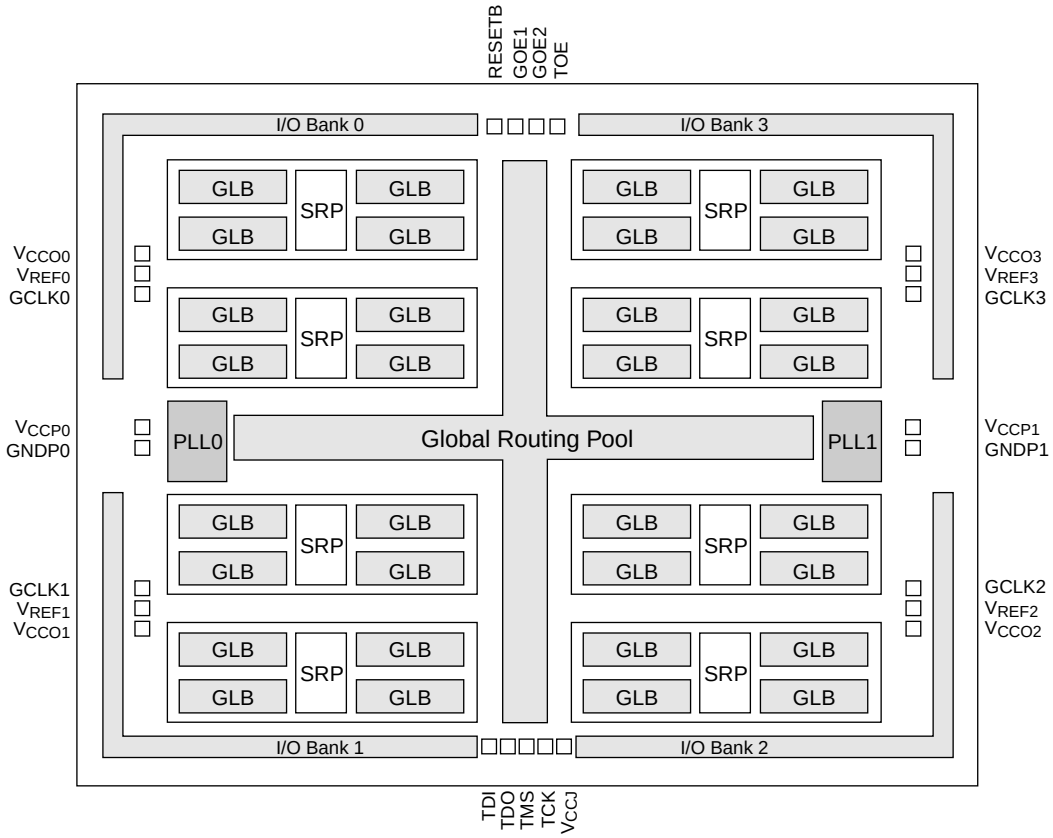
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	384
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	676-BBGA
Supplier Device Package	676-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024vg-75f676c

Figure 1. Functional Block Diagram



Overview

The ispMACH 5000VG devices consist of multiple SuperWIDE 68-input, 32-macrocell Generic Logic Blocks (GLBs) interconnected by a tiered routing system. Figure 1 shows the functional block diagram of the ispMACH 5000VG. Groups of four GLBs, referred to as segments, are interconnected via a Segment Routing Pool (SRP). Segments are interconnected via the Global Routing Pool (GRP.) Together the GLBs and the routing pools allow designers to create large designs in a single device without compromising performance.

Each GLB has 68 inputs coming from the SRP and contains 163 product terms. These product terms form groups of five product term clusters, which feed the PT sharing array or the macrocell directly. The ispMACH 5000VG allows up to 160 product terms to be connected to a single macrocell via the product term expanders and PT Sharing Array.

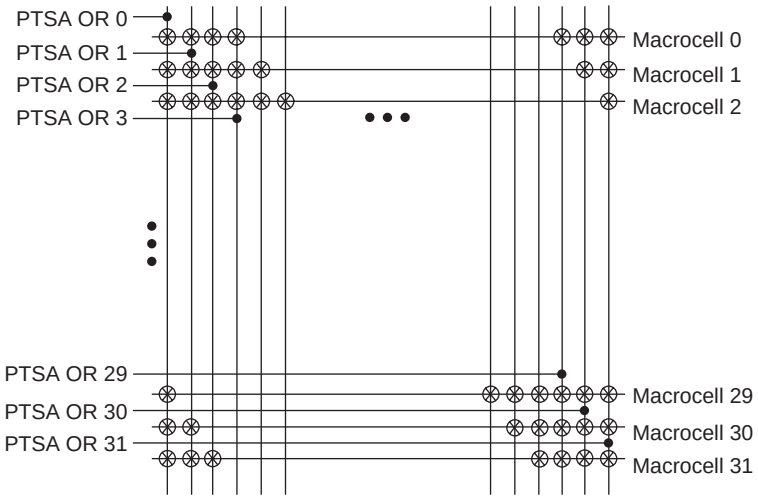
The macrocell is designed to provide flexible clocking and control functionality with the capability to select between global, product term and block-level resources. The outputs of the macrocells are fed back into the switch matrices and, if required, the sysIO cell.

All I/Os in the ispMACH 5000VG family are sysIOs, which are split into four banks. Each bank has a separate I/O power supply and reference voltage. The sysIO cells allow operation with a wide range of today's emerging interface standards. Within a bank, inputs can be set to a variety of standards, providing the reference voltage requirements of the chosen standards are compatible. Within a bank, the outputs can be set to differing standards, providing the I/O power supply voltage and the reference voltage requirements of the chosen standard are compatible. Support for this wide range of standards allows designers to achieve significantly higher board-level performance compared to the more traditional LVCMOS standards.

Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Figure 6 shows the graphical representation of the PTSA.

Figure 6. Product Term Sharing Array



Macrocell

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation.

The macrocells each have two outputs, which can be fed to the SRP, GRP and I/O cell. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 7 is a graphical representation of the ispMACH 5000VG macrocell.

Global clock pins have additional capabilities that allow for higher performance applications. Two global clock pins can be paired together to create a single global clock pin that can interface with certain differential signals.

The TOE and JTAG pins of the ispMACH 5000VG device are the only pins that do not have sysIO capabilities. These pins only support the LVTTL and LVCMOS standards.

There are three classes of I/O interface standards that are implemented in the ispMACH 5000VG devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Usage of these particular I/O interfaces requires the use of an additional VREF signal. At the system level, a termination voltage, VTT, is also required. Typically, an output will be terminated to VTT at the receiving end of the transmission line it is driving.

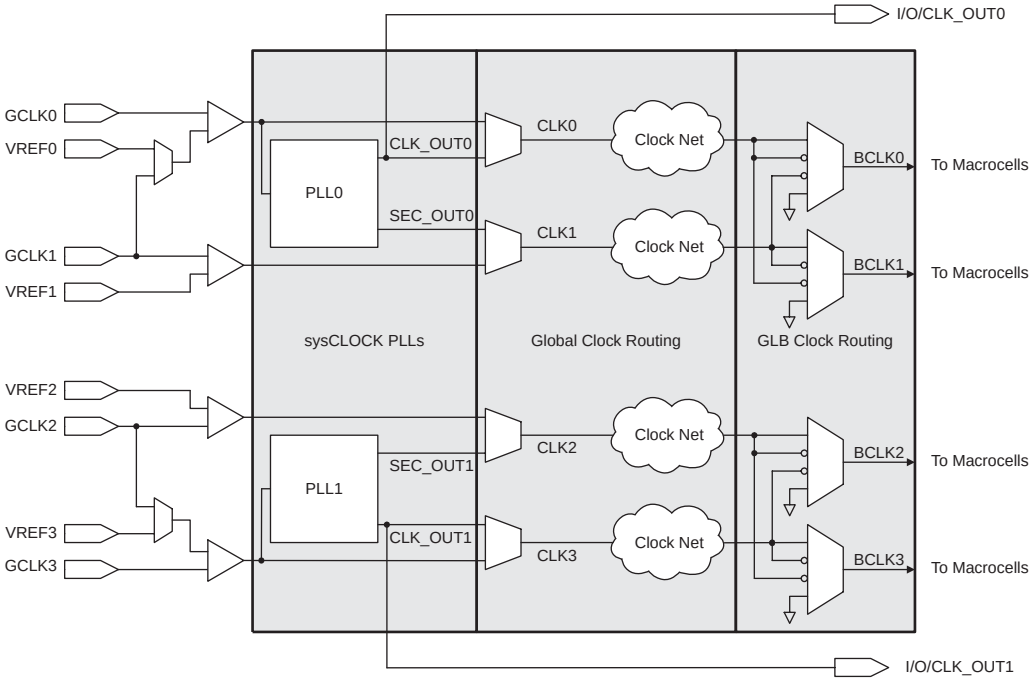
The final types of interfaces implemented are the differential standards LVDS and LVPECL. These interfaces are implemented on clock pins only. When using one of the differential standards, a pair of global clock pins (GCLK0 and GCLK1 or GCLK3 and GCLK2) is combined to create a single clock signal.

For more information on the sysIO capability, please refer to Technical Note TN1000: *ispMACH 5000VG sysIO Design and Usage Guidelines* .

GLB Clock Distribution

The ispMACH 5000VG family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the GLB clock multiplexes which generate the GLB clock signals (BCLK0-BCLK3). The GLB clock multiplexer allows a variety of true and complementary versions of the clocks to be used within the GLB. Each block clock can be the true or inverse of its associated global clock or the inverse of the adjacent global clock. Figure 9 shows the clock distribution network.

Figure 9. Clock Distribution Network



IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 5000VG devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispMACH 5000VG family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 5000VG devices provide In-System Programming (ISP™) capability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The ispMACH 5000VG devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 5000VG devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 5000VG devices during the testing of a circuit board.

Security Bit

A programmable security bit is provided on the ispMACH 5000VG devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary design from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Hot Socketing

The ispMACH 5000VG devices are well suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Density Migration

The ispMACH 5000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	+/-10	µA
I_{PU}[2]	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	-150	µA
			V_{CCO} = 2.5	-20	—	-150	µA
			V_{CCO} = 1.8	-10	—	-150	µA
I_{PD}[2]	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)		30	—	150	µA
I_{BHLS}[2]	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)		30	—	—	µA
I_{BHHS}[2]	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	—	µA
			V_{CCO} = 2.5	-20	—	—	µA
			V_{CCO} = 1.8	-10	—	—	µA
I_{BHLO}[2]	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	150	µA
I_{BHHO}[2]	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	-150	µA
I_{CC}[3, 4, 5]	Operating Power Supply Current	V_{CC} = 3.3V		—	380	—	mA
V_{BHT}	Bus Hold Trip Points			V_{IL} (MAX)	—	V_{IH} (MIN)	V
C_1	I/O Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_2	Clock Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_3	Global Input Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Only available for LVCMOS and LVTTL standards.
3. T_A = 25°C, f = 1.0MHz.
4. Device configured with 16-bit counters.
5. I_{CC} varies with specific device configuration and operating frequency.

ispMACH 5768VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.20

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 5768VG Internal Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BSR}	Block PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{SPTOE}	Segment PT OE Delay	—	2.40	—	3.60	—	7.75	—	9.10	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.40	—	2.10	—	1.75	—	2.10	ns

Notes: Timing v.1.20

1. Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details.
2. t_{PLL_DELAY} is the unit increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to 3.5ns in either direction in units of 0.5ns for each step.

ispMACH 51024VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL\_SEC\_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{H}	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS18_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 12mA Buffer	—	1.35	—	1.35	—	1.35	—	1.35	ns
LVCMOS25_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS25_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS25_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 8mA Buffer	—	0.70	—	0.70	—	0.70	—	0.70	ns
LVCMOS25_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 12mA Buffer	—	0.50	—	0.50	—	0.50	—	0.50	ns
LVCMOS25_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 16mA Buffer	—	0.25	—	0.25	—	0.25	—	0.25	ns
LVCMOS33_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS33_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS33_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 8mA Buffer	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS33_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 12mA Buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS33_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 16mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS33_20mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 20mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{BUF}, t_{EN}, t_{DIS}	Output configured as LVTTL Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.50	—	1.50	—	1.50	—	1.50	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI-X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_out	t_{BUF}, t_{EN}, t_{DIS}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_I standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
SSTL3_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_II standard	—	-0.35	—	-0.35	—	-0.35	—	-0.35	ns
SSTL2_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
HSTL_III_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF}, t_{EN}, t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.20

ispMACH 51024VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.10

Signal Descriptions

Signal Names	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the 1149.1 state machine.
TCK	Input - This pin is the Test Clock input pin, used to clock the 1149.1 state machine.
TDI	Input - This pin is the 1149.1 Test Data In pin, used to load data.
TDO	Output - This pin is the 1149.1 Test Data Out pin used to shift data out.
TOE	Input - Test Output Enable pin. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
RESETB	Dedicated Reset Input - This pin resets all registers in the devices. The global polarity (active high or low input) for this pin is selectable.
xyzz (e.g. 0A16)	Input/Output - These are the general purpose I/O used by the logic array. *x* is segment reference (numeric), *y* is GLB reference (alpha) and *z* is macrocell reference (numeric). *x*: 0-7 (1024) *x*: 0-5 (768) *y*: A-D *z*: 0-31
GND	Ground
NC	No connect
V_{CC}	Vcc - These are the power supply pins for the logic core.
GCLK0, GCLK3	Input - These pins are configured to be either dedicated CLK input or PLL input.
GCLK1, GCLK2	Input - These pins are dedicated CLK input.
CLK_OUT0, CLK_OUT1	Output - These pins are the PLL output pins.
PLL_RST0, PLL_RST1	Input - These pins are for resetting the PLL, input clock (M) divider.
VREF0, VREF1, VREF2, VREF3	Input - These are the reference supplies for the I/O banks.
PLL_FBK0, PLL_FBK1	Input - These PLL feedback inputs allow optional external PLL feedback.
V_{CCP0}, V_{CCP1}	V_{CC} - These are the V_{CC} supplies for the PLLs.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} - These are the V_{CC} supplies for each I/O bank.
GNDP0, GNDP1	GND - These are the separate ground connections for the PLLs.
V_{CCJ}	V_{CC} - This pin is for the 1149.1 test access port.

Note: For above, signal CLK_OUT0 connects to PLL0, and signal CLK_OUT1 connects to PLL1.

ispMACH 5768VG Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[2]	484-Ball fpBGA[2]
V_{CC}	F8, F9, H6, H11, J6, J11, L8, L9	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6
V_{CCO0}	C3, C7, G3	B5, D7, E2, E6, E9, F5, G4, J5
V_{CCO1}	K3, P3, P7	P5, U5, V6, V9, Y3
V_{CCO2}	K14, P10, P14	P18, U18, V14, V17, Y20
V_{CCO3}	C10, C14, G14	B18, D16, E14, E17, E21, F18, G19, J18
V_{CCP0}	H1	L7
V_{CCP1}	H16	N18
V_{CCJ}	J1	P4
V_{REF0}	E7	A9
V_{REF1}	M7	AA10
V_{REF2}	R13	AA13
V_{REF3}	A8	A15
GND PLL 0	H7	L6
GND PLL 1	J10	L16
GND	A1, C5, C12, E3, E14, G7, G8, G9, G10, H8, H9, H10, J7, J8, J9, K7, K8, K9, K10, M3, M14, P5, P12	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22
NC[3]	—	AA1

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 51024 Power Supply and NC Connections[1]

Signal	484-Ball fpBGA[2]	676-Ball fpBGA[2]
V_{CC}	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6	B29, D6, D10, D12, D19, D21, D25, F4, F27, K4, K27, M4, M27, W4, W27, AA4, AA27, AE4, AE27, AG6, AG10, AG12, AG19, AG21,AG25, AJ2
V_{CCO0}	B5, D7, E2, E6, E9, F5, G4, J5	E5, E7, E9, E11, F10, G5, J5, K6, L5
V_{CCO1}	P5, U5, V6, V9, Y3	Y5, AA6, AB5, AD5, AE10, AF5, AF7, AF9, AF11
V_{CCO2}	P18, U18, V14, V17, Y20	Y26, AA25, AB26, AD26, AE21, AF20, AF22, AF24, AF26
V_{CCO3}	B18, D16, E14, E17, E21, F18, G19, J18	E20, E22, E24, E26, F21, G26, J26, K25, L26
V_{CCP0}	L7	P5
V_{CCP1}	N18	N26
V_{CCJ}	P4	U6
V_{REF0}	A9	C11
V_{REF1}	AA10	AK10
V_{REF2}	AA13	AJ21
V_{REF3}	A15	E19
GND PLL 0	L6	R6
GND PLL 1	L16	P25
GND	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22	A1, A30, B2,C3, C28, D8, D23, F7, F9, F11, F12, F19, F20, F22, F24, G6, G25, H4, H27, J6, J25, L6, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L25, M6, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M25, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14,U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W25, Y6, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y25, AB6, AB25, AC4, AC27, AD6, AD25, AE7, AE9, AE11, AE12, AE19, AE20, AE22, AE24, AG8, AG23, AH3, AH28, AK1, AK30
NC[3]	AA1	A14, A15, A16, A17, B14, B15, B16, B17, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, E13, E14, E15, E16, E17, E18, F13, F14, F15, F16, F17, F18, AE13, AE14, AE15, AE16, AE17, AE18, AF13, AF14, AF15, AF16, AF17, AF18, AG13, AG14, AG15, AG16, AG17, AG18, AH14, AH15, AH16, AH17, AH18, AJ14, AJ15, AJ16, AJ17, AJ18, AK14, AK15, AK16, AK17

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 5768VG Logic Signal Connections

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0C-30	C8	D11
0	0C-28	B6	B11
0	0C-26	A5	E12
0	0C-24	D8	C11
0	0C-22	E8	F12
0	0C-20	B5	B10
0	GNDIO0	GND	GND
0	0C-18	A4	A10
0	0C-16	D7	D10
0	0C-14/VREF0	E7	A9
0	0C-12	C6	E11
0	0C-10	B4	B9
0	0C-8	A3	F11
0	0C-6	NC	A8
0	0C-4	NC	C10
0	0C-2	NC	A7
0	0C-0	NC	E10
0	0D-30	NC	B8
0	0D-28	NC	C8
0	GNDIO0	GND	GND
0	0D-26	NC	F10
0	0D-24	NC	A6
0	0D-22	NC	F9
0	0D-20	NC	C7
0	0D-18	NC	D9
0	0D-16	NC	B7
0	0D-14	D6	E8
0	0D-12	E6	A5
0	0D-10	A2	F8
0	0D-8	B3	C6
0	0D-6	C4	D8
0	0D-4	D5	A3
0	GNDIO0	GND	GND
0	0D-2	NC	A2
0	0D-0	NC	A4
0	0A-0	NC	F7
0	0A-2	NC	C5
0	0A-4	NC	F6
0	0A-6	NC	B3
0	0A-8	NC	NC
0	0A-10	NC	NC
0	GNDIO0	GND	GND
0	0A-12	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0A-14	NC	NC
0	0A-16	NC	B4
0	0A-18	NC	D5
0	0A-20	NC	B1
0	0A-22	NC	D6
0	0A-24	NC	C4
0	0A-26	NC	E4
0	GNDIO0	GND	GND
0	0A-28	B2	C2
0	0A-30	B1	C1
0	0B-30	C2	D1
0	0B-28	C1	D2
0	0B-26	NC	D3
0	0B-24	NC	E1
0	0B-22	NC	E3
0	0B-20	NC	F4
0	0B-18	NC	F1
0	0B-16	NC	F3
0	0B-14	NC	G6
0	0B-12	NC	G1
0	GNDIO0	GND	GND
0	0B-10	NC	G2
0	0B-8	NC	H1
0	0B-6	NC	G3
0	0B-4	NC	H2
0	0B-2	NC	H5
0	0B-0	NC	H6
0	1A-0	F7	J1
0	1A-2	F6	K1
0	1A-4	E5	H3
0	1A-6	D4	J2
0	1A-8	D3	H4
0	1A-10	D2	K2
0	GNDIO0	GND	GND
0	1A-12	D1	J6
0	1A-14	E4	L1
0	1A-16	NC	K3
0	1A-18	NC	J4
0	1A-20	NC	L2
0	1A-22	NC	M1
0	1A-24	NC	K6
0	1A-26	NC	K4
0	1A-28	NC	L3

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
3	4B-24	G11	M19
3	4B-26	F11	M21
3	4B-28	F10	L19
3	4B-30/CLK_OUT1	B11	L20
3	GNDIO3	GND	GND
3	4A-30	NC	M17
3	4A-28	NC	M22
3	4A-26	NC	K20
3	4A-24	NC	L18
3	4A-22	NC	L21
3	4A-20	NC	K19
3	4A-18	NC	L22
3	4A-16	NC	K17
3	4A-14	E13	K22
3	4A-12	B12	L17
3	GNDIO3	GND	GND
3	4A-10	E15	K21
3	4A-8	D15	K18
3	4A-6	NC	J17
3	4A-4	NC	J19
3	4A-2	D16	J22
3	4A-0	E12	J21
3	5B-0	NC	H19
3	5B-2	NC	H20
3	5B-4	NC	H17
3	5B-6	NC	H18
3	5B-8	NC	H22
3	5B-10	NC	H21
3	GNDIO3	GND	GND
3	5B-12	NC	G20
3	5B-14	NC	G22
3	5B-16	NC	G17
3	5B-18	NC	G21
3	5B-20	NC	F19
3	5B-22	NC	F20
3	5B-24	A16	F22
3	5B-26	B15	E22
3	5B-28	A15	E19
3	5B-30	D13	E20
3	5A-30	B14	D22
3	5A-28	B16	D21
3	GNDIO3	GND	GND
3	5A-26	C16	D20

Bank No.	Signal	256 fpBGA	484 fpBGA
3	5A-24	C15	C22
3	5A-22	D14	C18
3	5A-20	A14	C19
3	5A-18	C13	D17
3	5A-16	B13	C21
3	5A-14	NC	NC
3	5A-12	NC	NC
3	GNDIO3	GND	GND
3	5A-10	NC	NC
3	5A-8	NC	NC
3	5A-6	NC	B22
3	5A-4	NC	D18
3	5A-2	NC	B20
3	5A-0	NC	F17
3	5D-0	NC	B19
3	5D-2	NC	C17
3	GNDIO3	GND	GND
3	5D-4	NC	A21
3	5D-6	NC	D15
3	5D-8	NC	A20
3	5D-10	NC	C16
3	5D-12	NC	A19
3	5D-14	NC	F16
3	5D-16	NC	B16
3	5D-18	NC	D14
3	5D-20	NC	A18
3	5D-22	A13	F15
3	5D-24	A12	A17
3	5D-26	A11	B15
3	GNDIO3	GND	GND
3	5D-28	A10	A16
3	5D-30	C11	F14
3	5C-0	A9	C15
3	5C-2	D12	D13
3	5C-4	D11	E15
3	5C-6	B10	F13
3	5C-8	B9	B14
3	5C-10	E11	E13
3	5C-12/VREF3	A8	A15
3	5C-14	D10	D12
3	5C-16	E10	A14
3	5C-18	A7	B13
3	GNDIO3	GND	GND

ispMACH 51024VG Logic Signal Connections

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0C-30	D11	A13
0	0C-28	B11	B13
0	0C-26	E12	A12
0	0C-24	C11	B12
0	0C-22	F12	C12
0	0C-20	B10	A11
0	GNDIO0	GND	GND
0	0C-18	A10	B11
0	0C-16	D10	A10
0	0C-14/VREF0	A9	C11
0	0C-12	E11	E12
0	0C-10	B9	B10
0	0C-8	F11	D11
0	0C-6	A8	A9
0	0C-4	C10	C10
0	0C-2	A7	B9
0	0C-0	E10	A8
0	0D-30	B8	C9
0	0D-28	C8	B8
0	GNDIO0	GND	GND
0	0D-26	F10	E10
0	0D-24	A6	A7
0	0D-22	F9	D9
0	0D-20	C7	C8
0	0D-18	D9	B7
0	0D-16	B7	A6
0	0D-14	E8	C7
0	0D-12	A5	B6
0	0D-10	F8	A5
0	0D-8	C6	C6
0	0D-6	D8	D7
0	0D-4	A3	E8
0	GNDIO0	GND	GND
0	0D-2	A2	B5
0	0D-0	A4	A4
0	0A-0	F7	A3
0	0A-2	C5	B4
0	0A-4	F6	C5
0	0A-6	B3	F8
0	0A-8	NC	A2
0	0A-10	NC	B3
0	GNDIO0	GND	GND
0	0A-12	NC	C4

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0A-14	NC	D5
0	0A-16	B4	E6
0	0A-18	D5	D4
0	0A-20	B1	B1
0	0A-22	D6	C2
0	0A-24	C4	F6
0	0A-26	E4	D3
0	GNDIO0	GND	GND
0	0A-28	C2	E4
0	0A-30	C1	F5
0	0B-30	D1	C1
0	0B-28	D2	D2
0	0B-26	D3	E3
0	0B-24	E1	D1
0	0B-22	E3	E2
0	0B-20	F4	H6
0	0B-18	F1	F3
0	0B-16	F3	E1
0	0B-14	G6	G4
0	0B-12	G1	F2
0	GNDIO0	GND	GND
0	0B-10	G2	H5
0	0B-8	H1	G3
0	0B-6	G3	F1
0	0B-4	H2	G2
0	0B-2	H5	H3
0	0B-0	H6	G1
0	1A-0	J1	H2
0	1A-2	K1	J4
0	1A-4	H3	H1
0	1A-6	J2	J3
0	1A-8	H4	K5
0	1A-10	K2	J2
0	GNDIO0	GND	GND
0	1A-12	J6	J1
0	1A-14	L1	K3
0	1A-16	K3	K2
0	1A-18	J4	K1
0	1A-20	L2	L4
0	1A-22	M1	L3
0	1A-24	K6	L2
0	1A-26	K4	M5
0	1A-28	L3	L1

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
1	3A-4	V4	AJ4
1	3A-2	U7	AK3
1	3A-0	AB2	AK4
1	3D-0	V7	AJ5
1	3D-2	AA5	AH6
1	GNDIO1	GND	GND
1	3D-4	AB3	AF8
1	3D-6	Y6	AG7
1	3D-8	AB4	AK5
1	3D-10	Y7	AJ6
1	3D-12	AB5	AH7
1	3D-14	V8	AK6
1	3D-16	AA7	AJ7
1	3D-18	Y8	AH8
1	3D-20	AB6	AG9
1	3D-22	W8	AK7
1	3D-24	AA8	AF10
1	3D-26	Y10	AJ8
1	GNDIO1	GND	GND
1	3D-28	U8	AH9
1	3D-30	AB7	AK8
1	3C-0	U9	AJ9
1	3C-2	AA9	AH10
1	3C-4	W9	AK9
1	3C-6	AB8	AG11
1	3C-8	U10	AJ10
1	3C-10	AB9	AF12
1	3C-12	V11	AH11
1	3C-14/VREF1	AA10	AK10
1	3C-16	V10	AJ11
1	3C-18	AB10	AK11
1	GNDIO1	GND	GND
1	3C-20	W10	AH12
1	3C-22	W11	AJ12
1	3C-24	U11	AK12
1	3C-26	AA11	AH13
1	3C-28	V12	AJ13
1	3C-30	AB11	AK13
2	4C-30	W12	AK18
2	4C-28	Y11	AK19
2	4C-26	Y12	AJ19
2	4C-24	AB12	AH19
2	4C-22	U12	AK20

Bank No.	Signal	484 fpBGA	676 fpBGA
2	4C-20	AA12	AJ20
2	GNDIO2	GND	GND
2	4C-18	Y13	AK21
2	4C-16	AB13	AH20
2	4C-14	W13	AF19
2	4C-12/VREF2	AA13	AJ21
2	4C-10	U13	AG20
2	4C-8	AB14	AK22
2	4C-6	V13	AH21
2	4C-4	AA14	AJ22
2	4C-2	U14	AK23
2	4C-0	AB15	AH22
2	4D-30	Y15	AJ23
2	4D-28	AB16	AK24
2	GNDIO2	GND	GND
2	4D-26	AA15	AF21
2	4D-24	W14	AG22
2	4D-22	AB17	AH23
2	4D-20	Y16	AJ24
2	4D-18	AA16	AK25
2	4D-16	Y17	AH24
2	4D-14	AB18	AJ25
2	4D-12	V15	AK26
2	4D-10	AB19	AJ26
2	4D-8	W15	AH25
2	4D-6	AB20	AG24
2	4D-4	AA18	AF23
2	GNDIO2	GND	GND
2	4D-2	U15	AK27
2	4D-0	W17	AK28
2	4A-0	U16	AJ27
2	4A-2	AA19	AH26
2	4A-4	V16	AE23
2	4A-6	AB21	AK29
2	4A-8	NC	AJ28
2	4A-10	NC	AH27
2	GNDIO2	GND	GND
2	4A-12	NC	AG26
2	4A-14	NC	AF25
2	4A-16	Y18	AJ29
2	4A-18	W18	AG27
2	4A-20	AA20	AJ30
2	4A-22	W19	AH29

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
2	4A-24	Y19	AE25
2	4A-26	V19	AG28
2	GNDIO2	GND	GND
2	4A-28	Y21	AF27
2	4A-30	W20	AE26
2	4B-30	AA22	AH30
2	4B-28	W21	AG29
2	4B-26	Y22	AF28
2	4B-24	V20	AG30
2	4B-22	V21	AF29
2	4B-20	W22	AC25
2	4B-18	V18	AE28
2	4B-16	U20	AF30
2	4B-14	V22	AD27
2	4B-12	U19	AE29
2	GNDIO2	GND	GND
2	4B-10	U17	AC26
2	4B-8	U22	AD28
2	4B-6	T20	AE30
2	4B-4	T21	AD29
2	4B-2	T17	AC28
2	4B-0	R20	AD30
2	5A-0	NC	AC29
2	5A-2	NC	AB27
2	5A-4	NC	AC30
2	5A-6	NC	AB28
2	5A-8	NC	AA26
2	5A-10	NC	AB29
2	GNDIO2	GND	GND
2	5A-12	NC	AB30
2	5A-14	NC	AA28
2	5A-16	NC	AA29
2	5A-18	NC	AA30
2	5A-20	NC	Y27
2	5A-22	NC	Y28
2	5A-24	NC	Y29
2	5A-26	NC	W26
2	5A-28	NC	Y30
2	5A-30	NC	W28
2	GNDIO2	GND	GND
2	5B-30	NC	W29
2	5B-28	NC	W30
2	5B-26	NC	V25

Bank No.	Signal	484 fpBGA	676 fpBGA
2	5B-24	NC	V26
2	5B-22	NC	V27
2	5B-20	NC	V28
2	5B-18	NC	V29
2	5B-16	NC	V30
2	5B-14	NC	U25
2	5B-12	NC	U27
2	GNDIO2	GND	GND
2	5B-10	NC	U28
2	5B-8	NC	U29
2	5B-6	NC	U30
2	5B-4	NC	T27
2	5B-2	NC	T28
2	5B-0	NC	T29
3	6B-0	R21	T30
3	6B-2	T22	R29
3	6B4/PLL_FBK1	P21	R27
3	6B6/PLL_RST1	N20	R28
3	6B-8	R22	R30
3	6B-10	N21	P30
3	GNDIO3	GND	GND
3	6B-12	M18	P29
3	6B-14	N19	P28
3	6B-16	P22	P27
3	6B-18	M20	N30
3	6B-20	N22	N29
3	6B-22	N17	N28
3	6B-24	M19	N27
3	6B-26	M21	N25
3	6B-28	L19	M30
3	6B-30/CLK_OUT1	L20	M29
3	GNDIO3	GND	GND
3	6A-30	M17	M28
3	6A-28	M22	L30
3	6A-26	K20	M26
3	6A-24	L18	L29
3	6A-22	L21	L28
3	6A-20	K19	L27
3	6A-18	L22	K30
3	6A-16	K17	K29
3	6A-14	K22	K28
3	6A-12	L17	J30
3	GNDIO3	GND	GND

Signal Configuration

ispMACH 5768VG 256-ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF3	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	I/O	I/O	I/O	I/O	I/O/ CLK_OUT1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	B
C	I/O	I/O	VCCO3	I/O	GND	I/O	VCCO3	I/O	I/O	VCCO0	I/O	GND	I/O	VCCO0	I/O	I/O	C
D	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	D
E	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF0	I/O	I/O	I/O	GND	I/O	I/O	E
F	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ PLL_RST0	F
G	I/O	I/O/ PLL_FBK1	VCCO3	I/O	I/O	I/O	GND	GND	GND	GND	I/O/ CLK_OUT0	I/O	I/O	VCCO0	I/O/ PLL_FBK0	I/O	G
H	VCCP1	GOE1	GCLK2	GCLK3	I/O/ PLL_RST1	VCC	GND	GND	GND	GNDP0	VCC	I/O	GCLK0	TDI	TMS	VCCP0	H
J	I/O	GOE0	RESETB	TOE	I/O	VCC	GNDP1	GND	GND	GND	VCC	I/O	GCLK1	TCK	TDO	VCCJ	J
K	I/O	I/O	VCCO2	I/O	I/O	I/O	GND	GND	GND	GND	I/O	I/O	I/O	VCCO1	I/O	I/O	K
L	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	L
M	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	GND	I/O	I/O	M
N	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	VCCO2	I/O	GND	I/O	VCCO2	I/O	I/O	VCCO1	I/O	GND	I/O	VCCO1	I/O	I/O	P
R	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 5768VG

256fpBGA/5768VG

Bottom View

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispMACH 51024VG 676-ball fpBGA

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	B
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O/ VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	C
D	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	D
E	I/O	I/O	I/O	I/O	VCCO3	I/O	VCCO3	I/O	VCCO3	I/O	VCCO3	I/O/ VREF3	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	VCCO0	I/O	VCCO0	I/O	VCCO0	I/O	VCCO0	I/O	I/O	I/O	I/O	E
F	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCCO3	GND	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	GND	VCCO0	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	F
G	I/O	I/O	I/O	I/O	VCCO3	GND																			GND	VCCO0	I/O	I/O	I/O	I/O	G
H	I/O	I/O	I/O	GND	I/O	I/O																			I/O	I/O	GND	I/O	I/O	I/O	H
J	I/O	I/O	I/O	I/O	VCCO3	GND																			GND	VCCO0	I/O	I/O	I/O	I/O	J
K	I/O	I/O	I/O	VCC	I/O	VCCO3																			VCCO0	I/O	VCC	I/O	I/O	I/O	K
L	I/O	I/O	I/O	I/O	VCCO3	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	VCCO0	I/O	I/O	I/O	I/O	L
M	I/O	I/O/ CLK_OUT1	I/O	VCC	I/O	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	I/O	VCC	I/O	I/O/ CLK_OUT0	I/O	M
N	I/O	I/O	I/O	I/O	VCCP1	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	I/O	I/O	GCLK3	GNDP1					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	VCCP0	I/O	I/O	I/O	I/O/ PLL_RST0	P
R	I/O	I/O	I/O/ PLL_RST1	I/O/ PLL_FBK1	GOE1	GCLK2					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GNDP0	GCLK0	I/O/ PLL_FBK0	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	GOE0	RESETB					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GCLK1	TDI	TMS	I/O	I/O	I/O	T
U	I/O	I/O	I/O	I/O	TOE	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					VCCJ	TCK	I/O	I/O	I/O	I/O	U
V	I/O	I/O	I/O	I/O	I/O	I/O					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					I/O	TDO	I/O	I/O	I/O	I/O	V
W	I/O	I/O	I/O	VCC	I/O	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	I/O	VCC	I/O	I/O	I/O	W
Y	I/O	I/O	I/O	I/O	VCCO2	GND					GND	GND	GND	GND	GND	GND	GND	GND	GND	GND					GND	VCCO1	I/O	I/O	I/O	I/O	Y
AA	I/O	I/O	I/O	VCC	I/O	VCCO2																			VCCO1	I/O	VCC	I/O	I/O	I/O	AA
AB	I/O	I/O	I/O	I/O	VCCO2	GND																			GND	VCCO1	I/O	I/O	I/O	I/O	AB
AC	I/O	I/O	I/O	GND	I/O	I/O																			I/O	I/O	GND	I/O	I/O	I/O	AC
AD	I/O	I/O	I/O	I/O	VCCO2	GND																			GND	VCCO1	I/O	I/O	I/O	I/O	AD
AE	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCCO2	GND	GND	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	GND	GND	VCCO1	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	AE
AF	I/O	I/O	I/O	I/O	VCCO2	I/O	VCCO2	I/O	VCCO2	I/O	VCCO2	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	VCCO1	I/O	VCCO1	I/O	VCCO1	I/O	VCCO1	I/O	I/O	I/O	I/O	AF
AG	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	AG
AH	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	AH
AJ	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O	AJ
AK	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC[1]	NC[1]	NC[1]	NC[1]	I/O	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	AK
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 51024VG

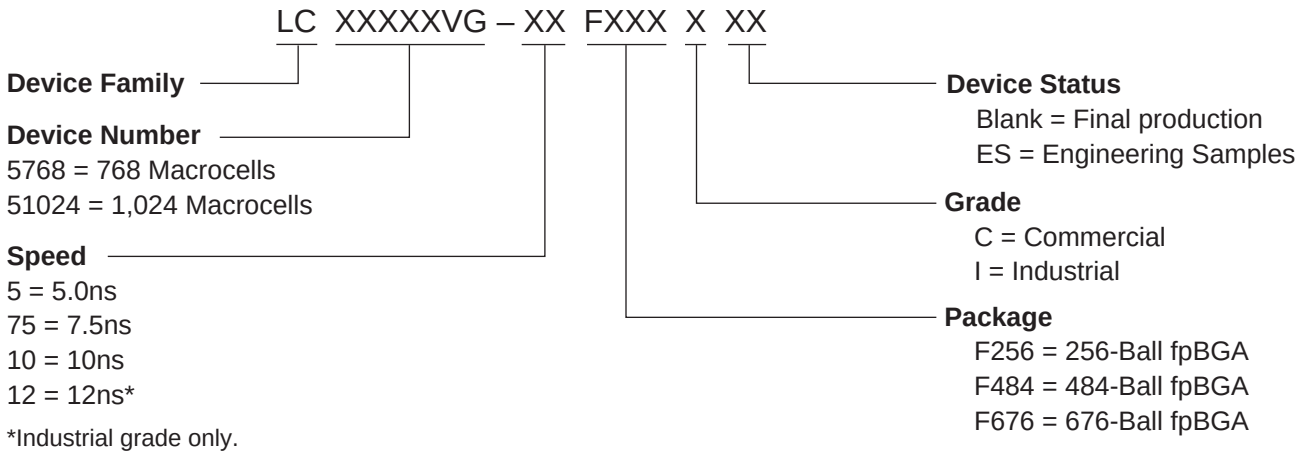
Bottom View

676BGA/51024VG

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/ispm5vg

Ordering Information

Commercial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-5F484C	fpBGA	484	1024	5	3.3
LC51024VG-75F484C	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484C	fpBGA	484	1024	10	3.3
LC51024VG-5F676C	fpBGA	676	1024	5	3.3
LC51024VG-75F676C	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676C	fpBGA	676	1024	10	3.3
LC5768VG-5F256C	fpBGA	256	768	5	3.3
LC5768VG-75F256C	fpBGA	256	768	7.5	3.3
LC5768VG-10F256C	fpBGA	256	768	10	3.3
LC5768VG-5F484C	fpBGA	484	768	5	3.3
LC5768VG-75F484C	fpBGA	484	768	7.5	3.3
LC5768VG-10F484C	fpBGA	484	768	10	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).