Lattice Semiconductor Corporation - LC51024VG-75F676I Datasheet

Welcome to E-XFL.COM

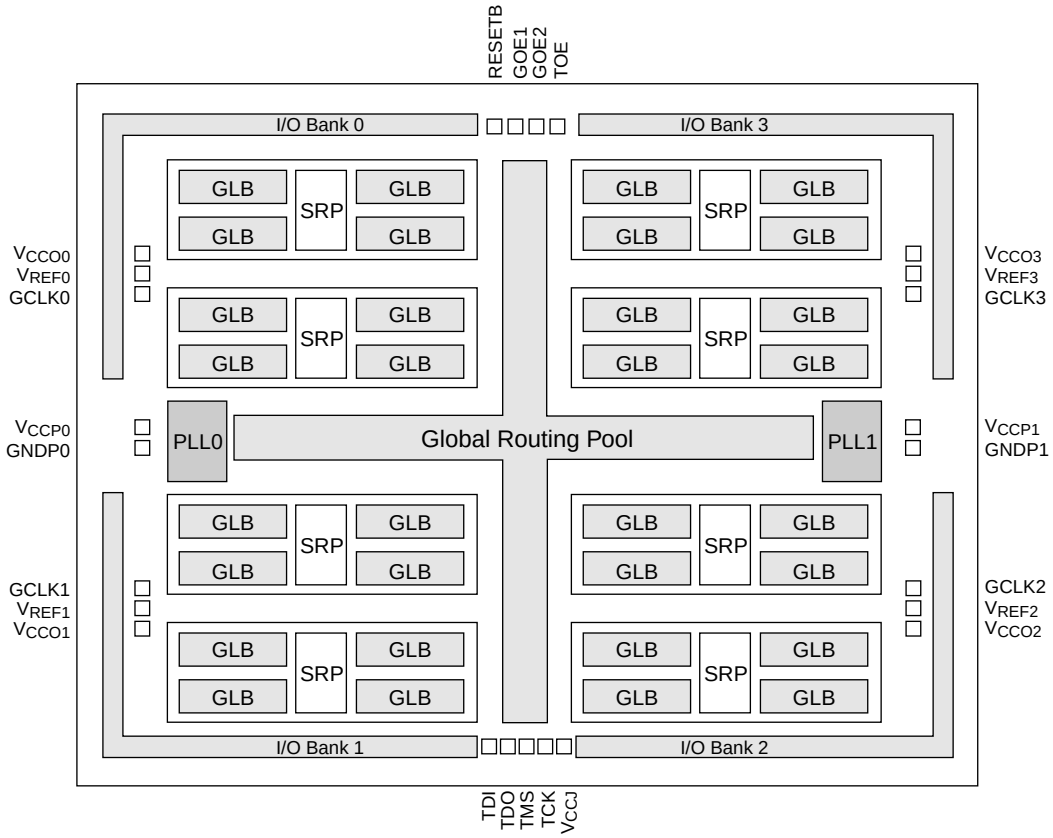
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	32
Number of Macrocells	1024
Number of Gates	-
Number of I/O	384
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	676-BBGA
Supplier Device Package	676-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc51024vg-75f676i

Figure 1. Functional Block Diagram



Overview

The ispMACH 5000VG devices consist of multiple SuperWIDE 68-input, 32-macrocell Generic Logic Blocks (GLBs) interconnected by a tiered routing system. Figure 1 shows the functional block diagram of the ispMACH 5000VG. Groups of four GLBs, referred to as segments, are interconnected via a Segment Routing Pool (SRP). Segments are interconnected via the Global Routing Pool (GRP.) Together the GLBs and the routing pools allow designers to create large designs in a single device without compromising performance.

Each GLB has 68 inputs coming from the SRP and contains 163 product terms. These product terms form groups of five product term clusters, which feed the PT sharing array or the macrocell directly. The ispMACH 5000VG allows up to 160 product terms to be connected to a single macrocell via the product term expanders and PT Sharing Array.

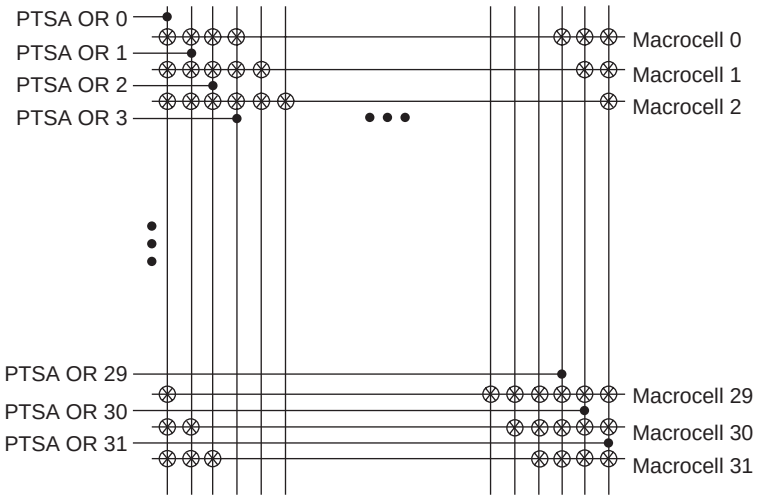
The macrocell is designed to provide flexible clocking and control functionality with the capability to select between global, product term and block-level resources. The outputs of the macrocells are fed back into the switch matrices and, if required, the sysIO cell.

All I/Os in the ispMACH 5000VG family are sysIOs, which are split into four banks. Each bank has a separate I/O power supply and reference voltage. The sysIO cells allow operation with a wide range of today's emerging interface standards. Within a bank, inputs can be set to a variety of standards, providing the reference voltage requirements of the chosen standards are compatible. Within a bank, the outputs can be set to differing standards, providing the I/O power supply voltage and the reference voltage requirements of the chosen standard are compatible. Support for this wide range of standards allows designers to achieve significantly higher board-level performance compared to the more traditional LVCMOS standards.

Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Figure 6 shows the graphical representation of the PTSA.

Figure 6. Product Term Sharing Array



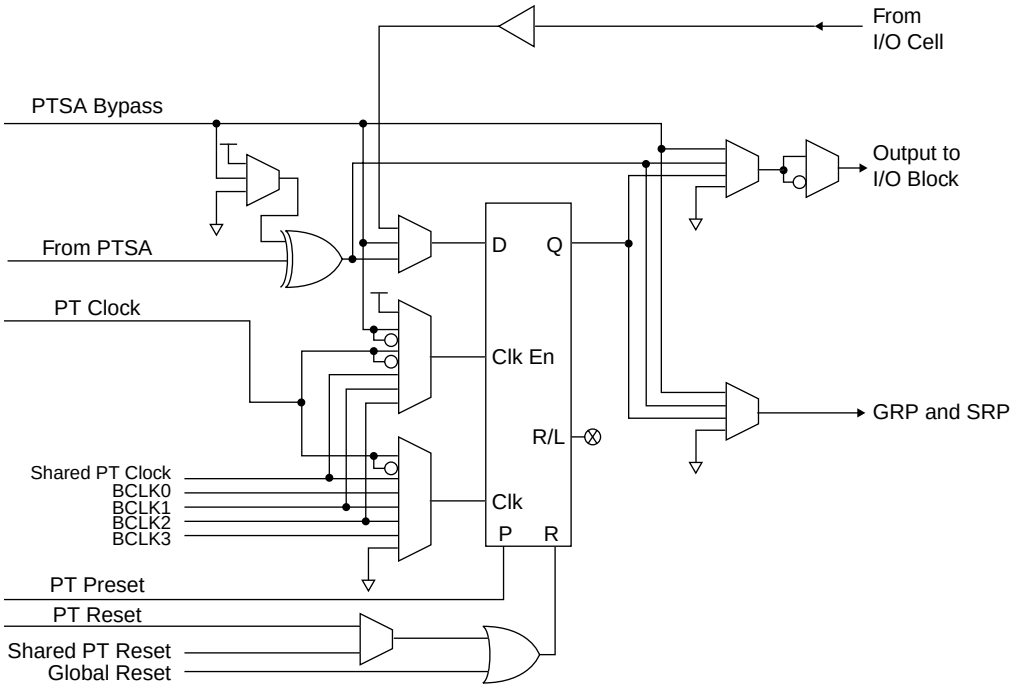
Macrocell

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation.

The macrocells each have two outputs, which can be fed to the SRP, GRP and I/O cell. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 7 is a graphical representation of the ispMACH 5000VG macrocell.

Figure 7. Macrocell



I/O Cell

The I/O cell of the ispMACH 5000VG device provides a high degree of flexibility. It includes the sysIO feature and an enhanced output enable MUX for optimal performance both on- and off-chip. The sysIO feature allows I/O cells to be configured to different I/O standards, drive strengths and slew rates. The enhanced output enable MUX provides up to 14 different output enable choices per I/O cell.

The I/O cell contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. The I/O cell receives its input from its associated macrocell. The I/O cell has a feedback line to its associated macrocell and a direct path to the GRP and SRP.

The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four Shared PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes.

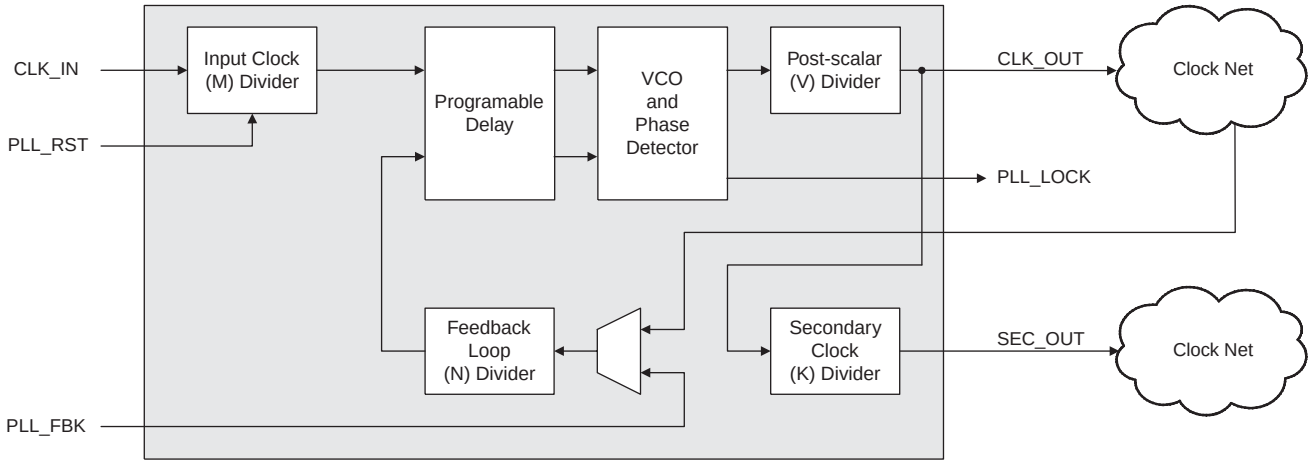
The four shared PTOE signals are derived from PT163 of each GLB in the segment. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 8 is a graphical representation of the I/O cell.

sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispMACH 5000VG devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The PLL outputs (CLK_OUT) are routed via a dedicated net to a dedicated pad. Further the buffers at these dedicated pads are regular I/O buffers that can select either the I/O macrocell or the CLK_OUT (CLK_OUT0/CLK_OUT1) signal. The CLK_OUT nets are not routed through the GRP. Additionally, there are two sets of signals used for external control. Each PLL has a set of PLL_RST, PLL_FBK and PLL_LOCK signals. Figure 10 shows the ispMACH 5000VG PLL block diagram.

Figure 10. PLL Block Diagram



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines in 0.5ns increments from 0 to 3.5ns. For more information on the PLL, please refer to Technical Note TN1003: *ispMACH 5000VG PLL Usage Guidelines* .

Power Management

The ispMACH 5000VG devices provide unique power management controls. The devices have two power settings, high power and low power, on a per node basis. Low power consumption is approximately 50% of high power consumption with a timing delay adder (tLP) to the routing delay of the low power node. Each node can be configured as either high power or low power. However, care should be taken when sharing product terms between nodes with different power settings.

The ispMACH 5000VG devices also have a power-off feature for unused product terms. By default, any product term that is not used is configured as such. This allows the device to operate at minimal power consumption without affecting the timing of the design. For more information on power management, please refer to Technical Note TN1002: *Power Estimation in ispMACH 5000VG Devices*.

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage (V_{CC}) . . . . . -0.5 to 5.4V

PLL Supply Voltage (V_{CCP}) . . . . . -0.5 to 5.4V

Output Supply Voltage (V_{CCO}) . . . . . -0.5 to 5.4V

Input Voltage Applied[4] . . . . . -0.5 to 5.6V

Tri-state Output Voltage Applied. . . . . -0.5 to 5.6V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature (Tj) with Power Applied . . . . . -55 to 130°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of < 20ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE1149.1 Test Access Port	1.65	3.6	V
Tj (Commercial)	Junction Commercial Operation	0	90	C
Tj (Industrial)	Junction Industrial Operation	-40	105	C

Note: V_{CCJ} must be set in appropriate range to be compatible with desired LVCMOS standard.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1000	—	Cycles

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-100	µA
		V_{IH} (MAX) $\le V_{IN} \le$ 5.5V	—	—	+/-100	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO}.
2. LVTTL, LVCMOS only
3. $0 < V_{CC} \le V_{CC}$ (MAX), $0 < V_{CCO} \le V_{CCO}$ (MAX)

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	+/-10	µA
I_{PU}[2]	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	-150	µA
			V_{CCO} = 2.5	-20	—	-150	µA
			V_{CCO} = 1.8	-10	—	-150	µA
I_{PD}[2]	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)		30	—	150	µA
I_{BHLS}[2]	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)		30	—	—	µA
I_{BHHS}[2]	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	—	µA
			V_{CCO} = 2.5	-20	—	—	µA
			V_{CCO} = 1.8	-10	—	—	µA
I_{BHLO}[2]	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	150	µA
I_{BHHO}[2]	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	-150	µA
I_{CC}[3, 4, 5]	Operating Power Supply Current	V_{CC} = 3.3V		—	380	—	mA
V_{BHT}	Bus Hold Trip Points			V_{IL} (MAX)	—	V_{IH} (MIN)	V
C_1	I/O Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_2	Clock Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_3	Global Input Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Only available for LVCMOS and LVTTL standards.
3. T_A = 25°C, f = 1.0MHz.
4. Device configured with 16-bit counters.
5. I_{CC} varies with specific device configuration and operating frequency.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3[1]	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	16, 12 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCO}$	$0.65V_{CCO}$	3.6	0.4	V_{CCO}-0.4	12, 8, 5.33, 4	-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
PCI-X	-0.3	$0.35V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
AGP-1X	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.7	V_{CCO}-1.1	8	-8
SSTL3 class II	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.5	V_{CCO}-0.9	16	-16
SSTL2 class I	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.54	V_{CCO}-0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.35	V_{CCO}-0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
CTT 2.5	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
HSTL class I	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	8	-8
HSTL class III	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	24	-8
GTL+	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.6	n/a	36	n/a

1. Software default setting
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed 96mA.

sysIO Differential Input DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max
V_{INP} . V_{INM}	LVDS Input voltage	—	0	2.4
V_{THD}	LVDS Differential input threshold	—	±100mV	—
V_{IL}	LVPECL Input Voltage Low	V_{CC} = 3.0 to 3.6V	V_{CC}-1.81	V_{CC}-1.48
		V_{CC} = 3.3V	1.49V	1.83V
V_{IH}	LVPECL Input Voltage High	V_{CC} = 3.0 to 3.6V	V_{CC}-1.17	V_{CC}-0.88
		V_{CC} = 3.3V	2.14V	2.42V

ispMACH 5768VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

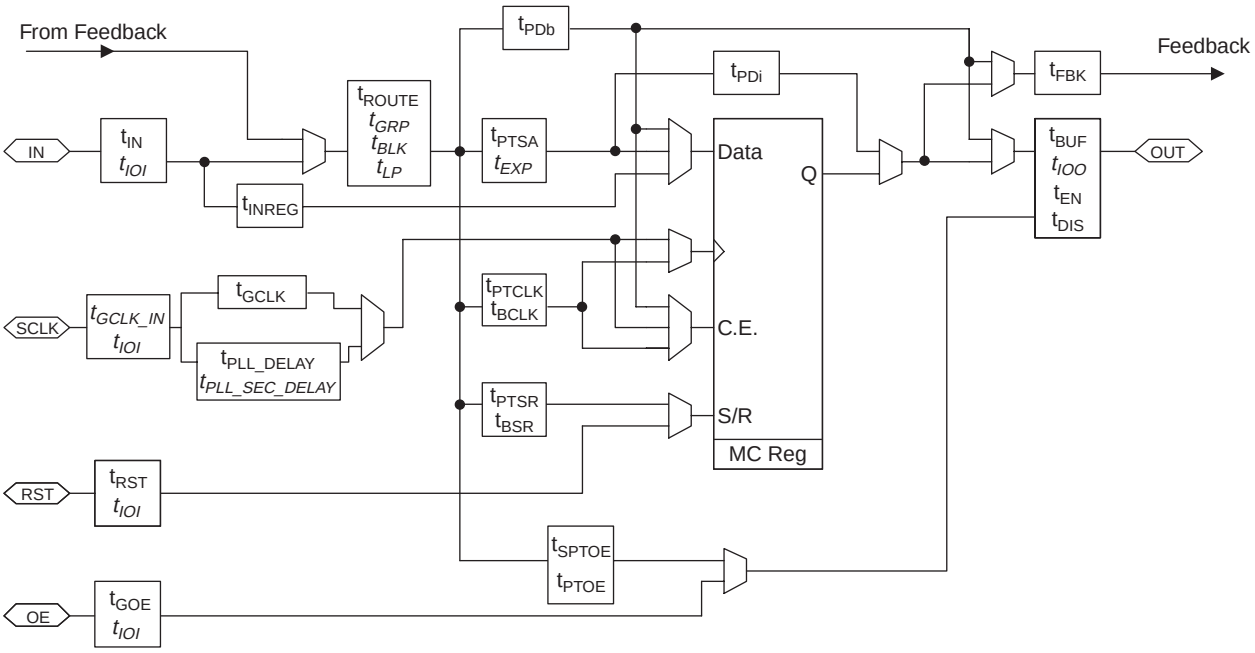
Timing v.1.20

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

Timing Model

The task of determining the timing through the ispMACH 5000VG family, like any CPLD, is relatively simple. The timing model provided in Figure 11 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, please refer to Technical Note TN1001: *ispMACH 5000VG Timing Model Design and Usage Guidelines.*

Figure 11. ispMACH 5000VG Timing Model



Italicized items are optional delay adders

ispMACH 51024VG Internal Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns
t_{BSR}	Block PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{SPTOE}	Segment PT OE Delay	—	2.40	—	3.60	—	7.75	—	9.10	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.40	—	2.10	—	1.75	—	2.10	ns

Notes: Timing v.1.10

1. Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details.
2. t_{PLL_DELAY} is the unit increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to 3.5ns in either direction in units of 0.5ns for each step.

ispMACH 5768VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVDS_in	t_{GCLK_IN}	Using LVDS standard	—	1.70	—	1.70	—	1.70	—	1.70	ns
LVPECL_in	t_{GCLK_IN}	Using LVPECL standard	—	2.10	—	2.10	—	2.10	—	2.10	ns
t_{IOO} Output Adders											
LVCMOS18_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 4mA Buffer	—	3.00	—	3.00	—	3.00	—	3.00	ns
LVCMOS18_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 5.33mA Buffer	—	2.50	—	2.50	—	2.50	—	2.50	ns
LVCMOS18_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 8mA Buffer	—	1.85	—	1.85	—	1.85	—	1.85	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS18_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 12mA Buffer	—	1.35	—	1.35	—	1.35	—	1.35	ns
LVCMOS25_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS25_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS25_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 8mA Buffer	—	0.70	—	0.70	—	0.70	—	0.70	ns
LVCMOS25_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 12mA Buffer	—	0.50	—	0.50	—	0.50	—	0.50	ns
LVCMOS25_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 16mA Buffer	—	0.25	—	0.25	—	0.25	—	0.25	ns
LVCMOS33_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS33_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS33_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 8mA Buffer	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS33_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 12mA Buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS33_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 16mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS33_20mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 20mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{BUF}, t_{EN}, t_{DIS}	Output configured as LVTTL Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.50	—	1.50	—	1.50	—	1.50	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI-X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_out	t_{BUF}, t_{EN}, t_{DIS}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_I standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
SSTL3_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_II standard	—	-0.35	—	-0.35	—	-0.35	—	-0.35	ns
SSTL2_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
HSTL_III_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF}, t_{EN}, t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.20

ispMACH 51024VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.10

ispMACH 51024VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
LVDS_in	t_{GCLK_IN}	Using LVDS standard	—	1.70	—	1.70	—	1.70	—	1.70	ns
LVPECL_in	t_{GCLK_IN}	Using LVPECL standard	—	2.10	—	2.10	—	2.10	—	2.10	ns
t_{IOO} Output Adders											
LVCMOS18_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 4mA Buffer	—	3.00	—	3.00	—	3.00	—	3.00	ns
LVCMOS18_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 5.33mA Buffer	—	2.50	—	2.50	—	2.50	—	2.50	ns
LVCMOS18_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 8mA Buffer	—	1.85	—	1.85	—	1.85	—	1.85	ns
LVCMOS18_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 12mA Buffer	—	1.35	—	1.35	—	1.35	—	1.35	ns
LVCMOS25_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS25_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS25_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 8mA Buffer	—	0.70	—	0.70	—	0.70	—	0.70	ns
LVCMOS25_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 12mA Buffer	—	0.50	—	0.50	—	0.50	—	0.50	ns
LVCMOS25_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 16mA Buffer	—	0.25	—	0.25	—	0.25	—	0.25	ns
LVCMOS33_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS33_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS33_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 8mA Buffer	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS33_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 12mA Buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS33_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 16mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS33_20mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 20mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{BUF}, t_{EN}, t_{DIS}	Output configured as LVTTL Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.50	—	1.50	—	1.50	—	1.50	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI-X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_out	t_{BUF}, t_{EN}, t_{DIS}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_I standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
SSTL3_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_II standard	—	-0.35	—	-0.35	—	-0.35	—	-0.35	ns

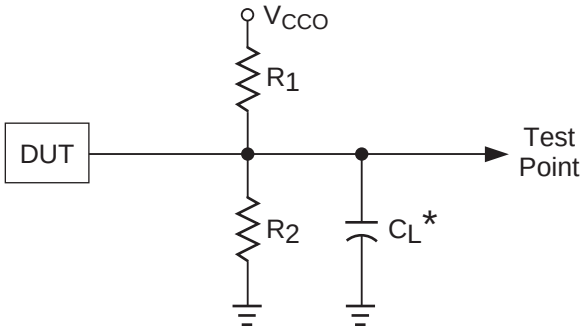
Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes Test Fixture and Probe Capacitance.

0213A/ispm5kvg

Table 3. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 3.3 I/O (L -> H, H -> L)	110	110	35pF	1.5	3.0V
Other LVCMOS Settings, (L -> H, H -> L)	∞	∞	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
Default LVCMOS 3.3 I/O (Z -> H)	∞	110	35pF	1.5V	3.0V
Default LVCMOS 3.3 I/O (Z -> L)	110	∞	35pF	1.5V	3.0V
Default LVCMOS 3.3 I/O (H -> Z)	∞	110	5pF	V_{OH} - 0.3	3.0V
Default LVCMOS 3.3 I/O (L -> Z)	110	∞	5pF	V_{OL} + 0.3	3.0V

Output test conditions for all other interfaces are determined by the respective standards. For further details, please refer to the following technical note:

- *ispMACH 5000VG sysIO Design and Usage Guidelines* (TN1000)

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
0	1A-30	NC	K5
0	GNDIO0	GND	GND
0	1B-30/CLK_OUT0	G6	N1
0	1B-28	NC	M2
0	1B-26	NC	P1
0	1B-24	NC	L4
0	1B-22	F5	N2
0	1B-20	E2	M3
0	1B-18	E1	L5
0	1B-16	F4	R1
0	1B-14	F3	P2
0	1B-12	F2	N3
0	GNDIO0	GND	GND
0	1B-10	G5	M6
0	1B-8	G4	M5
0	1B-6/PLL_RST0	F1	M4
0	1B-4/PLL_FBK0	G2	N4
0	1B-2	G1	N6
0	1B-0	H5	N5
1	2B-0	K1	R5
1	2B-2	K2	T2
1	2B-4	L1	T5
1	2B-6	J5	T3
1	2B-8	L2	U1
1	2B-10	K4	U4
1	GNDIO1	GND	GND
1	2B-12	M1	V1
1	2B-14	L3	U3
1	2B-16	L4	V5
1	2B-18	K5	V2
1	2B-20	M2	W1
1	2B-22	N1	V3
1	2B-24	NC	W2
1	2B-26	K6	Y1
1	2B-28	L5	Y2
1	2B-30	N2	W3
1	2A-30	L6	AA3
1	2A-28	L7	W4
1	GNDIO1	GND	GND
1	2A-26	P1	W5
1	2A-24	P2	Y4
1	2A-22	N3	T6
1	2A-20	R4	Y5

Bank No.	Signal	256 fpBGA	484 fpBGA
1	2A-18	NC	U6
1	2A-16	R1	AA4
1	2A-14	NC	NC
1	2A-12	NC	NC
1	GNDIO1	GND	GND
1	2A-10	NC	NC
1	2A-8	NC	NC
1	2A-6	T1	W6
1	2A-4	T2	V4
1	2A-2	R2	U7
1	2A-0	T3	AB2
1	2D-0	R3	V7
1	2D-2	P4	AA5
1	GNDIO1	GND	GND
1	2D-4	T4	AB3
1	2D-6	N4	Y6
1	2D-8	M4	AB4
1	2D-10	N5	Y7
1	2D-12	R5	AB5
1	2D-14	T5	V8
1	2D-16	NC	AA7
1	2D-18	NC	Y8
1	2D-20	NC	AB6
1	2D-22	T6	W8
1	2D-24	R6	AA8
1	2D-26	P6	Y10
1	GNDIO1	GND	GND
1	2D-28	M5	U8
1	2D-30	T7	AB7
1	2C-0	T8	U9
1	2C-2	R8	AA9
1	2C-4	M6	W9
1	2C-6	N6	AB8
1	2C-8	R7	U10
1	2C-10	T9	AB9
1	2C-12	T10	V11
1	2C-14/VREF1	M7	AA10
1	2C-16	N7	V10
1	2C-18	P8	AB10
1	GNDIO1	GND	GND
1	2C-20	R9	W10
1	2C-22	N8	W11
1	2C-24	M8	U11

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
0	1A-30	K5	M3
0	GNDIO0	GND	GND
0	1B-30/CLK_OUT0	N1	M2
0	1B-28	M2	M1
0	1B-26	P1	N6
0	1B-24	L4	N5
0	1B-22	N2	N4
0	1B-20	M3	N3
0	1B-18	L5	N2
0	1B-16	R1	N1
0	1B-14	P2	P6
0	1B-12	N3	P4
0	GNDIO0	GND	GND
0	1B-10	M6	P3
0	1B-8	M5	P2
0	1B-6/PLL_RST0	M4	P1
0	1B-4/PLL_FBK0	N4	R4
0	1B-2	N6	R3
0	1B-0	N5	R2
1	2B-0	NC	R1
1	2B-2	NC	T1
1	2B-4	NC	T3
1	2B-6	NC	T2
1	2B-8	NC	U1
1	2B-10	NC	U2
1	GNDIO1	GND	GND
1	2B-12	NC	U3
1	2B-14	NC	U4
1	2B-16	NC	V1
1	2B-18	NC	V2
1	2B-20	NC	V3
1	2B-22	NC	V4
1	2B-24	NC	W1
1	2B-26	NC	V6
1	2B-28	NC	W2
1	2B-30	NC	W3
1	GNDIO1	GND	GND
1	2A-30	NC	Y1
1	2A-28	NC	W5
1	2A-26	NC	Y2
1	2A-24	NC	Y3
1	2A-22	NC	AA1
1	2A-20	NC	Y4

Bank No.	Signal	484 fpBGA	676 fpBGA
1	2A-18	NC	AA2
1	2A-16	NC	AA3
1	2A-14	NC	AB1
1	2A-12	NC	AB2
1	GNDIO1	GND	GND
1	2A-10	NC	AA5
1	2A-8	NC	AB3
1	2A-6	NC	AC1
1	2A-4	NC	AB4
1	2A-2	NC	AC2
1	2A-0	NC	AD1
1	3B-0	R5	AC3
1	3B-2	T2	AD2
1	3B-4	T5	AE1
1	3B-6	T3	AD3
1	3B-8	U1	AE2
1	3B-10	U4	AC5
1	GNDIO1	GND	GND
1	3B-12	V1	AF1
1	3B-14	U3	AD4
1	3B-16	V5	AE3
1	3B-18	V2	AC6
1	3B-20	W1	AF2
1	3B-22	V3	AG1
1	3B-24	W2	AF3
1	3B-26	Y1	AG2
1	3B-28	Y2	AH1
1	3B-30	W3	AE5
1	3A-30	AA3	AF4
1	3A-28	W4	AG3
1	GNDIO1	GND	GND
1	3A-26	W5	AE6
1	3A-24	Y4	AH2
1	3A-22	T6	AJ1
1	3A-20	Y5	AG4
1	3A-18	U6	AF6
1	3A-16	AA4	AG5
1	3A-14	NC	AH4
1	3A-12	NC	AJ3
1	GNDIO1	GND	GND
1	3A-10	NC	AK2
1	3A-8	NC	AE8
1	3A-6	W6	AH5

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
2	4A-24	Y19	AE25
2	4A-26	V19	AG28
2	GNDIO2	GND	GND
2	4A-28	Y21	AF27
2	4A-30	W20	AE26
2	4B-30	AA22	AH30
2	4B-28	W21	AG29
2	4B-26	Y22	AF28
2	4B-24	V20	AG30
2	4B-22	V21	AF29
2	4B-20	W22	AC25
2	4B-18	V18	AE28
2	4B-16	U20	AF30
2	4B-14	V22	AD27
2	4B-12	U19	AE29
2	GNDIO2	GND	GND
2	4B-10	U17	AC26
2	4B-8	U22	AD28
2	4B-6	T20	AE30
2	4B-4	T21	AD29
2	4B-2	T17	AC28
2	4B-0	R20	AD30
2	5A-0	NC	AC29
2	5A-2	NC	AB27
2	5A-4	NC	AC30
2	5A-6	NC	AB28
2	5A-8	NC	AA26
2	5A-10	NC	AB29
2	GNDIO2	GND	GND
2	5A-12	NC	AB30
2	5A-14	NC	AA28
2	5A-16	NC	AA29
2	5A-18	NC	AA30
2	5A-20	NC	Y27
2	5A-22	NC	Y28
2	5A-24	NC	Y29
2	5A-26	NC	W26
2	5A-28	NC	Y30
2	5A-30	NC	W28
2	GNDIO2	GND	GND
2	5B-30	NC	W29
2	5B-28	NC	W30
2	5B-26	NC	V25

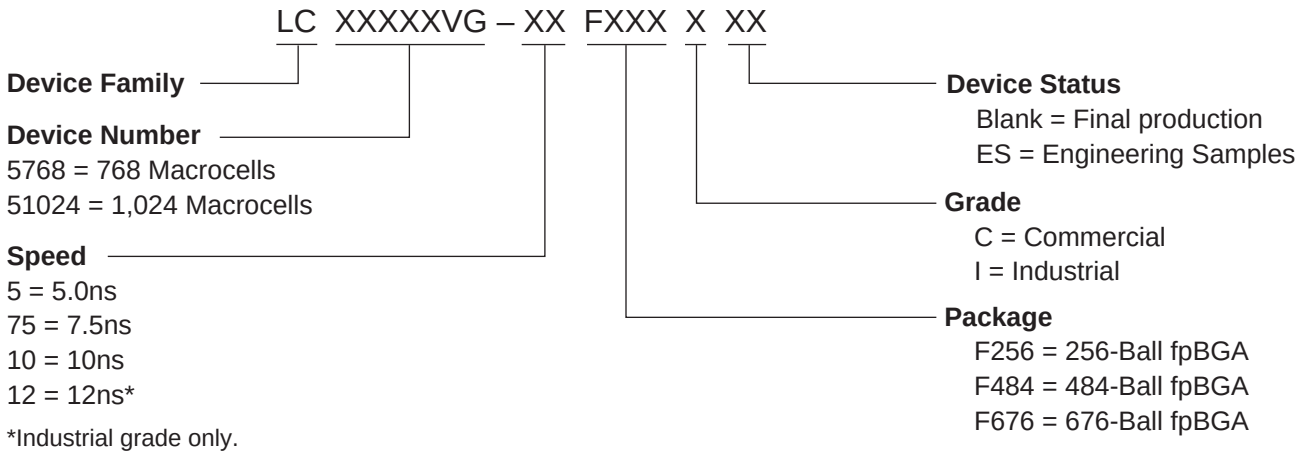
Bank No.	Signal	484 fpBGA	676 fpBGA
2	5B-24	NC	V26
2	5B-22	NC	V27
2	5B-20	NC	V28
2	5B-18	NC	V29
2	5B-16	NC	V30
2	5B-14	NC	U25
2	5B-12	NC	U27
2	GNDIO2	GND	GND
2	5B-10	NC	U28
2	5B-8	NC	U29
2	5B-6	NC	U30
2	5B-4	NC	T27
2	5B-2	NC	T28
2	5B-0	NC	T29
3	6B-0	R21	T30
3	6B-2	T22	R29
3	6B4/PLL_FBK1	P21	R27
3	6B6/PLL_RST1	N20	R28
3	6B-8	R22	R30
3	6B-10	N21	P30
3	GNDIO3	GND	GND
3	6B-12	M18	P29
3	6B-14	N19	P28
3	6B-16	P22	P27
3	6B-18	M20	N30
3	6B-20	N22	N29
3	6B-22	N17	N28
3	6B-24	M19	N27
3	6B-26	M21	N25
3	6B-28	L19	M30
3	6B-30/CLK_OUT1	L20	M29
3	GNDIO3	GND	GND
3	6A-30	M17	M28
3	6A-28	M22	L30
3	6A-26	K20	M26
3	6A-24	L18	L29
3	6A-22	L21	L28
3	6A-20	K19	L27
3	6A-18	L22	K30
3	6A-16	K17	K29
3	6A-14	K22	K28
3	6A-12	L17	J30
3	GNDIO3	GND	GND

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
3	6A-10	K21	J29
3	6A-8	K18	K26
3	6A-6	J17	J28
3	6A-4	J19	H30
3	6A-2	J22	J27
3	6A-0	J21	H29
3	7B-0	H19	G30
3	7B-2	H20	H28
3	7B-4	H17	G29
3	7B-6	H18	F30
3	7B-8	H22	G28
3	7B-10	H21	H26
3	GNDIO3	GND	GND
3	7B-12	G20	F29
3	7B-14	G22	G27
3	7B-16	G17	E30
3	7B-18	G21	F28
3	7B-20	F19	H25
3	7B-22	F20	E29
3	7B-24	F22	D30
3	7B-26	E22	E28
3	7B-28	E19	D29
3	7B-30	E20	C30
3	7A-30	D22	F26
3	7A-28	D21	E27
3	GNDIO3	GND	GND
3	7A-26	D20	D28
3	7A-24	C22	F25
3	7A-22	C18	C29
3	7A-20	C19	B30
3	7A-18	D17	D27
3	7A-16	C21	E25
3	7A-14	NC	D26
3	7A-12	NC	C27
3	GNDIO3	GND	GND
3	7A-10	NC	B28
3	7A-8	NC	A29
3	7A-6	B22	F23
3	7A-4	D18	C26
3	7A-2	B20	B27
3	7A-0	F17	A28
3	7D-0	B19	A27
3	7D-2	C17	B26

Bank No.	Signal	484 fpBGA	676 fpBGA
3	GNDIO3	GND	GND
3	7D-4	A21	E23
3	7D-6	D15	D24
3	7D-8	A20	C25
3	7D-10	C16	A26
3	7D-12	A19	B25
3	7D-14	F16	C24
3	7D-16	B16	A25
3	7D-18	D14	B24
3	7D-20	A18	C23
3	7D-22	F15	D22
3	7D-24	A17	A24
3	7D-26	B15	E21
3	GNDIO3	GND	GND
3	7D-28	A16	B23
3	7D-30	F14	C22
3	7C-0	C15	A23
3	7C-2	D13	B22
3	7C-4	E15	C21
3	7C-6	F13	A22
3	7C-8	B14	D20
3	7C-10	E13	B21
3	7C-12/VREF3	A15	E19
3	7C-14	D12	C20
3	7C-16	A14	A21
3	7C-18	B13	B20
3	GNDIO3	GND	GND
3	7C-20	A13	A20
3	7C-22	B12	C19
3	7C-24	C13	B19
3	7C-26	A12	A19
3	7C-28	C12	B18
3	7C-30	A11	A18
—	GCLK0	P6	R5
—	GCLK1	R6	T6
—	GCLK2	P17	R25
—	GCLK3	P19	P26
—	GOE0	R18	T26
—	GOE1	R17	R26
—	RESETB	R19	T25
—	TCK	R3	U5
—	TDI	R2	T5
—	TDO	R4	V5

Part Number Description



0212/ispm5vg

Ordering Information

Commercial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-5F484C	fpBGA	484	1024	5	3.3
LC51024VG-75F484C	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484C	fpBGA	484	1024	10	3.3
LC51024VG-5F676C	fpBGA	676	1024	5	3.3
LC51024VG-75F676C	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676C	fpBGA	676	1024	10	3.3
LC5768VG-5F256C	fpBGA	256	768	5	3.3
LC5768VG-75F256C	fpBGA	256	768	7.5	3.3
LC5768VG-10F256C	fpBGA	256	768	10	3.3
LC5768VG-5F484C	fpBGA	484	768	5	3.3
LC5768VG-75F484C	fpBGA	484	768	7.5	3.3
LC5768VG-10F484C	fpBGA	484	768	10	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).