Lattice Semiconductor Corporation - LC5768VG-10F256C Datasheet

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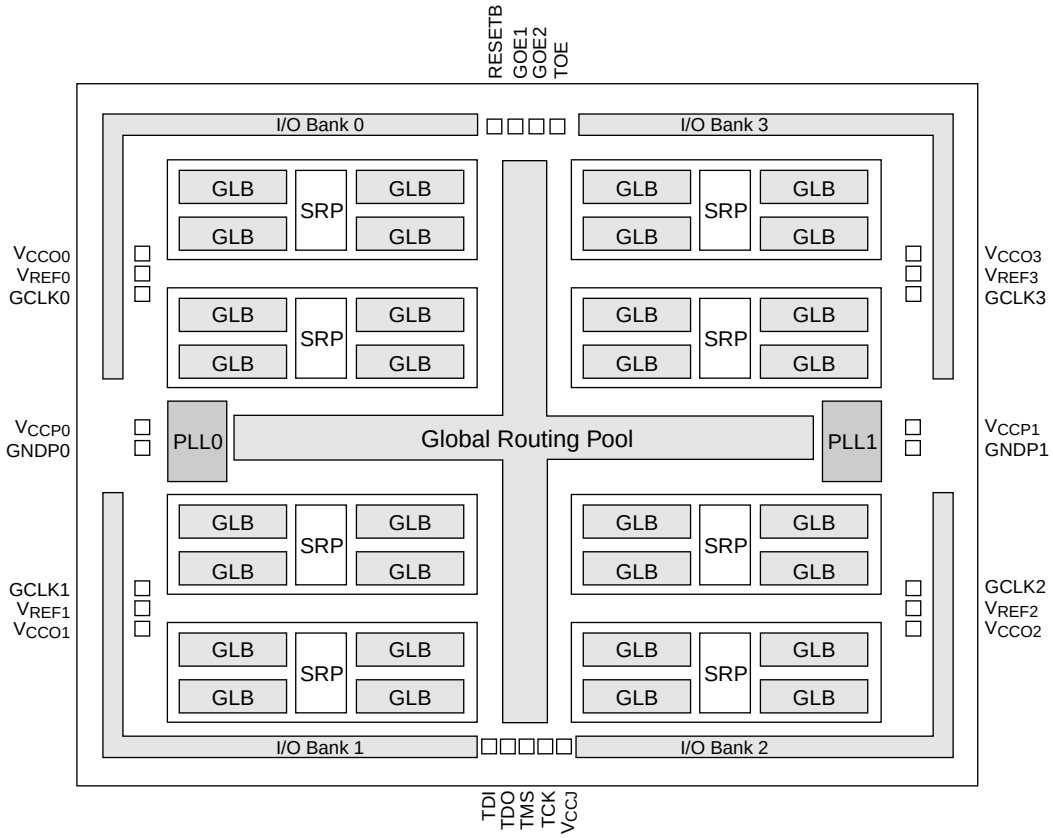
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	196
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768vg-10f256c

Figure 1. Functional Block Diagram



Overview

The ispMACH 5000VG devices consist of multiple SuperWIDE 68-input, 32-macrocell Generic Logic Blocks (GLBs) interconnected by a tiered routing system. Figure 1 shows the functional block diagram of the ispMACH 5000VG. Groups of four GLBs, referred to as segments, are interconnected via a Segment Routing Pool (SRP). Segments are interconnected via the Global Routing Pool (GRP.) Together the GLBs and the routing pools allow designers to create large designs in a single device without compromising performance.

Each GLB has 68 inputs coming from the SRP and contains 163 product terms. These product terms form groups of five product term clusters, which feed the PT sharing array or the macrocell directly. The ispMACH 5000VG allows up to 160 product terms to be connected to a single macrocell via the product term expanders and PT Sharing Array.

The macrocell is designed to provide flexible clocking and control functionality with the capability to select between global, product term and block-level resources. The outputs of the macrocells are fed back into the switch matrices and, if required, the sysIO cell.

All I/Os in the ispMACH 5000VG family are sysIOs, which are split into four banks. Each bank has a separate I/O power supply and reference voltage. The sysIO cells allow operation with a wide range of today's emerging interface standards. Within a bank, inputs can be set to a variety of standards, providing the reference voltage requirements of the chosen standards are compatible. Within a bank, the outputs can be set to differing standards, providing the I/O power supply voltage and the reference voltage requirements of the chosen standard are compatible. Support for this wide range of standards allows designers to achieve significantly higher board-level performance compared to the more traditional LVCMOS standards.

The ispMACH5000VG devices also contain sysCLOCK Phase Locked Loops (PLLs) that provide designers with increased clocking flexibility. The PLLs can be used to synthesize new clocks for use on-chip or elsewhere within the system. They can also be used to deskew clocks, again both at the chip and system levels. A variable delay line capability further improves this and allows designers to retard or advance the clock in order to tune set-up and clock-to-out times for optimal results. The ispMACH 5000VG Family Selection Guide (Table 1) details the key attributes and packages for the ispMACH 5000VG devices.

ispMACH 5000VG Architecture

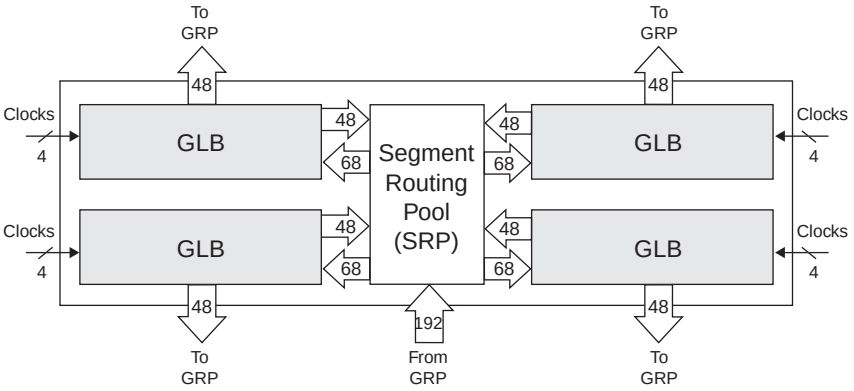
The ispMACH 5000VG Family of In-System Programmable High Density Logic Devices is based on segments containing four Generic Logic Blocks (GLBs) and a hierarchical routing pool (GRP) structure interconnecting the segments. A segment routing pool (SRP) connects each GLB in a segment allowing the maximum flexibility and speed.

Outputs from the GLBs drive the Segment Routing Pool (SRP) and the Global Routing Pool (GRP). Enhanced switching resources are provided to allow signals in the Segment Routing Pool to drive any or all the GLBs in the segment. Optimal switching is provided to allow all signals in the Global Routing Pool to be routed to any or all SRPs. This mechanism allows fast, efficient connections across the entire device.

Segment

Each segment contains four GLBs and a segment routing pool (SRP). Each GLB has 32 internal feedback outputs and 16 external feedback outputs, for a total of 48 outputs from each GLB feeding the SRP. The SRP contains up to 384 signals, 48 from each GLB and 192 from the GRP, with full routing capability. This routing scheme maximizes the flexibility and speed of the device without sacrificing the routing.

Figure 2. Segment



Generic Logic Block

Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and three control product terms. The GLB has 68 inputs from the Segment Routing Pool, which are available in both true and complement form for every product term. The three control product terms are used for shared reset, clock and output enable functions. Figure 3 shows the structure of the GLB from the macrocell perspective. This is referred to as a macrocell slice. There are 32 macrocell slices per GLB.

AND-Array

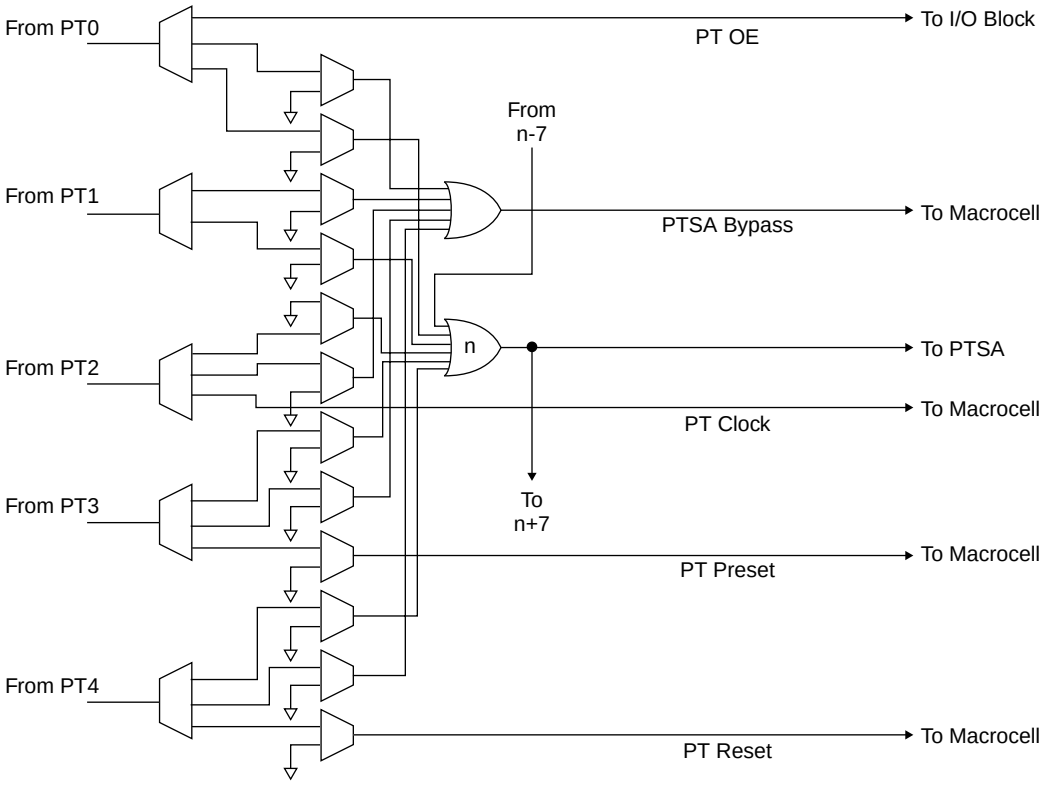
The programmable AND-Array consists of 68 inputs and 163 output product terms. The 68 inputs from the SRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 163 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining three control product terms feeding the Shared PT Clock, Shared PT Reset and Shared PT OE. Every set of five product terms from the 160 logic product terms forms a product term cluster start-

Enhanced Dual-OR Array

To facilitate logic functions requiring a very large number of product terms, the ispMACH 5000VG architecture has been enhanced with an innovative product term expander capability. This capability is embedded in the Dual-OR Array. The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the GLB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate.

The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 5 is a graphical representation of the Enhanced Dual-OR Array.

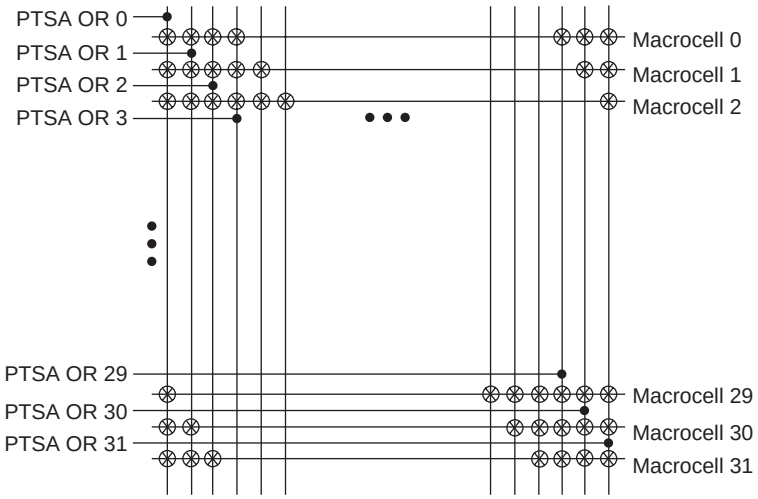
Figure 5. Enhanced Dual-OR Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Figure 6 shows the graphical representation of the PTSA.

Figure 6. Product Term Sharing Array



Macrocell

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation.

The macrocells each have two outputs, which can be fed to the SRP, GRP and I/O cell. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 7 is a graphical representation of the ispMACH 5000VG macrocell.

Global clock pins have additional capabilities that allow for higher performance applications. Two global clock pins can be paired together to create a single global clock pin that can interface with certain differential signals.

The TOE and JTAG pins of the ispMACH 5000VG device are the only pins that do not have sysIO capabilities. These pins only support the LVTTL and LVCMOS standards.

There are three classes of I/O interface standards that are implemented in the ispMACH 5000VG devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Usage of these particular I/O interfaces requires the use of an additional VREF signal. At the system level, a termination voltage, VTT, is also required. Typically, an output will be terminated to VTT at the receiving end of the transmission line it is driving.

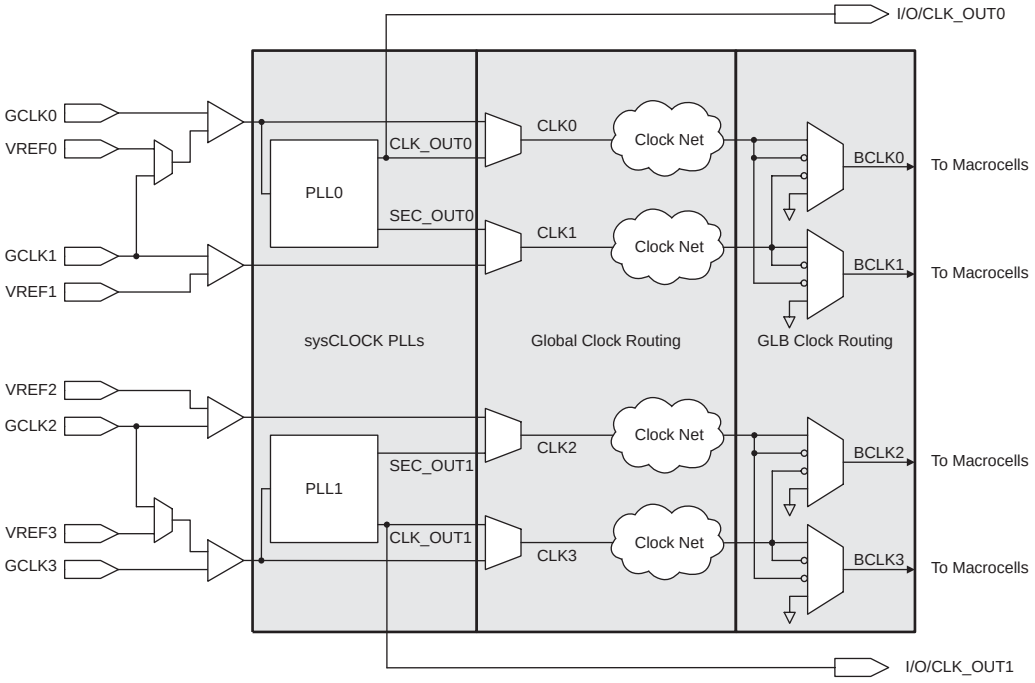
The final types of interfaces implemented are the differential standards LVDS and LVPECL. These interfaces are implemented on clock pins only. When using one of the differential standards, a pair of global clock pins (GCLK0 and GCLK1 or GCLK3 and GCLK2) is combined to create a single clock signal.

For more information on the sysIO capability, please refer to Technical Note TN1000: *ispMACH 5000VG sysIO Design and Usage Guidelines* .

GLB Clock Distribution

The ispMACH 5000VG family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the GLB clock multiplexes which generate the GLB clock signals (BCLK0-BCLK3). The GLB clock multiplexer allows a variety of true and complementary versions of the clocks to be used within the GLB. Each block clock can be the true or inverse of its associated global clock or the inverse of the adjacent global clock. Figure 9 shows the clock distribution network.

Figure 9. Clock Distribution Network

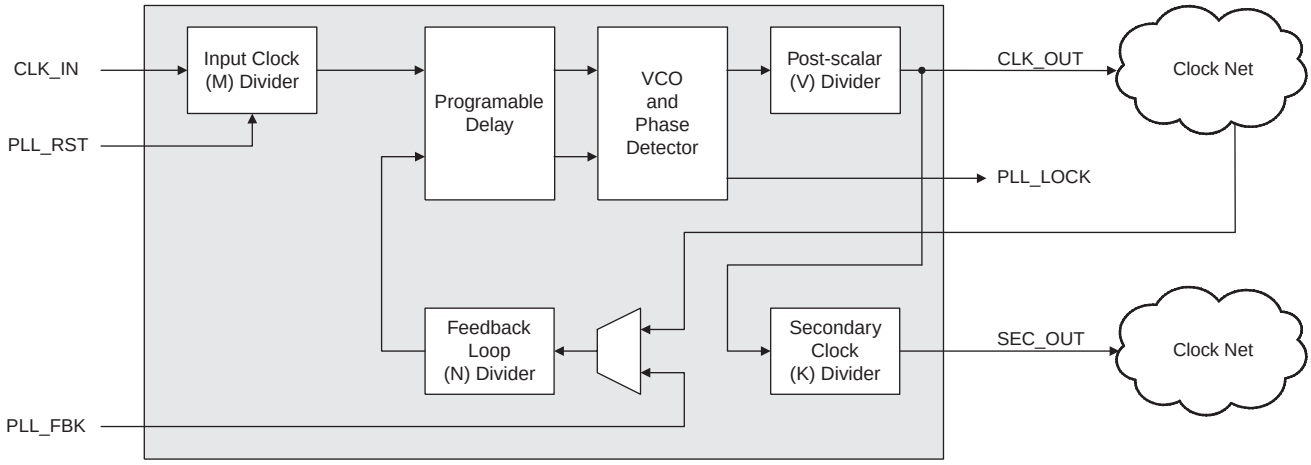


sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispMACH 5000VG devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The PLL outputs (CLK_OUT) are routed via a dedicated net to a dedicated pad. Further the buffers at these dedicated pads are regular I/O buffers that can select either the I/O macrocell or the CLK_OUT (CLK_OUT0/CLK_OUT1) signal. The CLK_OUT nets are not routed through the GRP. Additionally, there are two sets of signals used for external control. Each PLL has a set of PLL_RST, PLL_FBK and PLL_LOCK signals. Figure 10 shows the ispMACH 5000VG PLL block diagram.

Figure 10. PLL Block Diagram



In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit.

The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. This operates by inserting delay on the input or feedback lines in 0.5ns increments from 0 to 3.5ns. For more information on the PLL, please refer to Technical Note TN1003: *ispMACH 5000VG PLL Usage Guidelines* .

Power Management

The ispMACH 5000VG devices provide unique power management controls. The devices have two power settings, high power and low power, on a per node basis. Low power consumption is approximately 50% of high power consumption with a timing delay adder (tLP) to the routing delay of the low power node. Each node can be configured as either high power or low power. However, care should be taken when sharing product terms between nodes with different power settings.

The ispMACH 5000VG devices also have a power-off feature for unused product terms. By default, any product term that is not used is configured as such. This allows the device to operate at minimal power consumption without affecting the timing of the design. For more information on power management, please refer to Technical Note TN1002: *Power Estimation in ispMACH 5000VG Devices*.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 5000VG devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispMACH 5000VG family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 5000VG devices provide In-System Programming (ISP™) capability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The ispMACH 5000VG devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 5000VG devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 5000VG devices during the testing of a circuit board.

Security Bit

A programmable security bit is provided on the ispMACH 5000VG devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary design from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Hot Socketing

The ispMACH 5000VG devices are well suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Density Migration

The ispMACH 5000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	+/-10	µA
I_{PU}[2]	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	-150	µA
			V_{CCO} = 2.5	-20	—	-150	µA
			V_{CCO} = 1.8	-10	—	-150	µA
I_{PD}[2]	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)		30	—	150	µA
I_{BHLS}[2]	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)		30	—	—	µA
I_{BHHS}[2]	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	—	µA
			V_{CCO} = 2.5	-20	—	—	µA
			V_{CCO} = 1.8	-10	—	—	µA
I_{BHLO}[2]	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	150	µA
I_{BHHO}[2]	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	-150	µA
I_{CC}[3, 4, 5]	Operating Power Supply Current	V_{CC} = 3.3V		—	380	—	mA
V_{BHT}	Bus Hold Trip Points			V_{IL} (MAX)	—	V_{IH} (MIN)	V
C_1	I/O Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_2	Clock Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_3	Global Input Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Only available for LVCMOS and LVTTL standards.
3. T_A = 25°C, f = 1.0MHz.
4. Device configured with 16-bit counters.
5. I_{CC} varies with specific device configuration and operating frequency.

ispMACH 5768VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.20

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 51024VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.10

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 5768VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL\_SEC\_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{H}	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns

ispMACH 5768VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVDS_in	t_{GCLK_IN}	Using LVDS standard	—	1.70	—	1.70	—	1.70	—	1.70	ns
LVPECL_in	t_{GCLK_IN}	Using LVPECL standard	—	2.10	—	2.10	—	2.10	—	2.10	ns
t_{IOO} Output Adders											
LVCMOS18_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 4mA Buffer	—	3.00	—	3.00	—	3.00	—	3.00	ns
LVCMOS18_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 5.33mA Buffer	—	2.50	—	2.50	—	2.50	—	2.50	ns
LVCMOS18_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 8mA Buffer	—	1.85	—	1.85	—	1.85	—	1.85	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
HSTL_III_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF}, t_{EN}, t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.20

ispMACH 51024VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.10

sysCLOCK PLL Timing

Over Recommended Operating Conditions[1]

Symbol	Parameter	Conditions	Min	Max	Units
t_R,t_F	Input clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, period jitter (peak)[1]	—	—	+/- 200	ps
t_{PWH}	Input clock, high time	—	1.6	—	ns
t_{PWL}	Input clock, low time	—	1.6	—	ns
f_{MDIVIN}	M Divider input, frequency range	—	5	180	MHz
$f_{MDIVOUT}$	M Divider output, frequency range	—	5	180	MHz
f_{VDIVIN}	V Divider input, frequency range	—	60	200	MHz
$f_{VDIVOUT}$	V Divider output, frequency range	—	5	180	MHz
$t_{OUTDUTY}$	Output clock, duty cycle	—	40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean Reference, 5MHz ≤ $f_{MDIVOUT}$ < 80MHz	—	+/- 200	ps
		Clean Reference, 80MHz ≤ $f_{MDIVOUT}$ ≤ 180MHz	—	+/- 100	ps
$t_{JIT(\phi)}$	Output clock, accumulated phase jitter (peak)[2]	Clean Reference, 5MHz ≤ $f_{MDIVOUT}$ < 80MHz	—	+/- 200	ps
		Clean Reference, 80MHz ≤ $f_{MDIVOUT}$ ≤ 180MHz	—	+/- 100	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	1	ns
t_ϕ	Input clock to external feedback delta	External feedback	—	500	ps
t_{LOCK}	Time to acquire phase lock after input stable	—	—	30	µs
t_{PLL_DELAY}	Delay increment	—	+/- 0.35	+/- 0.65	ns
t_{RANGE}	Total output delay range	—	+/- 2.45	+/- 4.55	ns
t_{PLL_RSTR}	Reset recovery time of the M-divider	—	11.0	—	ns
t_{PLL_RSTW}	Minimum reset pulse width	—	6.0	—	ns

1. This condition assures that the output phase jitter ($t_{JIT(\phi)}$) will remain within specification.
2. Accumulated jitter measured over 10,000 waveform samples.

Boundary Scan Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
$t_{BVTCPSU}$	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

ispMACH 5768VG Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[2]	484-Ball fpBGA[2]
V_{CC}	F8, F9, H6, H11, J6, J11, L8, L9	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6
V_{CCO0}	C3, C7, G3	B5, D7, E2, E6, E9, F5, G4, J5
V_{CCO1}	K3, P3, P7	P5, U5, V6, V9, Y3
V_{CCO2}	K14, P10, P14	P18, U18, V14, V17, Y20
V_{CCO3}	C10, C14, G14	B18, D16, E14, E17, E21, F18, G19, J18
V_{CCP0}	H1	L7
V_{CCP1}	H16	N18
V_{CCJ}	J1	P4
V_{REF0}	E7	A9
V_{REF1}	M7	AA10
V_{REF2}	R13	AA13
V_{REF3}	A8	A15
GND PLL 0	H7	L6
GND PLL 1	J10	L16
GND	A1, C5, C12, E3, E14, G7, G8, G9, G10, H8, H9, H10, J7, J8, J9, K7, K8, K9, K10, M3, M14, P5, P12	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22
NC[3]	—	AA1

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 51024 Power Supply and NC Connections[1]

Signal	484-Ball fpBGA[2]	676-Ball fpBGA[2]
V_{CC}	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6	B29, D6, D10, D12, D19, D21, D25, F4, F27, K4, K27, M4, M27, W4, W27, AA4, AA27, AE4, AE27, AG6, AG10, AG12, AG19, AG21,AG25, AJ2
V_{CCO0}	B5, D7, E2, E6, E9, F5, G4, J5	E5, E7, E9, E11, F10, G5, J5, K6, L5
V_{CCO1}	P5, U5, V6, V9, Y3	Y5, AA6, AB5, AD5, AE10, AF5, AF7, AF9, AF11
V_{CCO2}	P18, U18, V14, V17, Y20	Y26, AA25, AB26, AD26, AE21, AF20, AF22, AF24, AF26
V_{CCO3}	B18, D16, E14, E17, E21, F18, G19, J18	E20, E22, E24, E26, F21, G26, J26, K25, L26
V_{CCP0}	L7	P5
V_{CCP1}	N18	N26
V_{CCJ}	P4	U6
V_{REF0}	A9	C11
V_{REF1}	AA10	AK10
V_{REF2}	AA13	AJ21
V_{REF3}	A15	E19
GND PLL 0	L6	R6
GND PLL 1	L16	P25
GND	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22	A1, A30, B2,C3, C28, D8, D23, F7, F9, F11, F12, F19, F20, F22, F24, G6, G25, H4, H27, J6, J25, L6, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L25, M6, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M25, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14,U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W25, Y6, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y25, AB6, AB25, AC4, AC27, AD6, AD25, AE7, AE9, AE11, AE12, AE19, AE20, AE22, AE24, AG8, AG23, AH3, AH28, AK1, AK30
NC[3]	AA1	A14, A15, A16, A17, B14, B15, B16, B17, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, E13, E14, E15, E16, E17, E18, F13, F14, F15, F16, F17, F18, AE13, AE14, AE15, AE16, AE17, AE18, AF13, AF14, AF15, AF16, AF17, AF18, AG13, AG14, AG15, AG16, AG17, AG18, AH14, AH15, AH16, AH17, AH18, AJ14, AJ15, AJ16, AJ17, AJ18, AK14, AK15, AK16, AK17

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
2	4A-24	Y19	AE25
2	4A-26	V19	AG28
2	GNDIO2	GND	GND
2	4A-28	Y21	AF27
2	4A-30	W20	AE26
2	4B-30	AA22	AH30
2	4B-28	W21	AG29
2	4B-26	Y22	AF28
2	4B-24	V20	AG30
2	4B-22	V21	AF29
2	4B-20	W22	AC25
2	4B-18	V18	AE28
2	4B-16	U20	AF30
2	4B-14	V22	AD27
2	4B-12	U19	AE29
2	GNDIO2	GND	GND
2	4B-10	U17	AC26
2	4B-8	U22	AD28
2	4B-6	T20	AE30
2	4B-4	T21	AD29
2	4B-2	T17	AC28
2	4B-0	R20	AD30
2	5A-0	NC	AC29
2	5A-2	NC	AB27
2	5A-4	NC	AC30
2	5A-6	NC	AB28
2	5A-8	NC	AA26
2	5A-10	NC	AB29
2	GNDIO2	GND	GND
2	5A-12	NC	AB30
2	5A-14	NC	AA28
2	5A-16	NC	AA29
2	5A-18	NC	AA30
2	5A-20	NC	Y27
2	5A-22	NC	Y28
2	5A-24	NC	Y29
2	5A-26	NC	W26
2	5A-28	NC	Y30
2	5A-30	NC	W28
2	GNDIO2	GND	GND
2	5B-30	NC	W29
2	5B-28	NC	W30
2	5B-26	NC	V25

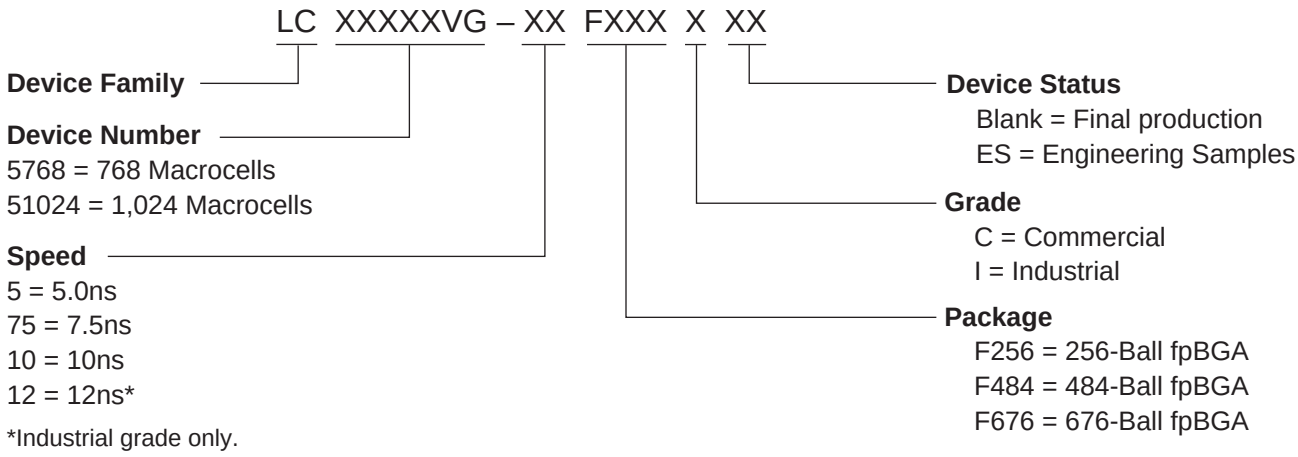
Bank No.	Signal	484 fpBGA	676 fpBGA
2	5B-24	NC	V26
2	5B-22	NC	V27
2	5B-20	NC	V28
2	5B-18	NC	V29
2	5B-16	NC	V30
2	5B-14	NC	U25
2	5B-12	NC	U27
2	GNDIO2	GND	GND
2	5B-10	NC	U28
2	5B-8	NC	U29
2	5B-6	NC	U30
2	5B-4	NC	T27
2	5B-2	NC	T28
2	5B-0	NC	T29
3	6B-0	R21	T30
3	6B-2	T22	R29
3	6B4/PLL_FBK1	P21	R27
3	6B6/PLL_RST1	N20	R28
3	6B-8	R22	R30
3	6B-10	N21	P30
3	GNDIO3	GND	GND
3	6B-12	M18	P29
3	6B-14	N19	P28
3	6B-16	P22	P27
3	6B-18	M20	N30
3	6B-20	N22	N29
3	6B-22	N17	N28
3	6B-24	M19	N27
3	6B-26	M21	N25
3	6B-28	L19	M30
3	6B-30/CLK_OUT1	L20	M29
3	GNDIO3	GND	GND
3	6A-30	M17	M28
3	6A-28	M22	L30
3	6A-26	K20	M26
3	6A-24	L18	L29
3	6A-22	L21	L28
3	6A-20	K19	L27
3	6A-18	L22	K30
3	6A-16	K17	K29
3	6A-14	K22	K28
3	6A-12	L17	J30
3	GNDIO3	GND	GND

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
3	6A-10	K21	J29
3	6A-8	K18	K26
3	6A-6	J17	J28
3	6A-4	J19	H30
3	6A-2	J22	J27
3	6A-0	J21	H29
3	7B-0	H19	G30
3	7B-2	H20	H28
3	7B-4	H17	G29
3	7B-6	H18	F30
3	7B-8	H22	G28
3	7B-10	H21	H26
3	GNDIO3	GND	GND
3	7B-12	G20	F29
3	7B-14	G22	G27
3	7B-16	G17	E30
3	7B-18	G21	F28
3	7B-20	F19	H25
3	7B-22	F20	E29
3	7B-24	F22	D30
3	7B-26	E22	E28
3	7B-28	E19	D29
3	7B-30	E20	C30
3	7A-30	D22	F26
3	7A-28	D21	E27
3	GNDIO3	GND	GND
3	7A-26	D20	D28
3	7A-24	C22	F25
3	7A-22	C18	C29
3	7A-20	C19	B30
3	7A-18	D17	D27
3	7A-16	C21	E25
3	7A-14	NC	D26
3	7A-12	NC	C27
3	GNDIO3	GND	GND
3	7A-10	NC	B28
3	7A-8	NC	A29
3	7A-6	B22	F23
3	7A-4	D18	C26
3	7A-2	B20	B27
3	7A-0	F17	A28
3	7D-0	B19	A27
3	7D-2	C17	B26

Bank No.	Signal	484 fpBGA	676 fpBGA
3	GNDIO3	GND	GND
3	7D-4	A21	E23
3	7D-6	D15	D24
3	7D-8	A20	C25
3	7D-10	C16	A26
3	7D-12	A19	B25
3	7D-14	F16	C24
3	7D-16	B16	A25
3	7D-18	D14	B24
3	7D-20	A18	C23
3	7D-22	F15	D22
3	7D-24	A17	A24
3	7D-26	B15	E21
3	GNDIO3	GND	GND
3	7D-28	A16	B23
3	7D-30	F14	C22
3	7C-0	C15	A23
3	7C-2	D13	B22
3	7C-4	E15	C21
3	7C-6	F13	A22
3	7C-8	B14	D20
3	7C-10	E13	B21
3	7C-12/VREF3	A15	E19
3	7C-14	D12	C20
3	7C-16	A14	A21
3	7C-18	B13	B20
3	GNDIO3	GND	GND
3	7C-20	A13	A20
3	7C-22	B12	C19
3	7C-24	C13	B19
3	7C-26	A12	A19
3	7C-28	C12	B18
3	7C-30	A11	A18
—	GCLK0	P6	R5
—	GCLK1	R6	T6
—	GCLK2	P17	R25
—	GCLK3	P19	P26
—	GOE0	R18	T26
—	GOE1	R17	R26
—	RESETB	R19	T25
—	TCK	R3	U5
—	TDI	R2	T5
—	TDO	R4	V5

Part Number Description



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Ordering Information

Commercial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-5F484C	fpBGA	484	1024	5	3.3
LC51024VG-75F484C	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484C	fpBGA	484	1024	10	3.3
LC51024VG-5F676C	fpBGA	676	1024	5	3.3
LC51024VG-75F676C	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676C	fpBGA	676	1024	10	3.3
LC5768VG-5F256C	fpBGA	256	768	5	3.3
LC5768VG-75F256C	fpBGA	256	768	7.5	3.3
LC5768VG-10F256C	fpBGA	256	768	10	3.3
LC5768VG-5F484C	fpBGA	484	768	5	3.3
LC5768VG-75F484C	fpBGA	484	768	7.5	3.3
LC5768VG-10F484C	fpBGA	484	768	10	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).

Industrial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-75F484I	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484I	fpBGA	484	1024	10	3.3
LC51024VG-12F484I	fpBGA	484	1024	12	3.3
LC51024VG-75F676I	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676I	fpBGA	676	1024	10	3.3
LC51024VG-12F676I	fpBGA	676	1024	12	3.3
LC5768VG-75F256I	fpBGA	256	768	7.5	3.3
LC5768VG-10F256I	fpBGA	256	768	10	3.3
LC5768VG-12F256I	fpBGA	256	768	12	3.3
LC5768VG-75F484I	fpBGA	484	768	7.5	3.3
LC5768VG-10F484I	fpBGA	484	768	10	3.3
LC5768VG-12F484I	fpBGA	484	768	12	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 5000VG family:

- *ispMACH 5000VG sysIO Design and Usage Guidelines* (TN1000)
- *ispMACH 5000VG Timing Model Design and Usage Guidelines* (TN1001)
- *Power Estimation in ispMACH 5000VG Devices* (TN1002)
- *ispMACH 5000VG PLL Usage Guidelines* (TN1003)