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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	304
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768vg-10f484c

Enhanced Dual-OR Array

To facilitate logic functions requiring a very large number of product terms, the ispMACH 5000VG architecture has been enhanced with an innovative product term expander capability. This capability is embedded in the Dual-OR Array. The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the GLB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate.

The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 5 is a graphical representation of the Enhanced Dual-OR Array.

Figure 5. Enhanced Dual-OR Array

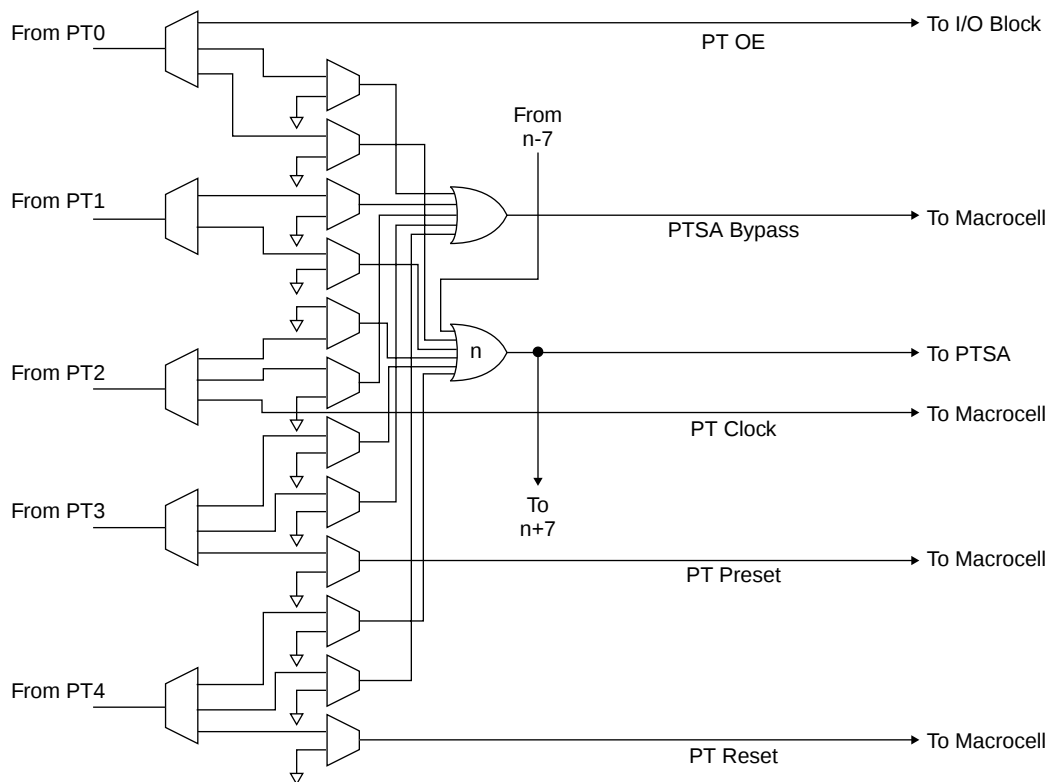
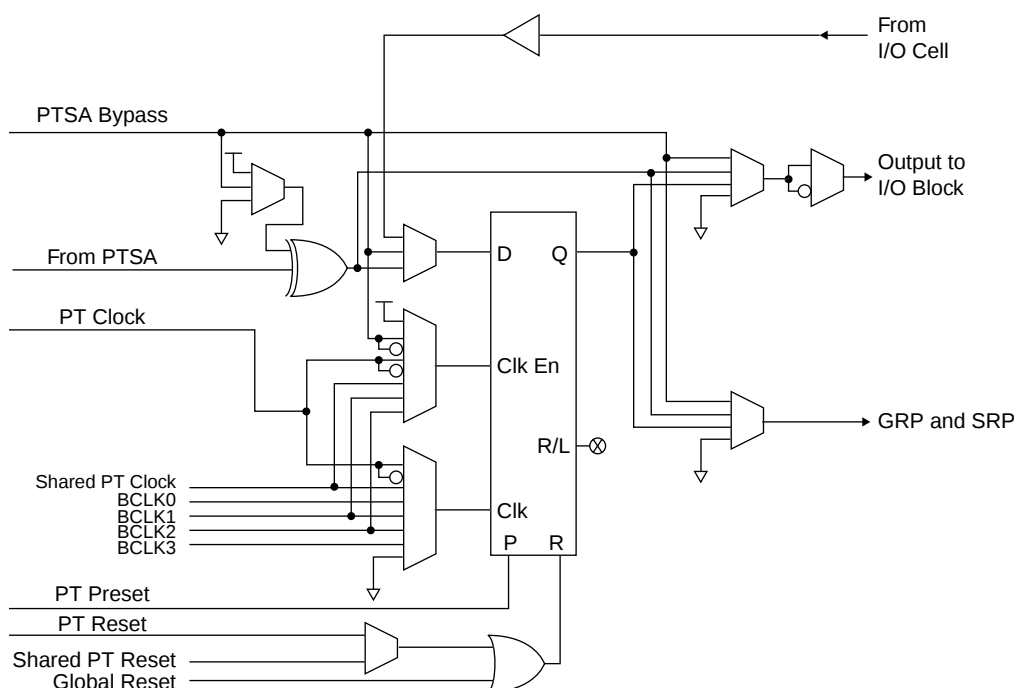


Figure 7. Macrocell

I/O Cell

The I/O cell of the ispMACH 5000VG device provides a high degree of flexibility. It includes the sysIO feature and an enhanced output enable MUX for optimal performance both on- and off-chip. The sysIO feature allows I/O cells to be configured to different I/O standards, drive strengths and slew rates. The enhanced output enable MUX provides up to 14 different output enable choices per I/O cell.

The I/O cell contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. The I/O cell receives its input from its associated macrocell. The I/O cell has a feedback line to its associated macrocell and a direct path to the GRP and SRP.

The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four Shared PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes.

The four shared PTOE signals are derived from PT163 of each GLB in the segment. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 8 is a graphical representation of the I/O cell.

Absolute Maximum Ratings^{1, 2, 3}

Supply Voltage (V_{CC}) -0.5 to 5.4V

PLL Supply Voltage (V_{CCP}) -0.5 to 5.4V

Output Supply Voltage (V_{CCO}) -0.5 to 5.4V

Input Voltage Applied⁴ -0.5 to 5.6V

Tri-state Output Voltage Applied -0.5 to 5.6V

Storage Temperature -65 to 150°C

Junction Temperature (T_j) with Power Applied -55 to 130°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of < 20ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE1149.1 Test Access Port	1.65	3.6	V
T_j (Commercial)	Junction Commercial Operation	0	90	C
T_j (Industrial)	Junction Industrial Operation	-40	105	C

Note: V_{CCJ} must be set in appropriate range to be compatible with desired LVCMOS standard.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1000	—	Cycles

Hot Socketing Characteristics^{1,2,3}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	—	—	+/-100	μA
		V_{IH} (MAX) $\leq V_{IN} \leq 5.5V$	—	—	+/-100	μA

1. Insensitive to sequence of V_{CC} and V_{CCO} . However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO} .
2. LVTTTL, LVCMOS only
3. $0 < V_{CC} \leq V_{CC}$ (MAX), $0 < V_{CCO} \leq V_{CCO}$ (MAX)

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I _{IL} , I _{IH} ¹	Input or I/O Leakage Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	+/-10	μA
I _{PU} ²	I/O Weak Pull-up Resistor Current	V _{CCO} = 3.3	-30	—	-150	μA
		V _{CCO} = 2.5	-20	—	-150	μA
		V _{CCO} = 1.8	-10	—	-150	μA
I _{PD} ²	I/O Weak Pull-down Resistor Current	V _{IL} (MAX) ≤ V _{IN} ≤ V _{IH} (MAX)	30	—	150	μA
I _{BHLS} ²	Bus Hold Low Sustaining Current	V _{IN} = V _{IL} (MAX)	30	—	—	μA
I _{BHHS} ²	Bus Hold High Sustaining Current	V _{CCO} = 3.3	-30	—	—	μA
		V _{CCO} = 2.5	-20	—	—	μA
		V _{CCO} = 1.8	-10	—	—	μA
I _{BHLO} ²	Bus Hold Low Overdrive Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	150	μA
I _{BHHO} ²	Bus Hold High Overdrive Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	-150	μA
I _{CC} ^{3, 4, 5}	Operating Power Supply Current	V _{CC} = 3.3V	—	380	—	mA
V _{BHT}	Bus Hold Trip Points		V _{IL} (MAX)	—	V _{IH} (MIN)	V
C ₁	I/O Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5				
C ₂	Clock Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5				
C ₃	Global Input Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5				

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. Only available for LVCMOS and LVTTL standards.

3. $T_A = 25^\circ C$, $f = 1.0MHz$.

4. Device configured with 16-bit counters.

5. I_{CC} varies with specific device configuration and operating frequency.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}^2 (mA)	I_{OH}^2 (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3 ¹	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCO} - 0.4$	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCO}$	$0.65V_{CCO}$	3.6	0.4	$V_{CCO} - 0.4$	12, 8, 5.33, 4	-12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
PCI 3.3	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
PCI-X	-0.3	$0.35V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
AGP-1X	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
SSTL3 class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCO} - 1.1$	8	-8
SSTL3 class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCO} - 0.9$	16	-16
SSTL2 class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCO} - 0.62$	7.6	-7.6
SSTL2 class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCO} - 0.43$	15.2	-15.2
CTT 3.3	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
CTT 2.5	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
HSTL class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
GTL+	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.6	n/a	36	n/a

1. Software default setting

2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed 96mA.

sysIO Differential Input DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max
$V_{INP} \cdot V_{INM}$	LVDS Input voltage	—	0	2.4
V_{THD}	LVDS Differential input threshold	—	$\pm 100\text{mV}$	—
V_{IL}	LVPECL Input Voltage Low	$V_{CC} = 3.0$ to 3.6V	$V_{CC} - 1.81$	$V_{CC} - 1.48$
		$V_{CC} = 3.3\text{V}$	1.49V	1.83V
V_{IH}	LVPECL Input Voltage High	$V_{CC} = 3.0$ to 3.6V	$V_{CC} - 1.17$	$V_{CC} - 0.88$
		$V_{CC} = 3.3\text{V}$	2.14V	2.42V

ispMACH 51024VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1,2,3}	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}^4	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
$f_{MAX} (Ext.)$	Clock frequency with external feedback, $1/(t_{S_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
$f_{MAX} (Tog.)$	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.10

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 5768VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t _{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t _{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t _{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t _{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t _{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t _{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t _{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t _{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t _{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t _{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t _{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t _{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t _{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
t _{PLL_SEC_DELAY}	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t _{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t _S	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t _{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t _H	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t _{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t _{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns
t _{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t _{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t _{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t _{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t _{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t _{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t _{SRI}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t _{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t _{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t _{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns

ispMACH 51024VG Internal Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns
t_{BSR}	Block PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t_{SPTOE}	Segment PT OE Delay	—	2.40	—	3.60	—	7.75	—	9.10	ns
t_{PTOE}	Macrocell PT OE Delay	—	1.40	—	2.10	—	1.75	—	2.10	ns

Notes:

Timing v.1.1.10

1. Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details.
2. t_{PLL_DELAY} is the unit increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to 3.5ns in either direction in units of 0.5ns for each step.

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
LVC MOS18_12mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 1.8V & 12mA Buffer	—	1.35	—	1.35	—	1.35	—	1.35	ns
LVC MOS25_4mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVC MOS25_5mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVC MOS25_8mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 8mA Buffer	—	0.70	—	0.70	—	0.70	—	0.70	ns
LVC MOS25_12mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 12mA Buffer	—	0.50	—	0.50	—	0.50	—	0.50	ns
LVC MOS25_16mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 2.5V & 16mA Buffer	—	0.25	—	0.25	—	0.25	—	0.25	ns
LVC MOS33_4mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVC MOS33_5mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVC MOS33_8mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 8mA Buffer	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVC MOS33_12mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 12mA Buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVC MOS33_16mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 16mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVC MOS33_20mA_out	t_{BUF} , t_{EN} , t_{DIS}	Output configured as 3.3V & 20mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{BUF} , t_{EN} , t_{DIS}	Output configured as LVTTL Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
Slow Slew	t_{BUF} , t_{EN}	Output configured for slow slew rate	—	1.50	—	1.50	—	1.50	—	1.50	ns
PCI_out	t_{BUF} , t_{EN} , t_{DIS}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_out	t_{BUF} , t_{EN} , t_{DIS}	Using PCI-X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_out	t_{BUF} , t_{EN} , t_{DIS}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL3_I standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
SSTL3_II_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL3_II standard	—	-0.35	—	-0.35	—	-0.35	—	-0.35	ns
SSTL2_I_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF} , t_{EN} , t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF} , t_{EN} , t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF} , t_{EN} , t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF} , t_{EN} , t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns

Note: Open drain timing is the same as corresponding LVC MOS timing.

Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
HSTL_III_out	t_{BUF} , t_{EN} , t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF} , t_{EN} , t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 51024VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{OI} Input Adders											
LVCMOS18_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

ispMACH 51024VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
SSTL2_I_out	t_{BUF} t_{EN} , t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF} t_{EN} , t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF} t_{EN} , t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF} t_{EN} , t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF} t_{EN} , t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns
HSTL_III_out	t_{BUF} t_{EN} , t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF} t_{EN} , t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

sysCLOCK PLL Timing

Over Recommended Operating Conditions¹

Symbol	Parameter	Conditions	Min	Max	Units
t_R, t_F	Input clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, period jitter (peak) ¹	—	—	+/- 200	ps
t_{PWH}	Input clock, high time	—	1.6	—	ns
t_{PWL}	Input clock, low time	—	1.6	—	ns
f_{MDIVIN}	M Divider input, frequency range	—	5	180	MHz
$f_{MDIVOUT}$	M Divider output, frequency range	—	5	180	MHz
f_{VDIVIN}	V Divider input, frequency range	—	60	200	MHz
$f_{VDIVOUT}$	V Divider output, frequency range	—	5	180	MHz
$t_{OUTDUTY}$	Output clock, duty cycle	—	40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean Reference, $5\text{MHz} \leq f_{MDIVOUT} < 80\text{MHz}$	—	+/- 200	ps
		Clean Reference, $80\text{MHz} \leq f_{MDIVOUT} \leq 180\text{MHz}$	—	+/- 100	ps
$t_{JIT(\phi)}$	Output clock, accumulated phase jitter (peak) ²	Clean Reference, $5\text{MHz} \leq f_{MDIVOUT} < 80\text{MHz}$	—	+/- 200	ps
		Clean Reference, $80\text{MHz} \leq f_{MDIVOUT} \leq 180\text{MHz}$	—	+/- 100	ps
$t_{CLK_OUT_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	1	ns
t_ϕ	Input clock to external feedback delta	External feedback	—	500	ps
t_{LOCK}	Time to acquire phase lock after input stable	—	—	30	μs
t_{PLL_DELAY}	Delay increment	—	+/- 0.35	+/- 0.65	ns
t_{RANGE}	Total output delay range	—	+/- 2.45	+/- 4.55	ns
t_{PLL_RSTR}	Reset recovery time of the M-divider	—	11.0	—	ns
t_{PLL_RSTW}	Minimum reset pulse width	—	6.0	—	ns

1. This condition assures that the output phase jitter ($t_{JIT(\phi)}$) will remain within specification.

2. Accumulated jitter measured over 10,000 waveform samples.

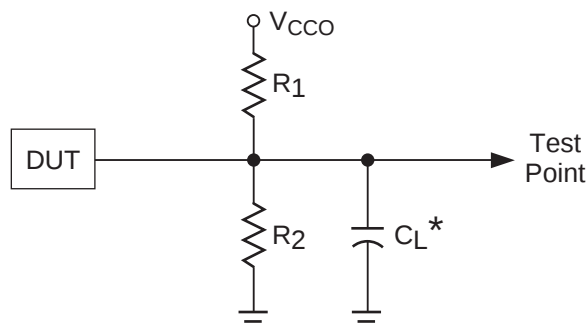
Boundary Scan Timing Specifications

Symbol	Parameter	Min.	Max.	Units
t_{BTCP}	TCK [BSCAN test] clock cycle	40	—	ns
t_{BTCH}	TCK [BSCAN test] pulse width high	20	—	ns
t_{BTCL}	TCK [BSCAN test] pulse width low	20	—	ns
t_{BTSU}	TCK [BSCAN test] setup time	8	—	ns
t_{BTH}	TCK [BSCAN test] hold time	10	—	ns
t_{BRF}	TCK [BSCAN test] rise and fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
t_{BTOZ}	TAP controller falling edge of clock to data output disable	—	10	ns
t_{BTVO}	TAP controller falling edge of clock to data output enable	—	10	ns
$t_{BVTCPUSU}$	BSCAN test Capture register setup time	8	—	ns
t_{BTCPH}	BSCAN test Capture register hold time	10	—	ns
t_{BTUCO}	BSCAN test Update reg, falling edge of clock to valid output	—	25	ns
t_{BTUOZ}	BSCAN test Update reg, falling edge of clock to output disable	—	25	ns
t_{BTUOV}	BSCAN test Update reg, falling edge of clock to output enable	—	25	ns

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.

Figure 12. Output Test Load, LVTTTL and LVCMOS Standards



* C_L includes Test Fixture and Probe Capacitance.

0213A/ispM5kvg

Table 3. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 3.3 I/O (L -> H, H -> L)	110	110	35pF	1.5	3.0V
Other LVCMOS Settings, (L -> H, H -> L)	∞	∞	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = $V_{CCO}/2$	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = $V_{CCO}/2$	LVCMOS 1.8 = 1.65V
Default LVCMOS 3.3 I/O (Z -> H)	∞	110	35pF	1.5V	3.0V
Default LVCMOS 3.3 I/O (Z -> L)	110	∞	35pF	1.5V	3.0V
Default LVCMOS 3.3 I/O (H -> Z)	∞	110	5pF	$V_{OH} - 0.3$	3.0V
Default LVCMOS 3.3 I/O (L -> Z)	110	∞	5pF	$V_{OL} + 0.3$	3.0V

Output test conditions for all other interfaces are determined by the respective standards. For further details, please refer to the following technical note:

- *ispMACH 5000VG sysIO Design and Usage Guidelines (TN1000)*

ispMACH 5768VG Logic Signal Connections

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0C-30	C8	D11
0	0C-28	B6	B11
0	0C-26	A5	E12
0	0C-24	D8	C11
0	0C-22	E8	F12
0	0C-20	B5	B10
0	GNDIO0	GND	GND
0	0C-18	A4	A10
0	0C-16	D7	D10
0	0C-14/VREF0	E7	A9
0	0C-12	C6	E11
0	0C-10	B4	B9
0	0C-8	A3	F11
0	0C-6	NC	A8
0	0C-4	NC	C10
0	0C-2	NC	A7
0	0C-0	NC	E10
0	0D-30	NC	B8
0	0D-28	NC	C8
0	GNDIO0	GND	GND
0	0D-26	NC	F10
0	0D-24	NC	A6
0	0D-22	NC	F9
0	0D-20	NC	C7
0	0D-18	NC	D9
0	0D-16	NC	B7
0	0D-14	D6	E8
0	0D-12	E6	A5
0	0D-10	A2	F8
0	0D-8	B3	C6
0	0D-6	C4	D8
0	0D-4	D5	A3
0	GNDIO0	GND	GND
0	0D-2	NC	A2
0	0D-0	NC	A4
0	0A-0	NC	F7
0	0A-2	NC	C5
0	0A-4	NC	F6
0	0A-6	NC	B3
0	0A-8	NC	NC
0	0A-10	NC	NC
0	GNDIO0	GND	GND
0	0A-12	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0A-14	NC	NC
0	0A-16	NC	B4
0	0A-18	NC	D5
0	0A-20	NC	B1
0	0A-22	NC	D6
0	0A-24	NC	C4
0	0A-26	NC	E4
0	GNDIO0	GND	GND
0	0A-28	B2	C2
0	0A-30	B1	C1
0	0B-30	C2	D1
0	0B-28	C1	D2
0	0B-26	NC	D3
0	0B-24	NC	E1
0	0B-22	NC	E3
0	0B-20	NC	F4
0	0B-18	NC	F1
0	0B-16	NC	F3
0	0B-14	NC	G6
0	0B-12	NC	G1
0	GNDIO0	GND	GND
0	0B-10	NC	G2
0	0B-8	NC	H1
0	0B-6	NC	G3
0	0B-4	NC	H2
0	0B-2	NC	H5
0	0B-0	NC	H6
0	1A-0	F7	J1
0	1A-2	F6	K1
0	1A-4	E5	H3
0	1A-6	D4	J2
0	1A-8	D3	H4
0	1A-10	D2	K2
0	GNDIO0	GND	GND
0	1A-12	D1	J6
0	1A-14	E4	L1
0	1A-16	NC	K3
0	1A-18	NC	J4
0	1A-20	NC	L2
0	1A-22	NC	M1
0	1A-24	NC	K6
0	1A-26	NC	K4
0	1A-28	NC	L3

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
0	1A-30	NC	K5
0	GNDIO0	GND	GND
0	1B-30/CLK_OUT0	G6	N1
0	1B-28	NC	M2
0	1B-26	NC	P1
0	1B-24	NC	L4
0	1B-22	F5	N2
0	1B-20	E2	M3
0	1B-18	E1	L5
0	1B-16	F4	R1
0	1B-14	F3	P2
0	1B-12	F2	N3
0	GNDIO0	GND	GND
0	1B-10	G5	M6
0	1B-8	G4	M5
0	1B-6/PLL_RST0	F1	M4
0	1B-4/PLL_FBK0	G2	N4
0	1B-2	G1	N6
0	1B-0	H5	N5
1	2B-0	K1	R5
1	2B-2	K2	T2
1	2B-4	L1	T5
1	2B-6	J5	T3
1	2B-8	L2	U1
1	2B-10	K4	U4
1	GNDIO1	GND	GND
1	2B-12	M1	V1
1	2B-14	L3	U3
1	2B-16	L4	V5
1	2B-18	K5	V2
1	2B-20	M2	W1
1	2B-22	N1	V3
1	2B-24	NC	W2
1	2B-26	K6	Y1
1	2B-28	L5	Y2
1	2B-30	N2	W3
1	2A-30	L6	AA3
1	2A-28	L7	W4
1	GNDIO1	GND	GND
1	2A-26	P1	W5
1	2A-24	P2	Y4
1	2A-22	N3	T6
1	2A-20	R4	Y5

Bank No.	Signal	256 fpBGA	484 fpBGA
1	2A-18	NC	U6
1	2A-16	R1	AA4
1	2A-14	NC	NC
1	2A-12	NC	NC
1	GNDIO1	GND	GND
1	2A-10	NC	NC
1	2A-8	NC	NC
1	2A-6	T1	W6
1	2A-4	T2	V4
1	2A-2	R2	U7
1	2A-0	T3	AB2
1	2D-0	R3	V7
1	2D-2	P4	AA5
1	GNDIO1	GND	GND
1	2D-4	T4	AB3
1	2D-6	N4	Y6
1	2D-8	M4	AB4
1	2D-10	N5	Y7
1	2D-12	R5	AB5
1	2D-14	T5	V8
1	2D-16	NC	AA7
1	2D-18	NC	Y8
1	2D-20	NC	AB6
1	2D-22	T6	W8
1	2D-24	R6	AA8
1	2D-26	P6	Y10
1	GNDIO1	GND	GND
1	2D-28	M5	U8
1	2D-30	T7	AB7
1	2C-0	T8	U9
1	2C-2	R8	AA9
1	2C-4	M6	W9
1	2C-6	N6	AB8
1	2C-8	R7	U10
1	2C-10	T9	AB9
1	2C-12	T10	V11
1	2C-14/VREF1	M7	AA10
1	2C-16	N7	V10
1	2C-18	P8	AB10
1	GNDIO1	GND	GND
1	2C-20	R9	W10
1	2C-22	N8	W11
1	2C-24	M8	U11

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
1	2C-26	T11	AA11
1	2C-28	T12	V12
1	2C-30	R10	AB11
2	3C-30	P9	W12
2	3C-28	R11	Y11
2	3C-26	T13	Y12
2	3C-24	N9	AB12
2	3C-22	M9	U12
2	3C-20	R12	AA12
2	GNDIO2	GND	GND
2	3C-18	P11	Y13
2	3C-16	N10	AB13
2	3C-14	M10	W13
2	3C-12/VREF2	R13	AA13
2	3C-10	T14	U13
2	3C-8	R14	AB14
2	3C-6	M11	V13
2	3C-4	N11	AA14
2	3C-2	P13	U14
2	3C-0	T15	AB15
2	3D-30	T16	Y15
2	3D-28	N12	AB16
2	GNDIO2	GND	GND
2	3D-26	NC	AA15
2	3D-24	NC	W14
2	3D-22	NC	AB17
2	3D-20	NC	Y16
2	3D-18	NC	AA16
2	3D-16	NC	Y17
2	3D-14	NC	AB18
2	3D-12	NC	V15
2	3D-10	NC	AB19
2	3D-8	NC	W15
2	3D-6	NC	AB20
2	3D-4	NC	AA18
2	GNDIO2	GND	GND
2	3D-2	L10	U15
2	3D-0	L11	W17
2	3A-0	K11	U16
2	3A-2	R15	AA19
2	3A-4	NC	V16
2	3A-6	NC	AB21
2	3A-8	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
2	3A-10	NC	NC
2	GNDIO2	GND	GND
2	3A-12	NC	NC
2	3A-14	NC	NC
2	3A-16	NC	Y18
2	3A-18	P15	W18
2	3A-20	R16	AA20
2	3A-22	P16	W19
2	3A-24	N14	Y19
2	3A-26	N13	V19
2	GNDIO2	GND	GND
2	3A-28	N15	Y21
2	3A-30	N16	W20
2	3B-30	M16	AA22
2	3B-28	M12	W21
2	3B-26	NC	Y22
2	3B-24	NC	V20
2	3B-22	M13	V21
2	3B-20	M15	W22
2	3B-18	L16	V18
2	3B-16	L15	U20
2	3B-14	L13	V22
2	3B-12	L14	U19
2	GNDIO2	GND	GND
2	3B-10	L12	U17
2	3B-8	K13	U22
2	3B-6	K15	T20
2	3B-4	K16	T21
2	3B-2	J16	T17
2	3B-0	K12	R20
3	4B-0	J12	R21
3	4B-2	G16	T22
3	4B-4/PLL_FBK1	G15	P21
3	4B-6/PLL_RST1	H12	N20
3	4B-8	G12	R22
3	4B-10	G13	N21
3	GNDIO3	GND	GND
3	4B-12	F16	M18
3	4B-14	F15	N19
3	4B-16	F13	P22
3	4B-18	F14	M20
3	4B-20	F12	N22
3	4B-22	E16	N17

ispMACH 51024VG Logic Signal Connections

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0C-30	D11	A13
0	0C-28	B11	B13
0	0C-26	E12	A12
0	0C-24	C11	B12
0	0C-22	F12	C12
0	0C-20	B10	A11
0	GNDIO0	GND	GND
0	0C-18	A10	B11
0	0C-16	D10	A10
0	0C-14/VREF0	A9	C11
0	0C-12	E11	E12
0	0C-10	B9	B10
0	0C-8	F11	D11
0	0C-6	A8	A9
0	0C-4	C10	C10
0	0C-2	A7	B9
0	0C-0	E10	A8
0	0D-30	B8	C9
0	0D-28	C8	B8
0	GNDIO0	GND	GND
0	0D-26	F10	E10
0	0D-24	A6	A7
0	0D-22	F9	D9
0	0D-20	C7	C8
0	0D-18	D9	B7
0	0D-16	B7	A6
0	0D-14	E8	C7
0	0D-12	A5	B6
0	0D-10	F8	A5
0	0D-8	C6	C6
0	0D-6	D8	D7
0	0D-4	A3	E8
0	GNDIO0	GND	GND
0	0D-2	A2	B5
0	0D-0	A4	A4
0	0A-0	F7	A3
0	0A-2	C5	B4
0	0A-4	F6	C5
0	0A-6	B3	F8
0	0A-8	NC	A2
0	0A-10	NC	B3
0	GNDIO0	GND	GND
0	0A-12	NC	C4

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0A-14	NC	D5
0	0A-16	B4	E6
0	0A-18	D5	D4
0	0A-20	B1	B1
0	0A-22	D6	C2
0	0A-24	C4	F6
0	0A-26	E4	D3
0	GNDIO0	GND	GND
0	0A-28	C2	E4
0	0A-30	C1	F5
0	0B-30	D1	C1
0	0B-28	D2	D2
0	0B-26	D3	E3
0	0B-24	E1	D1
0	0B-22	E3	E2
0	0B-20	F4	H6
0	0B-18	F1	F3
0	0B-16	F3	E1
0	0B-14	G6	G4
0	0B-12	G1	F2
0	GNDIO0	GND	GND
0	0B-10	G2	H5
0	0B-8	H1	G3
0	0B-6	G3	F1
0	0B-4	H2	G2
0	0B-2	H5	H3
0	0B-0	H6	G1
0	1A-0	J1	H2
0	1A-2	K1	J4
0	1A-4	H3	H1
0	1A-6	J2	J3
0	1A-8	H4	K5
0	1A-10	K2	J2
0	GNDIO0	GND	GND
0	1A-12	J6	J1
0	1A-14	L1	K3
0	1A-16	K3	K2
0	1A-18	J4	K1
0	1A-20	L2	L4
0	1A-22	M1	L3
0	1A-24	K6	L2
0	1A-26	K4	M5
0	1A-28	L3	L1

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
3	6A-10	K21	J29
3	6A-8	K18	K26
3	6A-6	J17	J28
3	6A-4	J19	H30
3	6A-2	J22	J27
3	6A-0	J21	H29
3	7B-0	H19	G30
3	7B-2	H20	H28
3	7B-4	H17	G29
3	7B-6	H18	F30
3	7B-8	H22	G28
3	7B-10	H21	H26
3	GNDIO3	GND	GND
3	7B-12	G20	F29
3	7B-14	G22	G27
3	7B-16	G17	E30
3	7B-18	G21	F28
3	7B-20	F19	H25
3	7B-22	F20	E29
3	7B-24	F22	D30
3	7B-26	E22	E28
3	7B-28	E19	D29
3	7B-30	E20	C30
3	7A-30	D22	F26
3	7A-28	D21	E27
3	GNDIO3	GND	GND
3	7A-26	D20	D28
3	7A-24	C22	F25
3	7A-22	C18	C29
3	7A-20	C19	B30
3	7A-18	D17	D27
3	7A-16	C21	E25
3	7A-14	NC	D26
3	7A-12	NC	C27
3	GNDIO3	GND	GND
3	7A-10	NC	B28
3	7A-8	NC	A29
3	7A-6	B22	F23
3	7A-4	D18	C26
3	7A-2	B20	B27
3	7A-0	F17	A28
3	7D-0	B19	A27
3	7D-2	C17	B26

Bank No.	Signal	484 fpBGA	676 fpBGA
3	GNDIO3	GND	GND
3	7D-4	A21	E23
3	7D-6	D15	D24
3	7D-8	A20	C25
3	7D-10	C16	A26
3	7D-12	A19	B25
3	7D-14	F16	C24
3	7D-16	B16	A25
3	7D-18	D14	B24
3	7D-20	A18	C23
3	7D-22	F15	D22
3	7D-24	A17	A24
3	7D-26	B15	E21
3	GNDIO3	GND	GND
3	7D-28	A16	B23
3	7D-30	F14	C22
3	7C-0	C15	A23
3	7C-2	D13	B22
3	7C-4	E15	C21
3	7C-6	F13	A22
3	7C-8	B14	D20
3	7C-10	E13	B21
3	7C-12/VREF3	A15	E19
3	7C-14	D12	C20
3	7C-16	A14	A21
3	7C-18	B13	B20
3	GNDIO3	GND	GND
3	7C-20	A13	A20
3	7C-22	B12	C19
3	7C-24	C13	B19
3	7C-26	A12	A19
3	7C-28	C12	B18
3	7C-30	A11	A18
—	GCLK0	P6	R5
—	GCLK1	R6	T6
—	GCLK2	P17	R25
—	GCLK3	P19	P26
—	GOE0	R18	T26
—	GOE1	R17	R26
—	RESETB	R19	T25
—	TCK	R3	U5
—	TDI	R2	T5
—	TDO	R4	V5

Signal Configuration

ispMACH 5768VG 256-ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF3	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	I/O	I/O	I/O	I/O	I/O/ CLK_OUT1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	B
C	I/O	I/O	VCCO3	I/O	GND	I/O	VCCO3	I/O	I/O	VCCO0	I/O	GND	I/O	VCCO0	I/O	I/O	C
D	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	D
E	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF0	I/O	I/O	I/O	GND	I/O	I/O	E
F	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ PLL_RST0	F
G	I/O	I/O/ PLL_FBK1	VCCO3	I/O	I/O	I/O	GND	GND	GND	GND	I/O/ CLK_OUT0	I/O	I/O	VCCO0	I/O/ PLL_FBK0	I/O	G
H	VCCP1	GOE1	GCLK2	GCLK3	I/O/ PLL_RST1	VCC	GND	GND	GND	GNDP0	VCC	I/O	GCLK0	TDI	TMS	VCCP0	H
J	I/O	GOE0	RESETB	TOE	I/O	VCC	GNDP1	GND	GND	GND	VCC	I/O	GCLK1	TCK	TDO	VCCJ	J
K	I/O	I/O	VCCO2	I/O	I/O	I/O	GND	GND	GND	GND	I/O	I/O	I/O	VCCO1	I/O	I/O	K
L	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	L
M	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	GND	I/O	I/O	M
N	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	VCCO2	I/O	GND	I/O	VCCO2	I/O	I/O	VCCO1	I/O	GND	I/O	VCCO1	I/O	I/O	P
R	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 5768VG

256fpBGA/5768VG

Bottom View

Note: Ball A1 indicator dot on top side of package.

Industrial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-75F484I	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484I	fpBGA	484	1024	10	3.3
LC51024VG-12F484I	fpBGA	484	1024	12	3.3
LC51024VG-75F676I	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676I	fpBGA	676	1024	10	3.3
LC51024VG-12F676I	fpBGA	676	1024	12	3.3
LC5768VG-75F256I	fpBGA	256	768	7.5	3.3
LC5768VG-10F256I	fpBGA	256	768	10	3.3
LC5768VG-12F256I	fpBGA	256	768	12	3.3
LC5768VG-75F484I	fpBGA	484	768	7.5	3.3
LC5768VG-10F484I	fpBGA	484	768	10	3.3
LC5768VG-12F484I	fpBGA	484	768	12	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 5000VG family:

- *ispMACH 5000VG sysIO Design and Usage Guidelines* (TN1000)
- *ispMACH 5000VG Timing Model Design and Usage Guidelines* (TN1001)
- *Power Estimation in ispMACH 5000VG Devices* (TN1002)
- *ispMACH 5000VG PLL Usage Guidelines* (TN1003)