Lattice Semiconductor Corporation - LC5768VG-5F256C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	196
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768vg-5f256c

The ispMACH5000VG devices also contain sysCLOCK Phase Locked Loops (PLLs) that provide designers with increased clocking flexibility. The PLLs can be used to synthesize new clocks for use on-chip or elsewhere within the system. They can also be used to deskew clocks, again both at the chip and system levels. A variable delay line capability further improves this and allows designers to retard or advance the clock in order to tune set-up and clock-to-out times for optimal results. The ispMACH 5000VG Family Selection Guide (Table 1) details the key attributes and packages for the ispMACH 5000VG devices.

ispMACH 5000VG Architecture

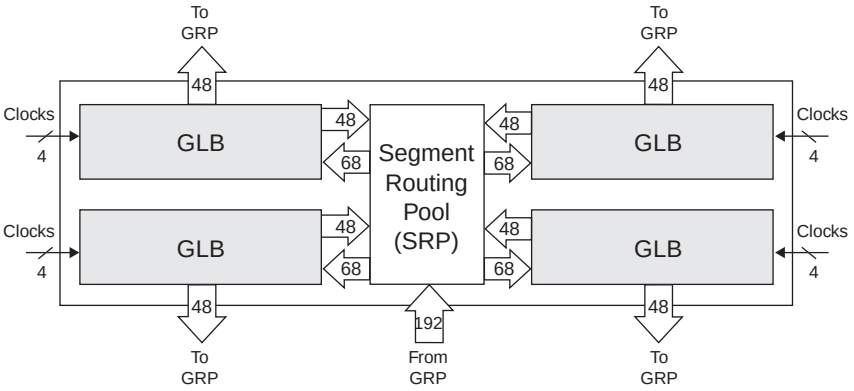
The ispMACH 5000VG Family of In-System Programmable High Density Logic Devices is based on segments containing four Generic Logic Blocks (GLBs) and a hierarchical routing pool (GRP) structure interconnecting the segments. A segment routing pool (SRP) connects each GLB in a segment allowing the maximum flexibility and speed.

Outputs from the GLBs drive the Segment Routing Pool (SRP) and the Global Routing Pool (GRP). Enhanced switching resources are provided to allow signals in the Segment Routing Pool to drive any or all the GLBs in the segment. Optimal switching is provided to allow all signals in the Global Routing Pool to be routed to any or all SRPs. This mechanism allows fast, efficient connections across the entire device.

Segment

Each segment contains four GLBs and a segment routing pool (SRP). Each GLB has 32 internal feedback outputs and 16 external feedback outputs, for a total of 48 outputs from each GLB feeding the SRP. The SRP contains up to 384 signals, 48 from each GLB and 192 from the GRP, with full routing capability. This routing scheme maximizes the flexibility and speed of the device without sacrificing the routing.

Figure 2. Segment



Generic Logic Block

Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and three control product terms. The GLB has 68 inputs from the Segment Routing Pool, which are available in both true and complement form for every product term. The three control product terms are used for shared reset, clock and output enable functions. Figure 3 shows the structure of the GLB from the macrocell perspective. This is referred to as a macrocell slice. There are 32 macrocell slices per GLB.

AND-Array

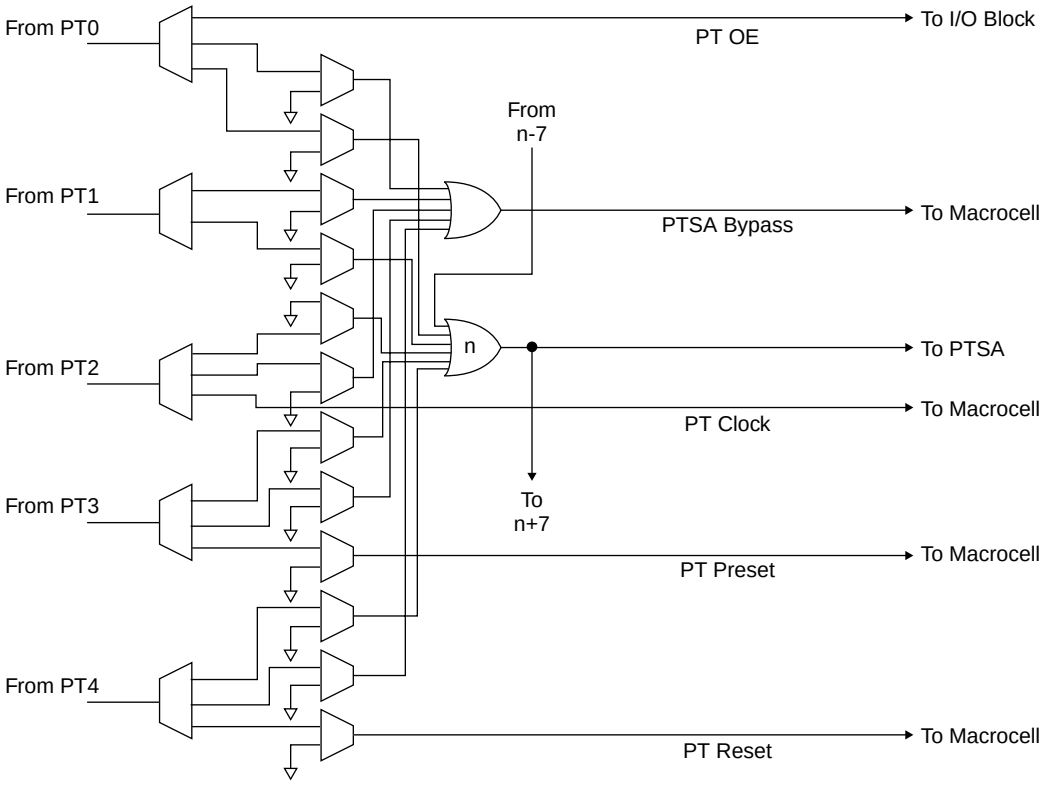
The programmable AND-Array consists of 68 inputs and 163 output product terms. The 68 inputs from the SRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 163 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining three control product terms feeding the Shared PT Clock, Shared PT Reset and Shared PT OE. Every set of five product terms from the 160 logic product terms forms a product term cluster start-

Enhanced Dual-OR Array

To facilitate logic functions requiring a very large number of product terms, the ispMACH 5000VG architecture has been enhanced with an innovative product term expander capability. This capability is embedded in the Dual-OR Array. The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the GLB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate.

The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 5 is a graphical representation of the Enhanced Dual-OR Array.

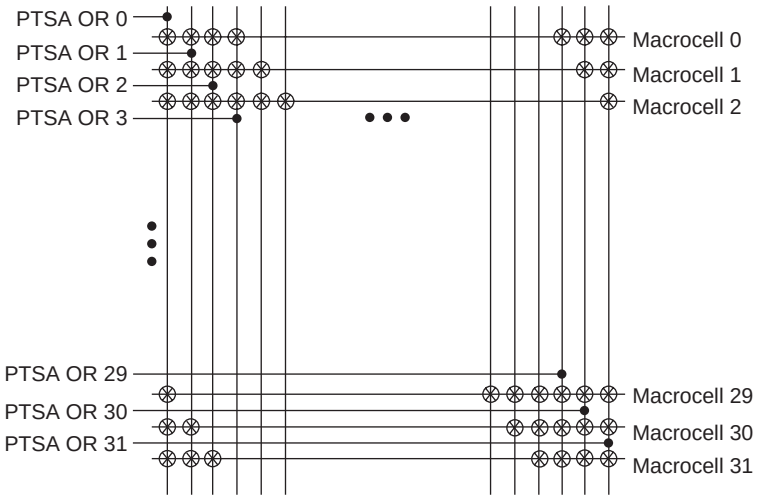
Figure 5. Enhanced Dual-OR Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Figure 6 shows the graphical representation of the PTSA.

Figure 6. Product Term Sharing Array



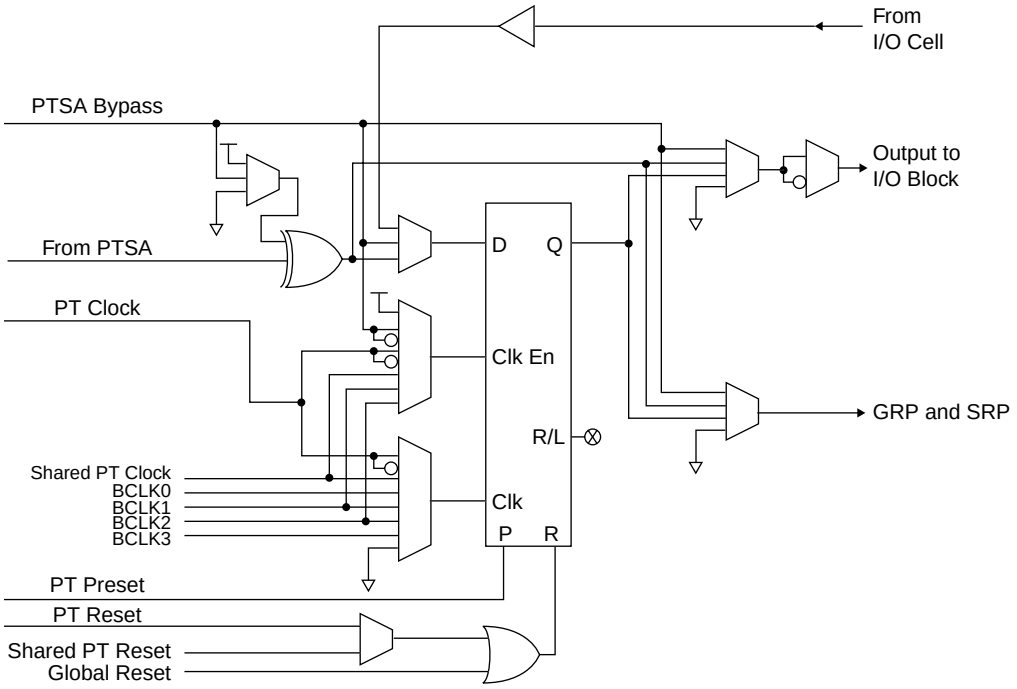
Macrocell

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation.

The macrocells each have two outputs, which can be fed to the SRP, GRP and I/O cell. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 7 is a graphical representation of the ispMACH 5000VG macrocell.

Figure 7. Macrocell



I/O Cell

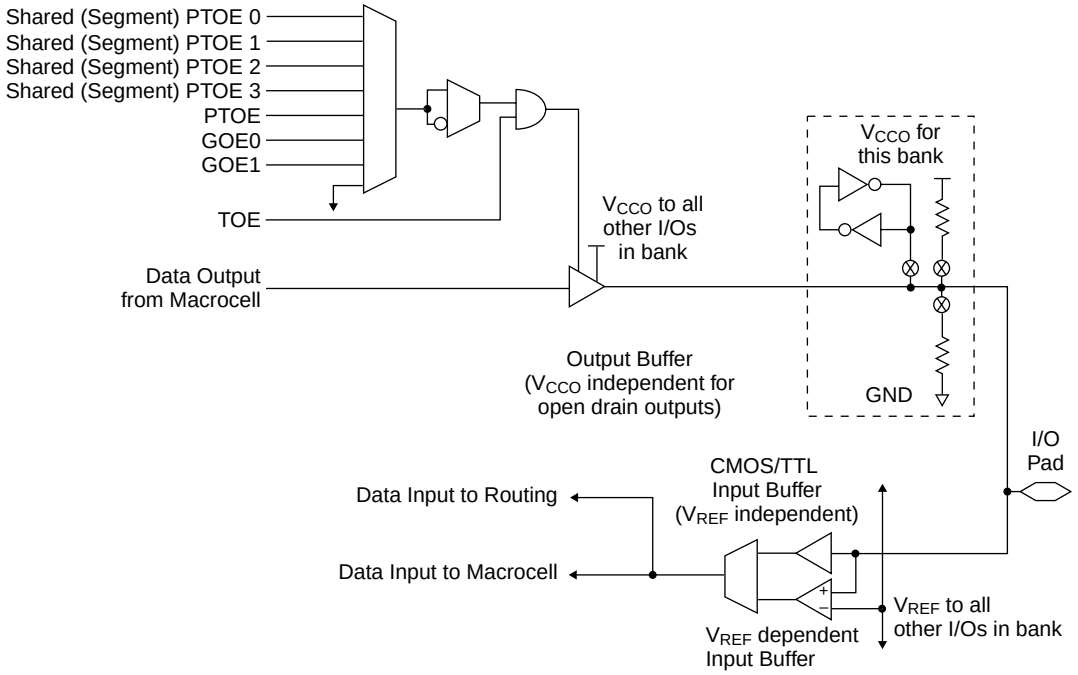
The I/O cell of the ispMACH 5000VG device provides a high degree of flexibility. It includes the sysIO feature and an enhanced output enable MUX for optimal performance both on- and off-chip. The sysIO feature allows I/O cells to be configured to different I/O standards, drive strengths and slew rates. The enhanced output enable MUX provides up to 14 different output enable choices per I/O cell.

The I/O cell contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. The I/O cell receives its input from its associated macrocell. The I/O cell has a feedback line to its associated macrocell and a direct path to the GRP and SRP.

The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four Shared PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes.

The four shared PTOE signals are derived from PT163 of each GLB in the segment. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 8 is a graphical representation of the I/O cell.

Figure 8. I/O Cell



sysIO Capability

The ispMACH 5000VG devices are divided into four sysIO banks, where each bank is capable of supporting 14 different I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Table 2 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

Table 2. ispMACH 5000VG Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3	3.3V	N/A	N/A
PCI-X	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential[1]	N/A	N/A	N/A
LVDS[1]	N/A	N/A	N/A

1. LVDS and LVPECL are only supported on the dedicated clock pins.

Global clock pins have additional capabilities that allow for higher performance applications. Two global clock pins can be paired together to create a single global clock pin that can interface with certain differential signals.

The TOE and JTAG pins of the ispMACH 5000VG device are the only pins that do not have sysIO capabilities. These pins only support the LVTTL and LVCMOS standards.

There are three classes of I/O interface standards that are implemented in the ispMACH 5000VG devices. The first is the unterminated, single-ended interface. It includes the 3.3V LVTTL standard along with the 1.8V, 2.5V and 3.3V LVCMOS interface standards. Additionally, PCI 3.3, PCI-X and AGP-1X are all subsets of this type of interface.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT and GTL+. Usage of these particular I/O interfaces requires the use of an additional VREF signal. At the system level, a termination voltage, VTT, is also required. Typically, an output will be terminated to VTT at the receiving end of the transmission line it is driving.

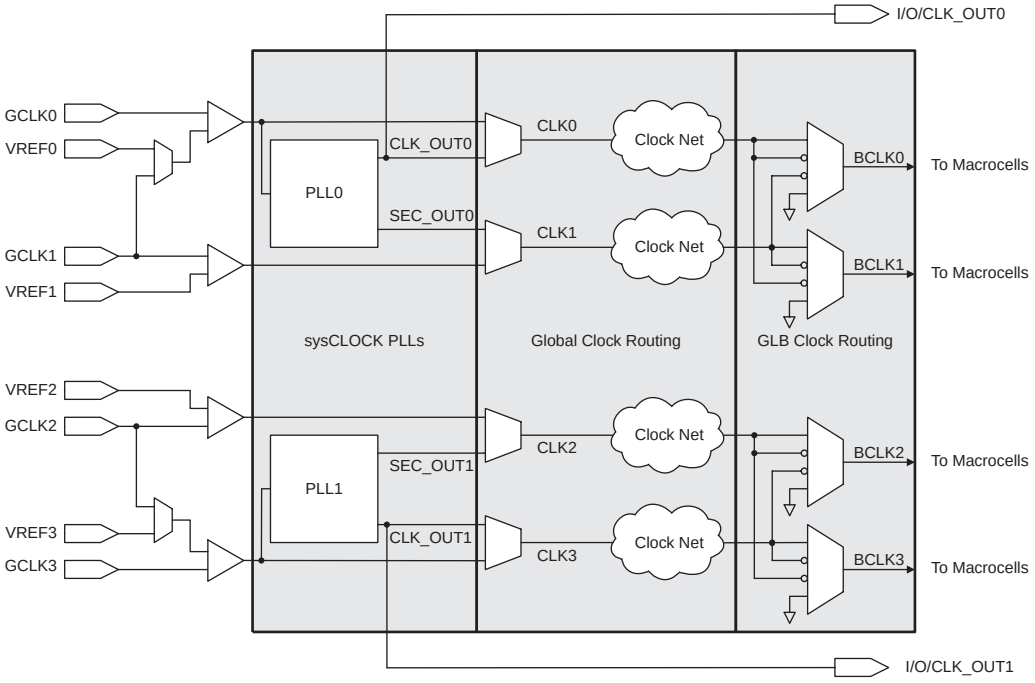
The final types of interfaces implemented are the differential standards LVDS and LVPECL. These interfaces are implemented on clock pins only. When using one of the differential standards, a pair of global clock pins (GCLK0 and GCLK1 or GCLK3 and GCLK2) is combined to create a single clock signal.

For more information on the sysIO capability, please refer to Technical Note TN1000: *ispMACH 5000VG sysIO Design and Usage Guidelines* .

GLB Clock Distribution

The ispMACH 5000VG family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the GLB clock multiplexes which generate the GLB clock signals (BCLK0-BCLK3). The GLB clock multiplexer allows a variety of true and complementary versions of the clocks to be used within the GLB. Each block clock can be the true or inverse of its associated global clock or the inverse of the adjacent global clock. Figure 9 shows the clock distribution network.

Figure 9. Clock Distribution Network



Absolute Maximum Ratings[1, 2, 3]

Supply Voltage (V_{CC}) . . . . . -0.5 to 5.4V

PLL Supply Voltage (V_{CCP}) . . . . . -0.5 to 5.4V

Output Supply Voltage (V_{CCO}) . . . . . -0.5 to 5.4V

Input Voltage Applied[4] . . . . . -0.5 to 5.6V

Tri-state Output Voltage Applied. . . . . -0.5 to 5.6V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature (Tj) with Power Applied . . . . . -55 to 130°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of < 20ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE1149.1 Test Access Port	1.65	3.6	V
Tj (Commercial)	Junction Commercial Operation	0	90	C
Tj (Industrial)	Junction Industrial Operation	-40	105	C

Note: V_{CCJ} must be set in appropriate range to be compatible with desired LVCMOS standard.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1000	—	Cycles

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-100	µA
		V_{IH} (MAX) $\le V_{IN} \le$ 5.5V	—	—	+/-100	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO}.
2. LVTTL, LVCMOS only
3. $0 < V_{CC} \le V_{CC}$ (MAX), $0 < V_{CCO} \le V_{CCO}$ (MAX)

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3[1]	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	16, 12 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCO}$	$0.65V_{CCO}$	3.6	0.4	V_{CCO}-0.4	12, 8, 5.33, 4	-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
PCI-X	-0.3	$0.35V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
AGP-1X	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.7	V_{CCO}-1.1	8	-8
SSTL3 class II	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.5	V_{CCO}-0.9	16	-16
SSTL2 class I	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.54	V_{CCO}-0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.35	V_{CCO}-0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
CTT 2.5	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
HSTL class I	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	8	-8
HSTL class III	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	24	-8
GTL+	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.6	n/a	36	n/a

1. Software default setting
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed 96mA.

sysIO Differential Input DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max
V_{INP} . V_{INM}	LVDS Input voltage	—	0	2.4
V_{THD}	LVDS Differential input threshold	—	±100mV	—
V_{IL}	LVPECL Input Voltage Low	V_{CC} = 3.0 to 3.6V	V_{CC}-1.81	V_{CC}-1.48
		V_{CC} = 3.3V	1.49V	1.83V
V_{IH}	LVPECL Input Voltage High	V_{CC} = 3.0 to 3.6V	V_{CC}-1.17	V_{CC}-0.88
		V_{CC} = 3.3V	2.14V	2.42V

ispMACH 5768VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL\_SEC\_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{H}	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns

ispMACH 5768VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVDS_in	t_{GCLK_IN}	Using LVDS standard	—	1.70	—	1.70	—	1.70	—	1.70	ns
LVPECL_in	t_{GCLK_IN}	Using LVPECL standard	—	2.10	—	2.10	—	2.10	—	2.10	ns
t_{IOO} Output Adders											
LVCMOS18_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 4mA Buffer	—	3.00	—	3.00	—	3.00	—	3.00	ns
LVCMOS18_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 5.33mA Buffer	—	2.50	—	2.50	—	2.50	—	2.50	ns
LVCMOS18_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 8mA Buffer	—	1.85	—	1.85	—	1.85	—	1.85	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
HSTL_III_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF}, t_{EN}, t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.20

ispMACH 51024VG Timing Adders

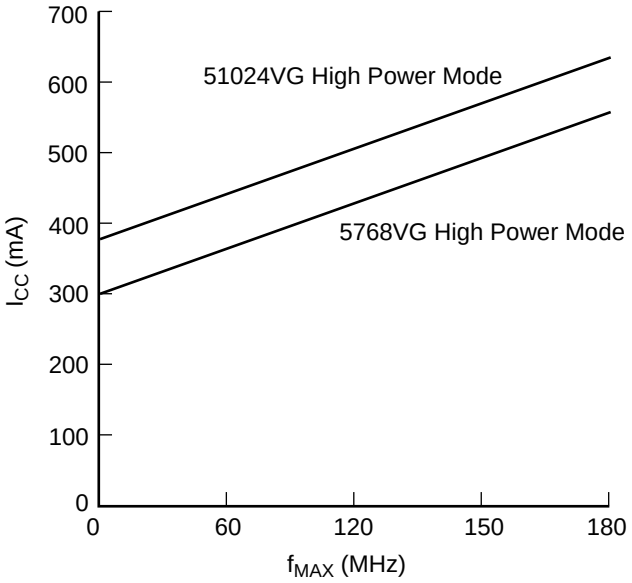
Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{IOI} Input Adders											
LVCMOS18_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN}, t_{GCLK_IN}, t_{RSTb}, t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns

Note: Open drain timing is the same as corresponding LVCMOS timing. Timing v.1.10

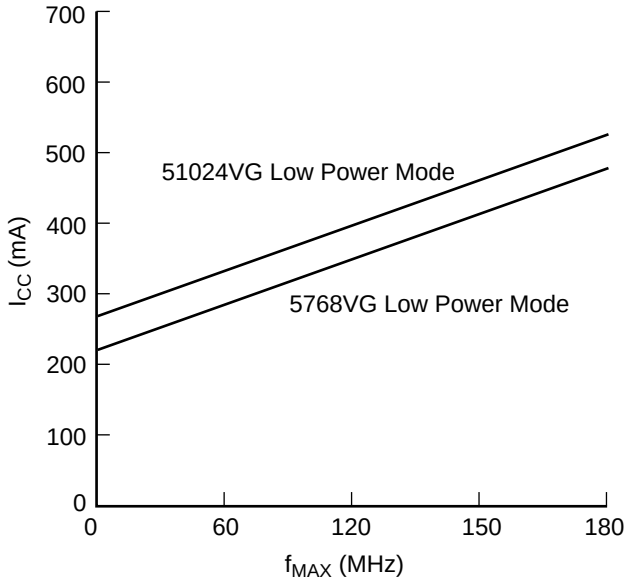
Power Consumption

ispMACH 5000VG Typical Power vs. Frequency

ispMACH 5000VG I_{CC} Curves at High Power Mode



ispMACH 5000VG I_{CC} Curves at Low Power Mode



Note: The devices are configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V, 25° C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	I_{DC} (mA)	I_{DCO} (mA)
ispMACH 5768VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	65	20
ispMACH 51024VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	80	20

Note: For further information about the use of these coefficients, refer to Technical Note TN1002, *Power Estimation in ispMACH 5000VG Devices*.

K0 = average current per product term in high power/MHz
K1 = average current per product term in low power/MHz
K2 = average current per GRP line/MHz
K3 = average current per PLL/MHz
K4 = DC current per product terms in high power
K5 = DC current per product terms in low power
K6 = Static DC current per PLL
I_{DC} = Static device current with all product terms powered off
I_{DCO} = Static I/O bank current

Icc estimates are based on typical conditions (Vcc = 3.3V, room temperature) and an assumption of one GLB load on average exists. These values are for estimates only. Since the value of Icc is sensitive to operating conditions and the program in the device, the actual Icc should be verified.

ispMACH 5768VG Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[2]	484-Ball fpBGA[2]
V_{CC}	F8, F9, H6, H11, J6, J11, L8, L9	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6
V_{CCO0}	C3, C7, G3	B5, D7, E2, E6, E9, F5, G4, J5
V_{CCO1}	K3, P3, P7	P5, U5, V6, V9, Y3
V_{CCO2}	K14, P10, P14	P18, U18, V14, V17, Y20
V_{CCO3}	C10, C14, G14	B18, D16, E14, E17, E21, F18, G19, J18
V_{CCP0}	H1	L7
V_{CCP1}	H16	N18
V_{CCJ}	J1	P4
V_{REF0}	E7	A9
V_{REF1}	M7	AA10
V_{REF2}	R13	AA13
V_{REF3}	A8	A15
GND PLL 0	H7	L6
GND PLL 1	J10	L16
GND	A1, C5, C12, E3, E14, G7, G8, G9, G10, H8, H9, H10, J7, J8, J9, K7, K8, K9, K10, M3, M14, P5, P12	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22
NC[3]	—	AA1

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 51024 Power Supply and NC Connections[1]

Signal	484-Ball fpBGA[2]	676-Ball fpBGA[2]
V_{CC}	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6	B29, D6, D10, D12, D19, D21, D25, F4, F27, K4, K27, M4, M27, W4, W27, AA4, AA27, AE4, AE27, AG6, AG10, AG12, AG19, AG21,AG25, AJ2
V_{CCO0}	B5, D7, E2, E6, E9, F5, G4, J5	E5, E7, E9, E11, F10, G5, J5, K6, L5
V_{CCO1}	P5, U5, V6, V9, Y3	Y5, AA6, AB5, AD5, AE10, AF5, AF7, AF9, AF11
V_{CCO2}	P18, U18, V14, V17, Y20	Y26, AA25, AB26, AD26, AE21, AF20, AF22, AF24, AF26
V_{CCO3}	B18, D16, E14, E17, E21, F18, G19, J18	E20, E22, E24, E26, F21, G26, J26, K25, L26
V_{CCP0}	L7	P5
V_{CCP1}	N18	N26
V_{CCJ}	P4	U6
V_{REF0}	A9	C11
V_{REF1}	AA10	AK10
V_{REF2}	AA13	AJ21
V_{REF3}	A15	E19
GND PLL 0	L6	R6
GND PLL 1	L16	P25
GND	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22	A1, A30, B2,C3, C28, D8, D23, F7, F9, F11, F12, F19, F20, F22, F24, G6, G25, H4, H27, J6, J25, L6, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L25, M6, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M25, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14,U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W25, Y6, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y25, AB6, AB25, AC4, AC27, AD6, AD25, AE7, AE9, AE11, AE12, AE19, AE20, AE22, AE24, AG8, AG23, AH3, AH28, AK1, AK30
NC[3]	AA1	A14, A15, A16, A17, B14, B15, B16, B17, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, E13, E14, E15, E16, E17, E18, F13, F14, F15, F16, F17, F18, AE13, AE14, AE15, AE16, AE17, AE18, AF13, AF14, AF15, AF16, AF17, AF18, AG13, AG14, AG15, AG16, AG17, AG18, AH14, AH15, AH16, AH17, AH18, AJ14, AJ15, AJ16, AJ17, AJ18, AK14, AK15, AK16, AK17

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 5768VG Logic Signal Connections

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0C-30	C8	D11
0	0C-28	B6	B11
0	0C-26	A5	E12
0	0C-24	D8	C11
0	0C-22	E8	F12
0	0C-20	B5	B10
0	GNDIO0	GND	GND
0	0C-18	A4	A10
0	0C-16	D7	D10
0	0C-14/VREF0	E7	A9
0	0C-12	C6	E11
0	0C-10	B4	B9
0	0C-8	A3	F11
0	0C-6	NC	A8
0	0C-4	NC	C10
0	0C-2	NC	A7
0	0C-0	NC	E10
0	0D-30	NC	B8
0	0D-28	NC	C8
0	GNDIO0	GND	GND
0	0D-26	NC	F10
0	0D-24	NC	A6
0	0D-22	NC	F9
0	0D-20	NC	C7
0	0D-18	NC	D9
0	0D-16	NC	B7
0	0D-14	D6	E8
0	0D-12	E6	A5
0	0D-10	A2	F8
0	0D-8	B3	C6
0	0D-6	C4	D8
0	0D-4	D5	A3
0	GNDIO0	GND	GND
0	0D-2	NC	A2
0	0D-0	NC	A4
0	0A-0	NC	F7
0	0A-2	NC	C5
0	0A-4	NC	F6
0	0A-6	NC	B3
0	0A-8	NC	NC
0	0A-10	NC	NC
0	GNDIO0	GND	GND
0	0A-12	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0A-14	NC	NC
0	0A-16	NC	B4
0	0A-18	NC	D5
0	0A-20	NC	B1
0	0A-22	NC	D6
0	0A-24	NC	C4
0	0A-26	NC	E4
0	GNDIO0	GND	GND
0	0A-28	B2	C2
0	0A-30	B1	C1
0	0B-30	C2	D1
0	0B-28	C1	D2
0	0B-26	NC	D3
0	0B-24	NC	E1
0	0B-22	NC	E3
0	0B-20	NC	F4
0	0B-18	NC	F1
0	0B-16	NC	F3
0	0B-14	NC	G6
0	0B-12	NC	G1
0	GNDIO0	GND	GND
0	0B-10	NC	G2
0	0B-8	NC	H1
0	0B-6	NC	G3
0	0B-4	NC	H2
0	0B-2	NC	H5
0	0B-0	NC	H6
0	1A-0	F7	J1
0	1A-2	F6	K1
0	1A-4	E5	H3
0	1A-6	D4	J2
0	1A-8	D3	H4
0	1A-10	D2	K2
0	GNDIO0	GND	GND
0	1A-12	D1	J6
0	1A-14	E4	L1
0	1A-16	NC	K3
0	1A-18	NC	J4
0	1A-20	NC	L2
0	1A-22	NC	M1
0	1A-24	NC	K6
0	1A-26	NC	K4
0	1A-28	NC	L3

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
1	2C-26	T11	AA11
1	2C-28	T12	V12
1	2C-30	R10	AB11
2	3C-30	P9	W12
2	3C-28	R11	Y11
2	3C-26	T13	Y12
2	3C-24	N9	AB12
2	3C-22	M9	U12
2	3C-20	R12	AA12
2	GNDIO2	GND	GND
2	3C-18	P11	Y13
2	3C-16	N10	AB13
2	3C-14	M10	W13
2	3C-12/VREF2	R13	AA13
2	3C-10	T14	U13
2	3C-8	R14	AB14
2	3C-6	M11	V13
2	3C-4	N11	AA14
2	3C-2	P13	U14
2	3C-0	T15	AB15
2	3D-30	T16	Y15
2	3D-28	N12	AB16
2	GNDIO2	GND	GND
2	3D-26	NC	AA15
2	3D-24	NC	W14
2	3D-22	NC	AB17
2	3D-20	NC	Y16
2	3D-18	NC	AA16
2	3D-16	NC	Y17
2	3D-14	NC	AB18
2	3D-12	NC	V15
2	3D-10	NC	AB19
2	3D-8	NC	W15
2	3D-6	NC	AB20
2	3D-4	NC	AA18
2	GNDIO2	GND	GND
2	3D-2	L10	U15
2	3D-0	L11	W17
2	3A-0	K11	U16
2	3A-2	R15	AA19
2	3A-4	NC	V16
2	3A-6	NC	AB21
2	3A-8	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
2	3A-10	NC	NC
2	GNDIO2	GND	GND
2	3A-12	NC	NC
2	3A-14	NC	NC
2	3A-16	NC	Y18
2	3A-18	P15	W18
2	3A-20	R16	AA20
2	3A-22	P16	W19
2	3A-24	N14	Y19
2	3A-26	N13	V19
2	GNDIO2	GND	GND
2	3A-28	N15	Y21
2	3A-30	N16	W20
2	3B-30	M16	AA22
2	3B-28	M12	W21
2	3B-26	NC	Y22
2	3B-24	NC	V20
2	3B-22	M13	V21
2	3B-20	M15	W22
2	3B-18	L16	V18
2	3B-16	L15	U20
2	3B-14	L13	V22
2	3B-12	L14	U19
2	GNDIO2	GND	GND
2	3B-10	L12	U17
2	3B-8	K13	U22
2	3B-6	K15	T20
2	3B-4	K16	T21
2	3B-2	J16	T17
2	3B-0	K12	R20
3	4B-0	J12	R21
3	4B-2	G16	T22
3	4B-4/PLL_FBK1	G15	P21
3	4B-6/PLL_RST1	H12	N20
3	4B-8	G12	R22
3	4B-10	G13	N21
3	GNDIO3	GND	GND
3	4B-12	F16	M18
3	4B-14	F15	N19
3	4B-16	F13	P22
3	4B-18	F14	M20
3	4B-20	F12	N22
3	4B-22	E16	N17

ispMACH 51024VG Logic Signal Connections (Continued)

Bank No.	Signal	484 fpBGA	676 fpBGA
3	6A-10	K21	J29
3	6A-8	K18	K26
3	6A-6	J17	J28
3	6A-4	J19	H30
3	6A-2	J22	J27
3	6A-0	J21	H29
3	7B-0	H19	G30
3	7B-2	H20	H28
3	7B-4	H17	G29
3	7B-6	H18	F30
3	7B-8	H22	G28
3	7B-10	H21	H26
3	GNDIO3	GND	GND
3	7B-12	G20	F29
3	7B-14	G22	G27
3	7B-16	G17	E30
3	7B-18	G21	F28
3	7B-20	F19	H25
3	7B-22	F20	E29
3	7B-24	F22	D30
3	7B-26	E22	E28
3	7B-28	E19	D29
3	7B-30	E20	C30
3	7A-30	D22	F26
3	7A-28	D21	E27
3	GNDIO3	GND	GND
3	7A-26	D20	D28
3	7A-24	C22	F25
3	7A-22	C18	C29
3	7A-20	C19	B30
3	7A-18	D17	D27
3	7A-16	C21	E25
3	7A-14	NC	D26
3	7A-12	NC	C27
3	GNDIO3	GND	GND
3	7A-10	NC	B28
3	7A-8	NC	A29
3	7A-6	B22	F23
3	7A-4	D18	C26
3	7A-2	B20	B27
3	7A-0	F17	A28
3	7D-0	B19	A27
3	7D-2	C17	B26

Bank No.	Signal	484 fpBGA	676 fpBGA
3	GNDIO3	GND	GND
3	7D-4	A21	E23
3	7D-6	D15	D24
3	7D-8	A20	C25
3	7D-10	C16	A26
3	7D-12	A19	B25
3	7D-14	F16	C24
3	7D-16	B16	A25
3	7D-18	D14	B24
3	7D-20	A18	C23
3	7D-22	F15	D22
3	7D-24	A17	A24
3	7D-26	B15	E21
3	GNDIO3	GND	GND
3	7D-28	A16	B23
3	7D-30	F14	C22
3	7C-0	C15	A23
3	7C-2	D13	B22
3	7C-4	E15	C21
3	7C-6	F13	A22
3	7C-8	B14	D20
3	7C-10	E13	B21
3	7C-12/VREF3	A15	E19
3	7C-14	D12	C20
3	7C-16	A14	A21
3	7C-18	B13	B20
3	GNDIO3	GND	GND
3	7C-20	A13	A20
3	7C-22	B12	C19
3	7C-24	C13	B19
3	7C-26	A12	A19
3	7C-28	C12	B18
3	7C-30	A11	A18
—	GCLK0	P6	R5
—	GCLK1	R6	T6
—	GCLK2	P17	R25
—	GCLK3	P19	P26
—	GOE0	R18	T26
—	GOE1	R17	R26
—	RESETB	R19	T25
—	TCK	R3	U5
—	TDI	R2	T5
—	TDO	R4	V5

Signal Configuration

ispMACH 5768VG and 51024VG 484-ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O / VREF3	I/O	I/O	I/O	I/O	I/O	I/O/ VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	**A**
B	I/O	VCC	I/O	I/O	VCCO3	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCCO0	I/O	I/O	VCC	I/O	**B**
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	**C**
D	I/O	I/O	I/O	GND	I/O	I/O	VCCO3	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO0	I/O	I/O	GND	I/O	I/O	I/O	**D**
E	I/O	VCCO3	I/O	I/O	VCC	VCCO3	GND	I/O	VCCO3	I/O	I/O	I/O	I/O	VCCO0	I/O	GND	VCCO0	VCC	I/O	I/O	VCCO0	I/O	**E**
F	I/O	VCC	I/O	I/O	VCCO3	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO0	I/O	I/O	VCC	I/O	**F**
G	I/O	I/O	I/O	VCCO3	GND	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	GND	VCCO0	I/O	I/O	I/O	**G**
H	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	**H**
J	I/O	I/O	VCC	I/O	VCCO3	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	VCCO0	I/O	VCC	I/O	I/O	**J**
K	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	**K**
L	I/O	I/O	I/O/ CLK_OUT1	I/O	I/O	I/O	GNDP1	GND	GND	GND	GND	GND	GND	GND	GND	VCCP0	GNDP0	I/O	I/O	I/O	I/O	I/O	**L**
M	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O/ PLL_RST0	I/O	I/O	I/O	**M**
N	I/O	I/O	I/O/ PLL_RST1	I/O	VCCP1	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O/ PLL_FBK0	I/O	I/O	I/O/ CLK_OUT0	**N**
P	I/O	I/O/ PLL_FBK1	VCC	GCLK3	VCCO2	GCLK2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK0	VCCO1	VCCJ	VCC	I/O	I/O	**P**
R	I/O	I/O	I/O	RESETB	GOE0	GOE1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK1	I/O	TDO	TCK	TDI	I/O	**R**
T	I/O	I/O	I/O	GND	TOE	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	GND	I/O	I/O	TMS	**T**
U	I/O	VCC	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	VCC	I/O	**U**
V	I/O	I/O	I/O	I/O	I/O	VCCO2	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	VCCO1	I/O	I/O	I/O	I/O	I/O	**V**
W	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	**W**
Y	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	**Y**
AA	I/O	VCC	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	VCC	I/O	I/O	I/O	VCC	NC[1]	**AA**
AB	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	**AB**
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

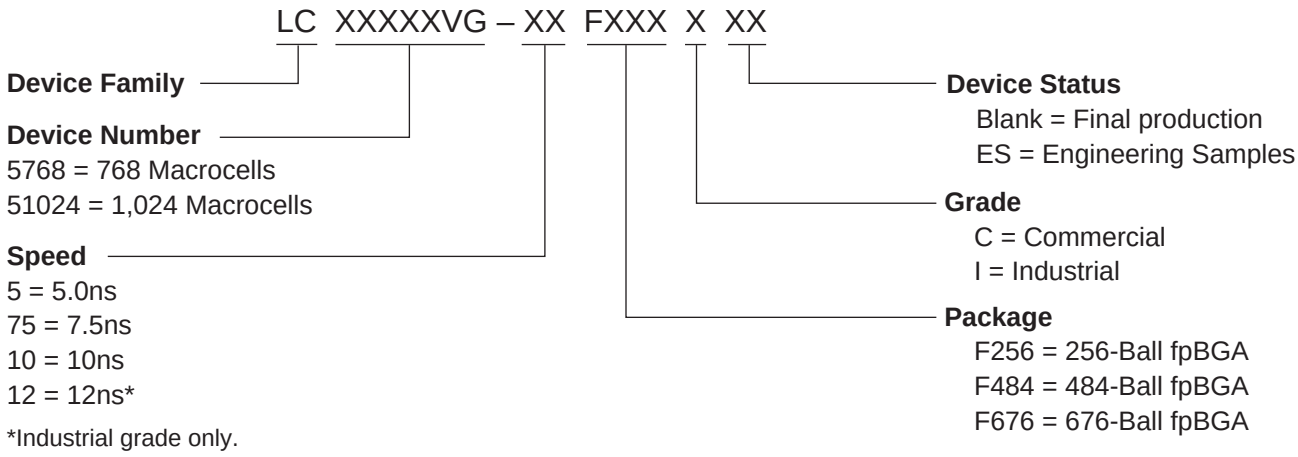
ispMACH 5768VG and 51024VG 484BGA/51024VG

Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/ispm5vg

Ordering Information

Commercial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-5F484C	fpBGA	484	1024	5	3.3
LC51024VG-75F484C	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484C	fpBGA	484	1024	10	3.3
LC51024VG-5F676C	fpBGA	676	1024	5	3.3
LC51024VG-75F676C	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676C	fpBGA	676	1024	10	3.3
LC5768VG-5F256C	fpBGA	256	768	5	3.3
LC5768VG-75F256C	fpBGA	256	768	7.5	3.3
LC5768VG-10F256C	fpBGA	256	768	10	3.3
LC5768VG-5F484C	fpBGA	484	768	5	3.3
LC5768VG-75F484C	fpBGA	484	768	7.5	3.3
LC5768VG-10F484C	fpBGA	484	768	10	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).

Industrial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-75F484I	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484I	fpBGA	484	1024	10	3.3
LC51024VG-12F484I	fpBGA	484	1024	12	3.3
LC51024VG-75F676I	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676I	fpBGA	676	1024	10	3.3
LC51024VG-12F676I	fpBGA	676	1024	12	3.3
LC5768VG-75F256I	fpBGA	256	768	7.5	3.3
LC5768VG-10F256I	fpBGA	256	768	10	3.3
LC5768VG-12F256I	fpBGA	256	768	12	3.3
LC5768VG-75F484I	fpBGA	484	768	7.5	3.3
LC5768VG-10F484I	fpBGA	484	768	10	3.3
LC5768VG-12F484I	fpBGA	484	768	12	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 5000VG family:

- *ispMACH 5000VG sysIO Design and Usage Guidelines* (TN1000)
- *ispMACH 5000VG Timing Model Design and Usage Guidelines* (TN1001)
- *Power Estimation in ispMACH 5000VG Devices* (TN1002)
- *ispMACH 5000VG PLL Usage Guidelines* (TN1003)