Lattice Semiconductor Corporation - LC5768VG-75F484C Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	304
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768vg-75f484c

The ispMACH5000VG devices also contain sysCLOCK Phase Locked Loops (PLLs) that provide designers with increased clocking flexibility. The PLLs can be used to synthesize new clocks for use on-chip or elsewhere within the system. They can also be used to deskew clocks, again both at the chip and system levels. A variable delay line capability further improves this and allows designers to retard or advance the clock in order to tune set-up and clock-to-out times for optimal results. The ispMACH 5000VG Family Selection Guide (Table 1) details the key attributes and packages for the ispMACH 5000VG devices.

ispMACH 5000VG Architecture

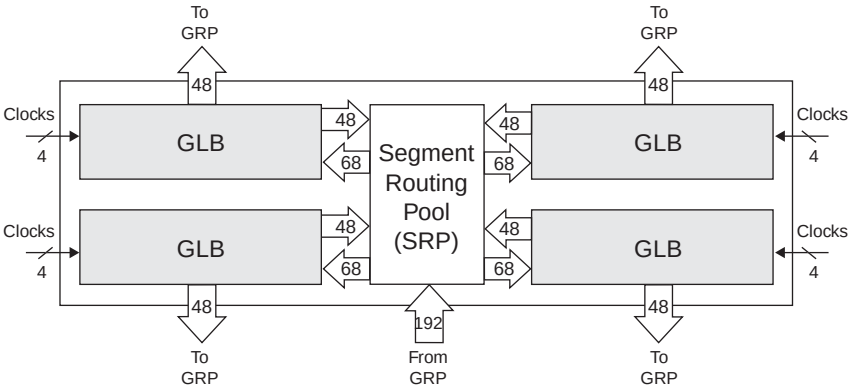
The ispMACH 5000VG Family of In-System Programmable High Density Logic Devices is based on segments containing four Generic Logic Blocks (GLBs) and a hierarchical routing pool (GRP) structure interconnecting the segments. A segment routing pool (SRP) connects each GLB in a segment allowing the maximum flexibility and speed.

Outputs from the GLBs drive the Segment Routing Pool (SRP) and the Global Routing Pool (GRP). Enhanced switching resources are provided to allow signals in the Segment Routing Pool to drive any or all the GLBs in the segment. Optimal switching is provided to allow all signals in the Global Routing Pool to be routed to any or all SRPs. This mechanism allows fast, efficient connections across the entire device.

Segment

Each segment contains four GLBs and a segment routing pool (SRP). Each GLB has 32 internal feedback outputs and 16 external feedback outputs, for a total of 48 outputs from each GLB feeding the SRP. The SRP contains up to 384 signals, 48 from each GLB and 192 from the GRP, with full routing capability. This routing scheme maximizes the flexibility and speed of the device without sacrificing the routing.

Figure 2. Segment



Generic Logic Block

Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and three control product terms. The GLB has 68 inputs from the Segment Routing Pool, which are available in both true and complement form for every product term. The three control product terms are used for shared reset, clock and output enable functions. Figure 3 shows the structure of the GLB from the macrocell perspective. This is referred to as a macrocell slice. There are 32 macrocell slices per GLB.

AND-Array

The programmable AND-Array consists of 68 inputs and 163 output product terms. The 68 inputs from the SRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 163 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining three control product terms feeding the Shared PT Clock, Shared PT Reset and Shared PT OE. Every set of five product terms from the 160 logic product terms forms a product term cluster start-

Enhanced Dual-OR Array

To facilitate logic functions requiring a very large number of product terms, the ispMACH 5000VG architecture has been enhanced with an innovative product term expander capability. This capability is embedded in the Dual-OR Array. The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the GLB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate.

The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 5 is a graphical representation of the Enhanced Dual-OR Array.

Figure 5. Enhanced Dual-OR Array

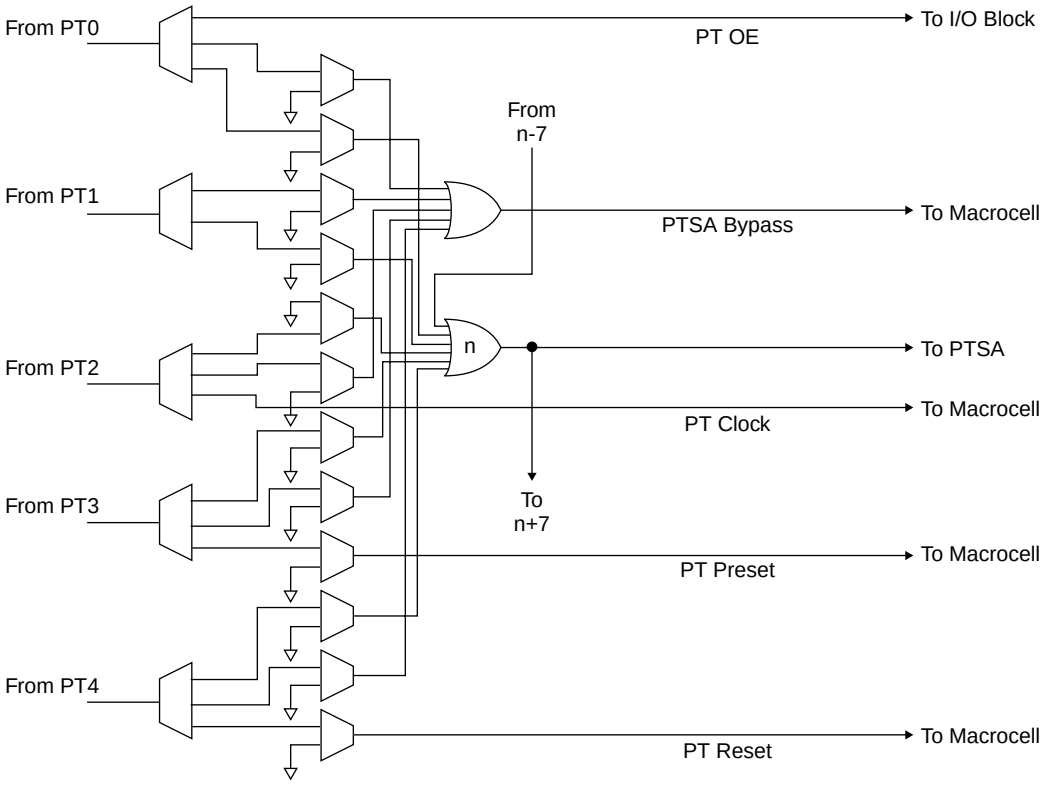
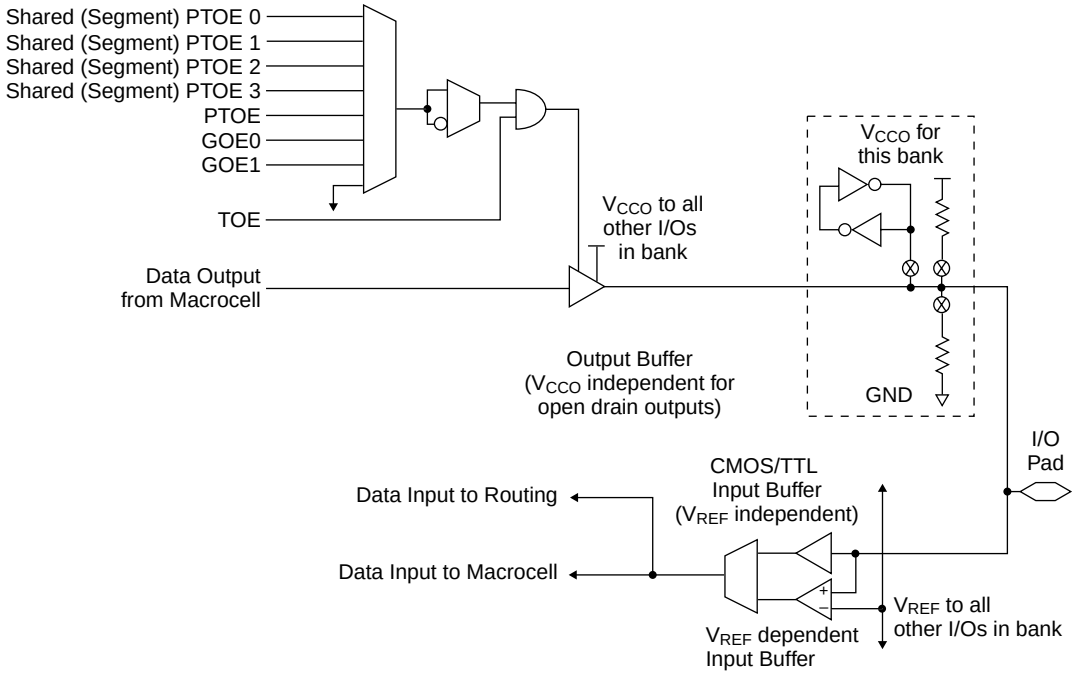


Figure 8. I/O Cell



sysIO Capability

The ispMACH 5000VG devices are divided into four sysIO banks, where each bank is capable of supporting 14 different I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing each bank complete independence from the others. Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Table 2 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

Table 2. ispMACH 5000VG Supported I/O Standards

sysIO Standard	V_{CCO}	V_{REF}	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3	3.3V	N/A	N/A
PCI-X	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	1.5V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential[1]	N/A	N/A	N/A
LVDS[1]	N/A	N/A	N/A

1. LVDS and LVPECL are only supported on the dedicated clock pins.

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage (V_{CC}) . . . . . -0.5 to 5.4V

PLL Supply Voltage (V_{CCP}) . . . . . -0.5 to 5.4V

Output Supply Voltage (V_{CCO}) . . . . . -0.5 to 5.4V

Input Voltage Applied[4] . . . . . -0.5 to 5.6V

Tri-state Output Voltage Applied. . . . . -0.5 to 5.6V

Storage Temperature . . . . . -65 to 150°C

Junction Temperature (Tj) with Power Applied . . . . . -55 to 130°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IH} (MAX)+2) volts is permitted for a duration of < 20ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{CCP}	Supply Voltage for PLL block	3.0	3.6	V
V_{CCJ}	Supply Voltage for IEEE1149.1 Test Access Port	1.65	3.6	V
Tj (Commercial)	Junction Commercial Operation	0	90	C
Tj (Industrial)	Junction Industrial Operation	-40	105	C

Note: V_{CCJ} must be set in appropriate range to be compatible with desired LVCMOS standard.

Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle	1000	—	Cycles

Hot Socketing Characteristics[1,2,3]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-100	µA
		V_{IH} (MAX) $\le V_{IN} \le$ 5.5V	—	—	+/-100	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise / fall rates for V_{CC} and V_{CCO}.
2. LVTTL, LVCMOS only
3. $0 < V_{CC} \le V_{CC}$ (MAX), $0 < V_{CCO} \le V_{CCO}$ (MAX)

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	+/-10	µA
I_{PU}[2]	I/O Weak Pull-up Resistor Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	-150	µA
			V_{CCO} = 2.5	-20	—	-150	µA
			V_{CCO} = 1.8	-10	—	-150	µA
I_{PD}[2]	I/O Weak Pull-down Resistor Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)		30	—	150	µA
I_{BHLS}[2]	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)		30	—	—	µA
I_{BHHS}[2]	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	V_{CCO} = 3.3	-30	—	—	µA
			V_{CCO} = 2.5	-20	—	—	µA
			V_{CCO} = 1.8	-10	—	—	µA
I_{BHLO}[2]	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	150	µA
I_{BHHO}[2]	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{IH}$ (MAX)		—	—	-150	µA
I_{CC}[3, 4, 5]	Operating Power Supply Current	V_{CC} = 3.3V		—	380	—	mA
V_{BHT}	Bus Hold Trip Points			V_{IL} (MAX)	—	V_{IH} (MIN)	V
C_1	I/O Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_2	Clock Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					
C_3	Global Input Capacitance[3]	V_{CC} = 3.3V, V_{IO} = 0 to V_{IH} (MAX)		—	10	—	pf
		V_{CCO} = 3.3V, 2.5, 1.8, 1.5					

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. Only available for LVCMOS and LVTTL standards.
3. T_A = 25°C, f = 1.0MHz.
4. Device configured with 16-bit counters.
5. I_{CC} varies with specific device configuration and operating frequency.

sysIO Recommended Operating Conditions[2]

Standard	V_{CCO} (V)		V_{REF} (V)	
	Min	Max	Min	Max
LVCMOS 3.3[1]	3.0	3.6	—	—
LVCMOS 2.5	2.3	2.7	—	—
LVCMOS 1.8	1.65	1.95	—	—
LVTTL	3.0	3.6	—	—
PCI 3.3	3.0	3.6	—	—
PCI-X	3.0	3.6	—	—
AGP-1X	3.15	3.45	—	—
SSTL 2	2.3	2.7	1.15	1.35
SSTL 3	3.0	3.6	1.3	1.7
CTT 3.3	3.0	3.6	1.35	1.65
CTT 2.5	2.3	2.7	1.35	1.65
HSTL	1.4	1.6	0.68	0.9
GTL+	1.4	3.6	0.882	1.122

1. Software default setting.
2. Typical values for V_{CCO} and V_{REF} are the average of the Min and Max values.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3[1]	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	16, 12 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCO}$	$0.65V_{CCO}$	3.6	0.4	V_{CCO}-0.4	12, 8, 5.33, 4	-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
PCI-X	-0.3	$0.35V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
AGP-1X	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.7	V_{CCO}-1.1	8	-8
SSTL3 class II	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.5	V_{CCO}-0.9	16	-16
SSTL2 class I	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.54	V_{CCO}-0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF}-0.18	V_{REF}+0.18	3.6	0.35	V_{CCO}-0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
CTT 2.5	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.4	V_{REF}+0.4	8	-8
HSTL class I	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	8	-8
HSTL class III	-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CCO}-0.4	24	-8
GTL+	-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	0.6	n/a	36	n/a

1. Software default setting
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed 96mA.

sysIO Differential Input DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max
V_{INP} . V_{INM}	LVDS Input voltage	—	0	2.4
V_{THD}	LVDS Differential input threshold	—	±100mV	—
V_{IL}	LVPECL Input Voltage Low	V_{CC} = 3.0 to 3.6V	V_{CC}-1.81	V_{CC}-1.48
		V_{CC} = 3.3V	1.49V	1.83V
V_{IH}	LVPECL Input Voltage High	V_{CC} = 3.0 to 3.6V	V_{CC}-1.17	V_{CC}-0.88
		V_{CC} = 3.3V	2.14V	2.42V

ispMACH 51024VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description[1,2,3]	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}[4]	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.10

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 5768VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t_{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t_{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t_{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t_{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t_{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t_{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t_{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t_{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t_{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t_{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
$t_{PLL\_SEC\_DELAY}$	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t_{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t_{S}	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t_{H}	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t_{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns
t_{CES}	Clock Enable Setup Time	2.60	—	3.90	—	5.05	—	5.95	—	ns
t_{CEH}	Clock Enable Hold Time	0.60	—	0.90	—	1.20	—	1.45	—	ns
t_{SL}	Latch Setup Time	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{SL_PT}	Latch Setup Time with PT Clock	2.80	—	4.20	—	5.50	—	6.60	—	ns
t_{HL}	Latch Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t_{GOi}	Latch Gate to Output/Feedback MUX Time	—	1.75	—	2.50	—	3.50	—	4.50	ns
t_{PDLi}	Propagation Delay through Transparent Latch to Output/Feedback MUX	—	2.40	—	3.50	—	4.00	—	4.50	ns
t_{SRi}	Asynchronous Reset or Set to Output/Feedback MUX Delay	—	0.75	—	1.00	—	1.25	—	1.50	ns
t_{SRR}	Asynchronous Reset or Set Recovery Delay	—	1.00	—	1.50	—	2.00	—	2.50	ns
Control Delays										
t_{BCLK}	GLB PT Clock Delay	—	3.10	—	4.65	—	6.00	—	7.00	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	3.00	—	4.50	—	6.00	—	7.00	ns

ispMACH 51024VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
LVDS_in	t_{GCLK_IN}	Using LVDS standard	—	1.70	—	1.70	—	1.70	—	1.70	ns
LVPECL_in	t_{GCLK_IN}	Using LVPECL standard	—	2.10	—	2.10	—	2.10	—	2.10	ns
t_{IOO} Output Adders											
LVCMOS18_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 4mA Buffer	—	3.00	—	3.00	—	3.00	—	3.00	ns
LVCMOS18_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 5.33mA Buffer	—	2.50	—	2.50	—	2.50	—	2.50	ns
LVCMOS18_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 8mA Buffer	—	1.85	—	1.85	—	1.85	—	1.85	ns
LVCMOS18_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 1.8V & 12mA Buffer	—	1.35	—	1.35	—	1.35	—	1.35	ns
LVCMOS25_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS25_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS25_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 8mA Buffer	—	0.70	—	0.70	—	0.70	—	0.70	ns
LVCMOS25_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 12mA Buffer	—	0.50	—	0.50	—	0.50	—	0.50	ns
LVCMOS25_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 2.5V & 16mA Buffer	—	0.25	—	0.25	—	0.25	—	0.25	ns
LVCMOS33_4mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 4mA Buffer	—	1.50	—	1.50	—	1.50	—	1.50	ns
LVCMOS33_5mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 5.33mA Buffer	—	1.25	—	1.25	—	1.25	—	1.25	ns
LVCMOS33_8mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 8mA Buffer	—	0.40	—	0.40	—	0.40	—	0.40	ns
LVCMOS33_12mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 12mA Buffer	—	0.10	—	0.10	—	0.10	—	0.10	ns
LVCMOS33_16mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 16mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVCMOS33_20mA_out	t_{BUF}, t_{EN}, t_{DIS}	Output configured as 3.3V & 20mA Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{BUF}, t_{EN}, t_{DIS}	Output configured as LVTTL Buffer	—	0.0	—	0.0	—	0.0	—	0.0	ns
Slow Slew	t_{BUF}, t_{EN}	Output configured for slow slew rate	—	1.50	—	1.50	—	1.50	—	1.50	ns
PCI_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_out	t_{BUF}, t_{EN}, t_{DIS}	Using PCI-X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_out	t_{BUF}, t_{EN}, t_{DIS}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_I standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
SSTL3_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL3_II standard	—	-0.35	—	-0.35	—	-0.35	—	-0.35	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

ispMACH 51024VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
SSTL2_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF}, t_{EN}, t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF}, t_{EN}, t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns
HSTL_III_out	t_{BUF}, t_{EN}, t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF}, t_{EN}, t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

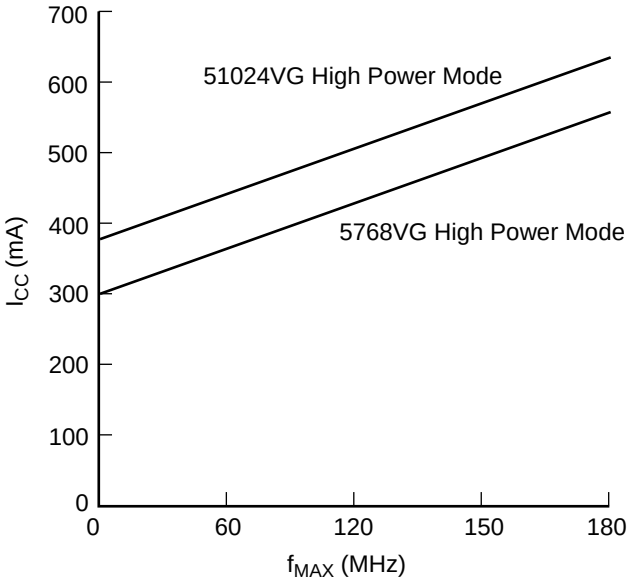
Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

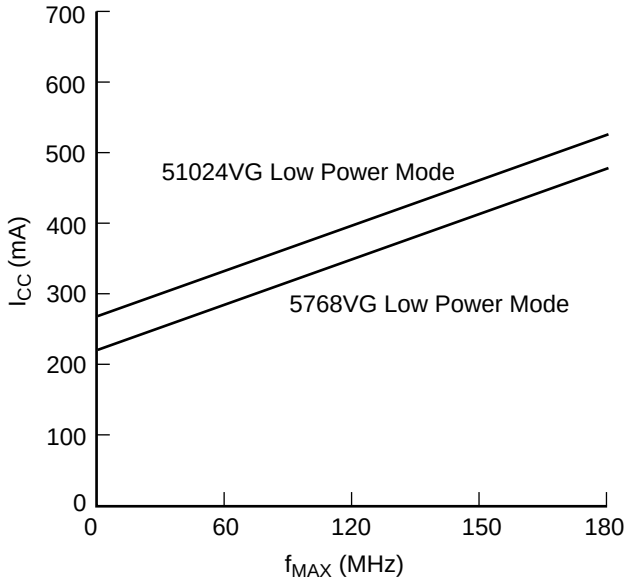
Power Consumption

ispMACH 5000VG Typical Power vs. Frequency

ispMACH 5000VG I_{CC} Curves at High Power Mode



ispMACH 5000VG I_{CC} Curves at Low Power Mode



Note: The devices are configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V, 25° C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	I_{DC} (mA)	I_{DCO} (mA)
ispMACH 5768VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	65	20
ispMACH 51024VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	80	20

Note: For further information about the use of these coefficients, refer to Technical Note TN1002, *Power Estimation in ispMACH 5000VG Devices*.

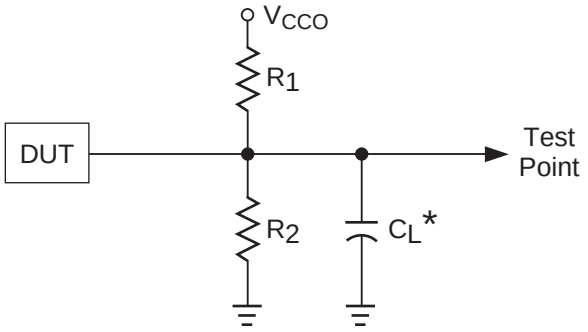
K0 = average current per product term in high power/MHz
K1 = average current per product term in low power/MHz
K2 = average current per GRP line/MHz
K3 = average current per PLL/MHz
K4 = DC current per product terms in high power
K5 = DC current per product terms in low power
K6 = Static DC current per PLL
I_{DC} = Static device current with all product terms powered off
I_{DCO} = Static I/O bank current

Icc estimates are based on typical conditions (Vcc = 3.3V, room temperature) and an assumption of one GLB load on average exists. These values are for estimates only. Since the value of Icc is sensitive to operating conditions and the program in the device, the actual Icc should be verified.

Switching Test Conditions

Figure 12 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.

Figure 12. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes Test Fixture and Probe Capacitance.

0213A/ispm5kvg

Table 3. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 3.3 I/O (L -> H, H -> L)	110	110	35pF	1.5	3.0V
Other LVCMOS Settings, (L -> H, H -> L)	∞	∞	35pF	LVCMOS 3.3 = 1.5V	LVCMOS 3.3 = 3.0V
				LVCMOS 2.5 = V_{CCO}/2	LVCMOS 2.5 = 2.3V
				LVCMOS 1.8 = V_{CCO}/2	LVCMOS 1.8 = 1.65V
Default LVCMOS 3.3 I/O (Z -> H)	∞	110	35pF	1.5V	3.0V
Default LVCMOS 3.3 I/O (Z -> L)	110	∞	35pF	1.5V	3.0V
Default LVCMOS 3.3 I/O (H -> Z)	∞	110	5pF	V_{OH} - 0.3	3.0V
Default LVCMOS 3.3 I/O (L -> Z)	110	∞	5pF	V_{OL} + 0.3	3.0V

Output test conditions for all other interfaces are determined by the respective standards. For further details, please refer to the following technical note:

- *ispMACH 5000VG sysIO Design and Usage Guidelines* (TN1000)

Signal Descriptions

Signal Names	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the 1149.1 state machine.
TCK	Input - This pin is the Test Clock input pin, used to clock the 1149.1 state machine.
TDI	Input - This pin is the 1149.1 Test Data In pin, used to load data.
TDO	Output - This pin is the 1149.1 Test Data Out pin used to shift data out.
TOE	Input - Test Output Enable pin. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
RESETB	Dedicated Reset Input - This pin resets all registers in the devices. The global polarity (active high or low input) for this pin is selectable.
xyzz (e.g. 0A16)	Input/Output - These are the general purpose I/O used by the logic array. *x* is segment reference (numeric), *y* is GLB reference (alpha) and *z* is macrocell reference (numeric). *x*: 0-7 (1024) *x*: 0-5 (768) *y*: A-D *z*: 0-31
GND	Ground
NC	No connect
V_{CC}	Vcc - These are the power supply pins for the logic core.
GCLK0, GCLK3	Input - These pins are configured to be either dedicated CLK input or PLL input.
GCLK1, GCLK2	Input - These pins are dedicated CLK input.
CLK_OUT0, CLK_OUT1	Output - These pins are the PLL output pins.
PLL_RST0, PLL_RST1	Input - These pins are for resetting the PLL, input clock (M) divider.
VREF0, VREF1, VREF2, VREF3	Input - These are the reference supplies for the I/O banks.
PLL_FBK0, PLL_FBK1	Input - These PLL feedback inputs allow optional external PLL feedback.
V_{CCP0}, V_{CCP1}	V_{CC} - These are the V_{CC} supplies for the PLLs.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} - These are the V_{CC} supplies for each I/O bank.
GNDP0, GNDP1	GND - These are the separate ground connections for the PLLs.
V_{CCJ}	V_{CC} - This pin is for the 1149.1 test access port.

Note: For above, signal CLK_OUT0 connects to PLL0, and signal CLK_OUT1 connects to PLL1.

ispMACH 51024 Power Supply and NC Connections[1]

Signal	484-Ball fpBGA[2]	676-Ball fpBGA[2]
V_{CC}	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6	B29, D6, D10, D12, D19, D21, D25, F4, F27, K4, K27, M4, M27, W4, W27, AA4, AA27, AE4, AE27, AG6, AG10, AG12, AG19, AG21,AG25, AJ2
V_{CCO0}	B5, D7, E2, E6, E9, F5, G4, J5	E5, E7, E9, E11, F10, G5, J5, K6, L5
V_{CCO1}	P5, U5, V6, V9, Y3	Y5, AA6, AB5, AD5, AE10, AF5, AF7, AF9, AF11
V_{CCO2}	P18, U18, V14, V17, Y20	Y26, AA25, AB26, AD26, AE21, AF20, AF22, AF24, AF26
V_{CCO3}	B18, D16, E14, E17, E21, F18, G19, J18	E20, E22, E24, E26, F21, G26, J26, K25, L26
V_{CCP0}	L7	P5
V_{CCP1}	N18	N26
V_{CCJ}	P4	U6
V_{REF0}	A9	C11
V_{REF1}	AA10	AK10
V_{REF2}	AA13	AJ21
V_{REF3}	A15	E19
GND PLL 0	L6	R6
GND PLL 1	L16	P25
GND	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22	A1, A30, B2,C3, C28, D8, D23, F7, F9, F11, F12, F19, F20, F22, F24, G6, G25, H4, H27, J6, J25, L6, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L25, M6, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M25, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14,U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W25, Y6, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y25, AB6, AB25, AC4, AC27, AD6, AD25, AE7, AE9, AE11, AE12, AE19, AE20, AE22, AE24, AG8, AG23, AH3, AH28, AK1, AK30
NC[3]	AA1	A14, A15, A16, A17, B14, B15, B16, B17, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, E13, E14, E15, E16, E17, E18, F13, F14, F15, F16, F17, F18, AE13, AE14, AE15, AE16, AE17, AE18, AF13, AF14, AF15, AF16, AF17, AF18, AG13, AG14, AG15, AG16, AG17, AG18, AH14, AH15, AH16, AH17, AH18, AJ14, AJ15, AJ16, AJ17, AJ18, AK14, AK15, AK16, AK17

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
3	4B-24	G11	M19
3	4B-26	F11	M21
3	4B-28	F10	L19
3	4B-30/CLK_OUT1	B11	L20
3	GNDIO3	GND	GND
3	4A-30	NC	M17
3	4A-28	NC	M22
3	4A-26	NC	K20
3	4A-24	NC	L18
3	4A-22	NC	L21
3	4A-20	NC	K19
3	4A-18	NC	L22
3	4A-16	NC	K17
3	4A-14	E13	K22
3	4A-12	B12	L17
3	GNDIO3	GND	GND
3	4A-10	E15	K21
3	4A-8	D15	K18
3	4A-6	NC	J17
3	4A-4	NC	J19
3	4A-2	D16	J22
3	4A-0	E12	J21
3	5B-0	NC	H19
3	5B-2	NC	H20
3	5B-4	NC	H17
3	5B-6	NC	H18
3	5B-8	NC	H22
3	5B-10	NC	H21
3	GNDIO3	GND	GND
3	5B-12	NC	G20
3	5B-14	NC	G22
3	5B-16	NC	G17
3	5B-18	NC	G21
3	5B-20	NC	F19
3	5B-22	NC	F20
3	5B-24	A16	F22
3	5B-26	B15	E22
3	5B-28	A15	E19
3	5B-30	D13	E20
3	5A-30	B14	D22
3	5A-28	B16	D21
3	GNDIO3	GND	GND
3	5A-26	C16	D20

Bank No.	Signal	256 fpBGA	484 fpBGA
3	5A-24	C15	C22
3	5A-22	D14	C18
3	5A-20	A14	C19
3	5A-18	C13	D17
3	5A-16	B13	C21
3	5A-14	NC	NC
3	5A-12	NC	NC
3	GNDIO3	GND	GND
3	5A-10	NC	NC
3	5A-8	NC	NC
3	5A-6	NC	B22
3	5A-4	NC	D18
3	5A-2	NC	B20
3	5A-0	NC	F17
3	5D-0	NC	B19
3	5D-2	NC	C17
3	GNDIO3	GND	GND
3	5D-4	NC	A21
3	5D-6	NC	D15
3	5D-8	NC	A20
3	5D-10	NC	C16
3	5D-12	NC	A19
3	5D-14	NC	F16
3	5D-16	NC	B16
3	5D-18	NC	D14
3	5D-20	NC	A18
3	5D-22	A13	F15
3	5D-24	A12	A17
3	5D-26	A11	B15
3	GNDIO3	GND	GND
3	5D-28	A10	A16
3	5D-30	C11	F14
3	5C-0	A9	C15
3	5C-2	D12	D13
3	5C-4	D11	E15
3	5C-6	B10	F13
3	5C-8	B9	B14
3	5C-10	E11	E13
3	5C-12/VREF3	A8	A15
3	5C-14	D10	D12
3	5C-16	E10	A14
3	5C-18	A7	B13
3	GNDIO3	GND	GND

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
3	5C-20	C9	A13
3	5C-22	E9	B12
3	5C-24	D9	C13
3	5C-26	B8	A12
3	5C-28	A6	C12
3	5C-30	B7	A11
—	GCLK0	H4	P6
—	GCLK1	J4	R6
—	GCLK2	H14	P17
—	GCLK3	H13	P19
—	GOE0	J15	R18
—	GOE1	H15	R17
—	RESETB	J14	R19
—	TCK	J3	R3
—	TDI	H3	R2
—	TDO	J2	R4
—	TMS	H2	T1
—	TOE	J13	T18

Signal Configuration

ispMACH 5768VG 256-ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF3	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	I/O	I/O	I/O	I/O	I/O/ CLK_OUT1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	B
C	I/O	I/O	VCCO3	I/O	GND	I/O	VCCO3	I/O	I/O	VCCO0	I/O	GND	I/O	VCCO0	I/O	I/O	C
D	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	D
E	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF0	I/O	I/O	I/O	GND	I/O	I/O	E
F	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ PLL_RST0	F
G	I/O	I/O/ PLL_FBK1	VCCO3	I/O	I/O	I/O	GND	GND	GND	GND	I/O/ CLK_OUT0	I/O	I/O	VCCO0	I/O/ PLL_FBK0	I/O	G
H	VCCP1	GOE1	GCLK2	GCLK3	I/O/ PLL_RST1	VCC	GND	GND	GND	GNDP0	VCC	I/O	GCLK0	TDI	TMS	VCCP0	H
J	I/O	GOE0	RESETB	TOE	I/O	VCC	GNDP1	GND	GND	GND	VCC	I/O	GCLK1	TCK	TDO	VCCJ	J
K	I/O	I/O	VCCO2	I/O	I/O	I/O	GND	GND	GND	GND	I/O	I/O	I/O	VCCO1	I/O	I/O	K
L	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	L
M	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	GND	I/O	I/O	M
N	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	VCCO2	I/O	GND	I/O	VCCO2	I/O	I/O	VCCO1	I/O	GND	I/O	VCCO1	I/O	I/O	P
R	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 5768VG

256fpBGA/5768VG

Bottom View

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispMACH 5768VG and 51024VG 484-ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O / VREF3	I/O	I/O	I/O	I/O	I/O	I/O/ VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	**A**
B	I/O	VCC	I/O	I/O	VCCO3	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCCO0	I/O	I/O	VCC	I/O	**B**
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	**C**
D	I/O	I/O	I/O	GND	I/O	I/O	VCCO3	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO0	I/O	I/O	GND	I/O	I/O	I/O	**D**
E	I/O	VCCO3	I/O	I/O	VCC	VCCO3	GND	I/O	VCCO3	I/O	I/O	I/O	I/O	VCCO0	I/O	GND	VCCO0	VCC	I/O	I/O	VCCO0	I/O	**E**
F	I/O	VCC	I/O	I/O	VCCO3	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO0	I/O	I/O	VCC	I/O	**F**
G	I/O	I/O	I/O	VCCO3	GND	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	GND	VCCO0	I/O	I/O	I/O	**G**
H	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	**H**
J	I/O	I/O	VCC	I/O	VCCO3	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	VCCO0	I/O	VCC	I/O	I/O	**J**
K	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	**K**
L	I/O	I/O	I/O/ CLK_OUT1	I/O	I/O	I/O	GNDP1	GND	GND	GND	GND	GND	GND	GND	GND	VCCP0	GNDP0	I/O	I/O	I/O	I/O	I/O	**L**
M	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O/ PLL_RST0	I/O	I/O	I/O	**M**
N	I/O	I/O	I/O/ PLL_RST1	I/O	VCCP1	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O/ PLL_FBK0	I/O	I/O	I/O/ CLK_OUT0	**N**
P	I/O	I/O/ PLL_FBK1	VCC	GCLK3	VCCO2	GCLK2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK0	VCCO1	VCCJ	VCC	I/O	I/O	**P**
R	I/O	I/O	I/O	RESETB	GOE0	GOE1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK1	I/O	TDO	TCK	TDI	I/O	**R**
T	I/O	I/O	I/O	GND	TOE	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	GND	I/O	I/O	TMS	**T**
U	I/O	VCC	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	VCC	I/O	**U**
V	I/O	I/O	I/O	I/O	I/O	VCCO2	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	VCCO1	I/O	I/O	I/O	I/O	I/O	**V**
W	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	**W**
Y	I/O	I/O	VCCO2	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	VCCO1	I/O	I/O	**Y**
AA	I/O	VCC	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	VCC	I/O	I/O	I/O	VCC	NC[1]	**AA**
AB	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	**AB**
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

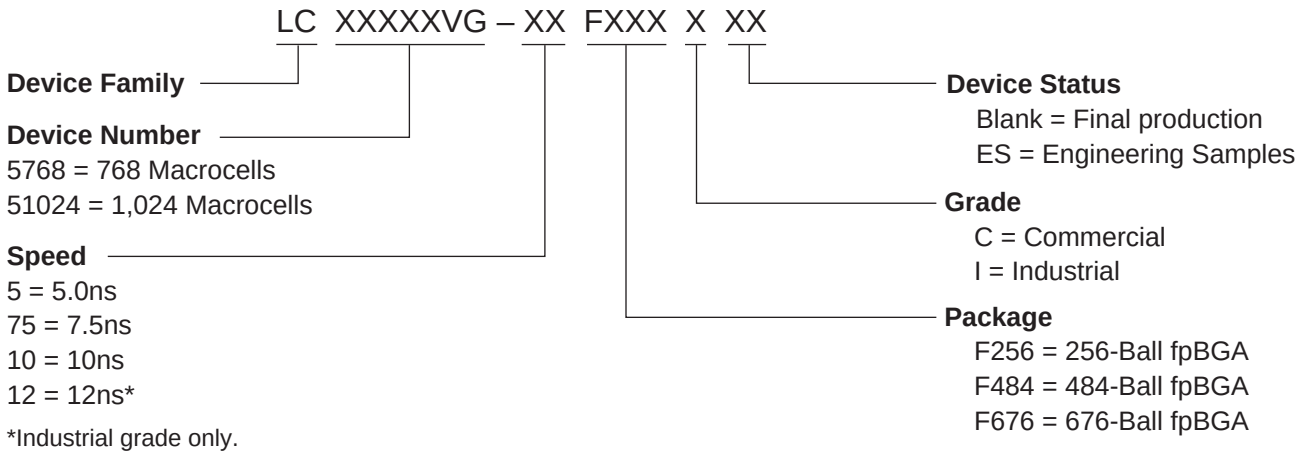
ispMACH 5768VG and 51024VG 484BGA/51024VG

Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/ispm5vg

Ordering Information

Commercial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-5F484C	fpBGA	484	1024	5	3.3
LC51024VG-75F484C	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484C	fpBGA	484	1024	10	3.3
LC51024VG-5F676C	fpBGA	676	1024	5	3.3
LC51024VG-75F676C	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676C	fpBGA	676	1024	10	3.3
LC5768VG-5F256C	fpBGA	256	768	5	3.3
LC5768VG-75F256C	fpBGA	256	768	7.5	3.3
LC5768VG-10F256C	fpBGA	256	768	10	3.3
LC5768VG-5F484C	fpBGA	484	768	5	3.3
LC5768VG-75F484C	fpBGA	484	768	7.5	3.3
LC5768VG-10F484C	fpBGA	484	768	10	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).