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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	24
Number of Macrocells	768
Number of Gates	-
Number of I/O	304
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	484-BBGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lc5768vg-75f484i

The ispMACH5000VG devices also contain sysCLOCK Phase Locked Loops (PLLs) that provide designers with increased clocking flexibility. The PLLs can be used to synthesize new clocks for use on-chip or elsewhere within the system. They can also be used to deskew clocks, again both at the chip and system levels. A variable delay line capability further improves this and allows designers to retard or advance the clock in order to tune set-up and clock-to-out times for optimal results. The ispMACH 5000VG Family Selection Guide (Table 1) details the key attributes and packages for the ispMACH 5000VG devices.

ispMACH 5000VG Architecture

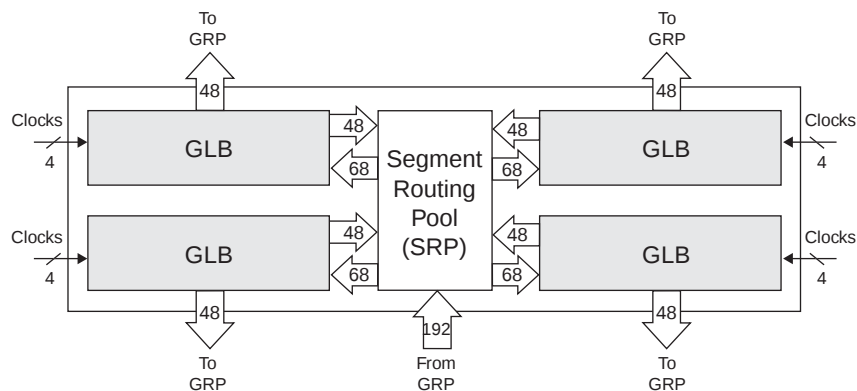
The ispMACH 5000VG Family of In-System Programmable High Density Logic Devices is based on segments containing four Generic Logic Blocks (GLBs) and a hierarchical routing pool (GRP) structure interconnecting the segments. A segment routing pool (SRP) connects each GLB in a segment allowing the maximum flexibility and speed.

Outputs from the GLBs drive the Segment Routing Pool (SRP) and the Global Routing Pool (GRP). Enhanced switching resources are provided to allow signals in the Segment Routing Pool to drive any or all the GLBs in the segment. Optimal switching is provided to allow all signals in the Global Routing Pool to be routed to any or all SRPs. This mechanism allows fast, efficient connections across the entire device.

Segment

Each segment contains four GLBs and a segment routing pool (SRP). Each GLB has 32 internal feedback outputs and 16 external feedback outputs, for a total of 48 outputs from each GLB feeding the SRP. The SRP contains up to 384 signals, 48 from each GLB and 192 from the GRP, with full routing capability. This routing scheme maximizes the flexibility and speed of the device without sacrificing the routing.

Figure 2. Segment



Generic Logic Block

Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and three control product terms. The GLB has 68 inputs from the Segment Routing Pool, which are available in both true and complement form for every product term. The three control product terms are used for shared reset, clock and output enable functions. Figure 3 shows the structure of the GLB from the macrocell perspective. This is referred to as a macrocell slice. There are 32 macrocell slices per GLB.

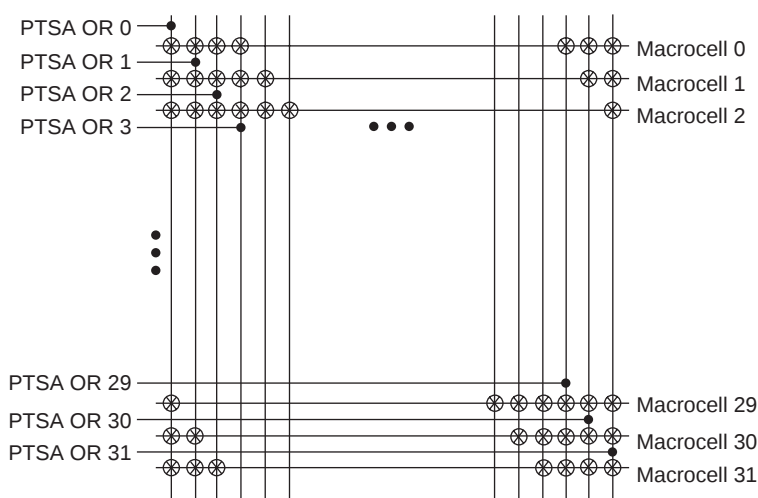
AND-Array

The programmable AND-Array consists of 68 inputs and 163 output product terms. The 68 inputs from the SRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 163 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining three control product terms feeding the Shared PT Clock, Shared PT Reset and Shared PT OE. Every set of five product terms from the 160 logic product terms forms a product term cluster start-

Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Figure 6 shows the graphical representation of the PTSA.

Figure 6. Product Term Sharing Array

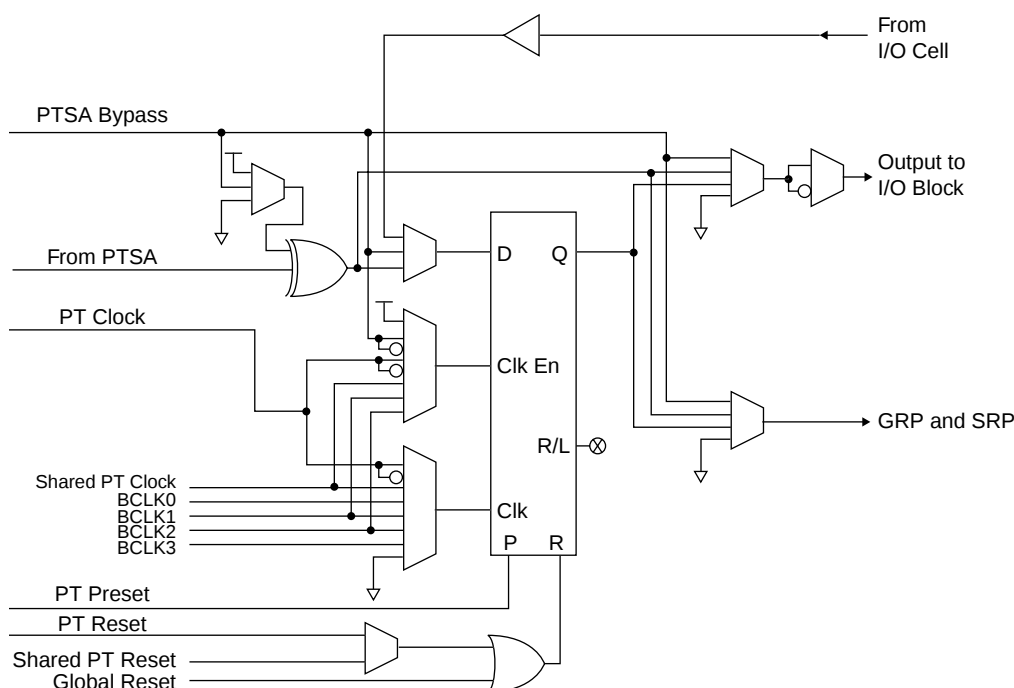


Macrocell

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation.

The macrocells each have two outputs, which can be fed to the SRP, GRP and I/O cell. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 7 is a graphical representation of the ispMACH 5000VG macrocell.

Figure 7. Macrocell

I/O Cell

The I/O cell of the ispMACH 5000VG device provides a high degree of flexibility. It includes the sysIO feature and an enhanced output enable MUX for optimal performance both on- and off-chip. The sysIO feature allows I/O cells to be configured to different I/O standards, drive strengths and slew rates. The enhanced output enable MUX provides up to 14 different output enable choices per I/O cell.

The I/O cell contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, a programmable pull-up resistor, a programmable pull-down resistor and a programmable bus-keeper latch. The I/O cell receives its input from its associated macrocell. The I/O cell has a feedback line to its associated macrocell and a direct path to the GRP and SRP.

The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four Shared PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes.

The four shared PTOE signals are derived from PT163 of each GLB in the segment. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 8 is a graphical representation of the I/O cell.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 5000VG devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispMACH 5000VG family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 5000VG devices provide In-System Programming (ISP™) capability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The ispMACH 5000VG devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 5000VG devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 5000VG devices during the testing of a circuit board.

Security Bit

A programmable security bit is provided on the ispMACH 5000VG devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary design from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Hot Socketing

The ispMACH 5000VG devices are well suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Density Migration

The ispMACH 5000 family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units	
I _{IL} , I _{IH} ¹	Input or I/O Leakage Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	+/-10	μA	
I _{PU} ²	I/O Weak Pull-up Resistor Current	V _{CCO} = 3.3	-30	—	-150	μA	
		V _{CCO} = 2.5	-20	—	-150	μA	
		V _{CCO} = 1.8	-10	—	-150	μA	
I _{PD} ²	I/O Weak Pull-down Resistor Current	V _{IL} (MAX) ≤ V _{IN} ≤ V _{IH} (MAX)	30	—	150	μA	
I _{BHLS} ²	Bus Hold Low Sustaining Current	V _{IN} = V _{IL} (MAX)	30	—	—	μA	
I _{BHHS} ²	Bus Hold High Sustaining Current	V _{IN} = 0.7 V _{CCO}	V _{CCO} = 3.3	-30	—	—	μA
		V _{CCO} = 2.5	-20	—	—	μA	
		V _{CCO} = 1.8	-10	—	—	μA	
I _{BHLO} ²	Bus Hold Low Overdrive Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	150	μA	
I _{BHHO} ²	Bus Hold High Overdrive Current	0V ≤ V _{IN} ≤ V _{IH} (MAX)	—	—	-150	μA	
I _{CC} ^{3, 4, 5}	Operating Power Supply Current	V _{CC} = 3.3V	—	380	—	mA	
V _{BHT}	Bus Hold Trip Points		V _{IL} (MAX)	—	V _{IH} (MIN)	V	
C ₁	I/O Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf	
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5					
C ₂	Clock Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf	
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5					
C ₃	Global Input Capacitance ³	V _{CC} = 3.3V, V _{IO} = 0 to V _{IH} (MAX)	—	10	—	pf	
		V _{CCO} = 3.3V, 2.5, 1.8, 1.5					

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.

2. Only available for LVCMOS and LVTTL standards.

3. $T_A = 25^\circ C$, $f = 1.0MHz$.

4. Device configured with 16-bit counters.

5. I_{CC} varies with specific device configuration and operating frequency.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}^2 (mA)	I_{OH}^2 (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3 ¹	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVTTTL	-0.3	0.8	2.0	5.5	0.4	2.4	20	-20
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	$V_{CCO} - 0.4$	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCO}$	$0.65V_{CCO}$	3.6	0.4	$V_{CCO} - 0.4$	12, 8, 5.33, 4	-12, -8, -5.33, -4
					0.2	$V_{CCO} - 0.2$	0.1	-0.1
PCI 3.3	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
PCI-X	-0.3	$0.35V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
AGP-1X	-0.3	$0.3V_{CCO}$	$0.5V_{CCO}$	3.6	$0.1V_{CCO}$	$0.9V_{CCO}$	1.5	-0.5
SSTL3 class I	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.7	$V_{CCO} - 1.1$	8	-8
SSTL3 class II	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.5	$V_{CCO} - 0.9$	16	-16
SSTL2 class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.54	$V_{CCO} - 0.62$	7.6	-7.6
SSTL2 class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	3.6	0.35	$V_{CCO} - 0.43$	15.2	-15.2
CTT 3.3	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
CTT 2.5	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	-8
HSTL class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	-8
HSTL class III	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	-8
GTL+	-0.3	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.6	n/a	36	n/a

1. Software default setting

2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed 96mA.

sysIO Differential Input DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max
$V_{INP} \cdot V_{INM}$	LVDS Input voltage	—	0	2.4
V_{THD}	LVDS Differential input threshold	—	$\pm 100\text{mV}$	—
V_{IL}	LVPECL Input Voltage Low	$V_{CC} = 3.0 \text{ to } 3.6\text{V}$	$V_{CC} - 1.81$	$V_{CC} - 1.48$
		$V_{CC} = 3.3\text{V}$	1.49V	1.83V
V_{IH}	LVPECL Input Voltage High	$V_{CC} = 3.0 \text{ to } 3.6\text{V}$	$V_{CC} - 1.17$	$V_{CC} - 0.88$
		$V_{CC} = 3.3\text{V}$	2.14V	2.42V

ispMACH 51024VG External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description ^{1,2,3}	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.0	—	7.5	—	10.0	—	12.0	ns
t_{PD_PTSA}	Data propagation delay, intrasegment path	—	6.0	—	9.0	—	11.5	—	13.5	ns
t_{PD_GLOBAL}	Data propagation delay, intersegment path	—	6.5	—	9.75	—	13.0	—	16.0	ns
t_S	GLB register setup time before clock, 5-PT bypass	3.0	—	5.0	—	7.5	—	9.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	3.0	—	6.0	—	8.5	—	10.0	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.8	—	3.0	—	4.0	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	GLB register hold time before clock, input reg. path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	4.4	—	5.0	—	6.0	—	7.0	ns
t_R	External reset pin to output delay	—	6.5	—	9.0	—	10.0	—	10.9	ns
t_{RW}	External reset pulse duration	4.0	—	6.0	—	8.0	—	9.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	7.0	—	9.75	—	11.5	—	13.4	ns
$t_{SPTOE/DIS}$	Input to output segment product term output enable/disable	—	8.0	—	11.25	—	17.5	—	20.4	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.2	—	7.5	—	8.85	—	10.0	ns
t_{CW}	Global clock width, high or low	1.6	—	2.75	—	3.6	—	4.3	—	ns
t_{GW}	Global gate width low (for low transparent) or high (for high transparent)	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.75	—	3.6	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.25	—	0.35	—	0.45	—	0.55	ns
	Clock-to-out skew, segment level	—	0.4	—	0.5	—	0.6	—	0.7	ns
f_{MAX}^4	Clock frequency with internal feedback	178.6	—	117.0	—	87.0	—	73.0	—	MHz
$f_{MAX} (Ext.)$	Clock frequency with external feedback, $1/(t_{S_PTSA} + t_{CO})$	135.1	—	90.9	—	69.0	—	58.8	—	MHz
$f_{MAX} (Tog.)$	Clock frequency max Toggle	312.5	—	181.0	—	138.0	—	116.0	—	MHz

Timing v.1.10

1. Timing numbers are based on default LVCMOS 3.3 I/O Buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, assuming segment and global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

ispMACH 5768VG Internal Timing Parameters (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{BSR}	Block PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t _{PTSR}	Macrocell PT Set/Reset Delay	—	2.00	—	3.00	—	4.00	—	4.80	ns
t _{SPTOE}	Segment PT OE Delay	—	2.40	—	3.60	—	7.75	—	9.10	ns
t _{POTOE}	Macrocell PT OE Delay	—	1.40	—	2.10	—	1.75	—	2.10	ns

Notes:

Timing v.1.20

1. Internal Timing Parameters are not tested and are for reference only. Refer to Timing Model in this data sheet for further details.
2. t_{PLL_DELAY} is the unit increment by which the clock signal can be incremented. The PLL can adjust the clock signal by up to 3.5ns in either direction in units of 0.5ns for each step.

ispMACH 51024VG Internal Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5		-75		-10		-12		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
In/Out Delays										
t _{IN}	Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t _{GCLK_IN}	Global Clock Input Buffer Delay	—	0.65	—	0.95	—	1.25	—	1.40	ns
t _{GOE}	Global OE Pin Delay	—	4.05	—	5.00	—	6.00	—	7.00	ns
t _{BUF}	Delay through Output Buffer	—	1.15	—	1.50	—	1.75	—	1.90	ns
t _{EN}	Output Enable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t _{DIS}	Output Disable Time	—	2.15	—	2.50	—	2.85	—	3.00	ns
t _{RSTb}	Global RESETbar Pin Delay	—	4.60	—	6.50	—	7.00	—	7.50	ns
Routing Delays										
t _{ROUTE}	Delay through SRP	—	2.80	—	4.20	—	5.65	—	6.90	ns
t _{PTSA}	Product Term Sharing Array Delay	—	0.40	—	1.85	—	2.35	—	2.50	ns
t _{PDB}	5-PT Bypass Propagation Delay	—	0.40	—	0.85	—	1.35	—	1.80	ns
t _{PDi}	Macrocell Propagation Delay	—	1.00	—	0.50	—	0.50	—	0.80	ns
t _{INREG}	Input Buffer to Macrocell Register Delay	—	3.00	—	3.05	—	3.50	—	4.40	ns
t _{FBK}	Internal Feedback Delay	—	0.00	—	0.00	—	0.00	—	0.00	ns
t _{GCLK}	Global Clock Tree Delay	—	0.85	—	0.70	—	0.55	—	0.65	ns
t _{PLL_DELAY}	Programmable PLL Delay Increment	—	0.50	—	0.50	—	0.50	—	0.50	ns
t _{PLL_SEC_DELAY}	Additional Delay When Using Secondary PLL Output	—	0.60	—	0.60	—	0.60	—	0.60	ns
t _{GRP}	Global Routing Pool Delay	—	1.50	—	2.25	—	3.00	—	4.00	ns
Register/Latch Delays										
t _S	D-Register Setup Time	0.65	—	0.65	—	1.05	—	1.25	—	ns
t _{S_PT}	D-Register Setup Time with PT Clock	0.65	—	0.65	—	1.05	—	1.25	—	ns
t _H	D-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{ST}	T-Register Setup Time	1.15	—	1.15	—	1.55	—	1.75	—	ns
t _{ST_PT}	T-Register Setup Time with PT Clock	1.15	—	1.15	—	1.55	—	1.75	—	ns
t _{HT}	T-Register Hold Time	0.00	—	0.00	—	0.00	—	0.00	—	ns
t _{COi}	Register Clock to Output/Feedback MUX Time	—	1.75	—	1.85	—	2.45	—	3.05	ns

ispMACH 5768VG Timing Adders (Continued)

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
HSTL_III_out	t_{BUF} , t_{EN} , t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF} , t_{EN} , t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.20

ispMACH 51024VG Timing Adders

Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLA}	t_{ROUTE}	GLB Loading Adder	—	0.0	—	0.0	—	0.0	—	0.0	ns
t_{EXP}	t_{PTSA}	PT Expander Adder	—	1.5	—	2.0	—	2.5	—	2.5	ns
t_{LP}	t_{ROUTE}	Low Power Adder	—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{OI} Input Adders											
LVCMOS18_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS1.8 standard	—	0.90	—	0.90	—	0.90	—	0.90	ns
LVCMOS25_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
LVCMOS33_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVCMOS3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
LVTTL	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using LVTTL standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using PCI standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
PCI_X_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using PCI_X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using AGP-1X standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL3_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL3_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL3_II_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL3_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL2_I standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
SSTL2_II_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using SSTL2_II standard	—	1.00	—	1.00	—	1.00	—	1.00	ns
CTT33_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using CTT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using CTT2.5 standard	—	0.15	—	0.15	—	0.15	—	0.15	ns
HSTL_I_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using HSTL_I standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
HSTL_III_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using HSTL_III standard	—	1.25	—	1.25	—	1.25	—	1.25	ns
GTL+_in	t_{IN} , t_{GCLK_IN} , t_{RSTb} , t_{GOE}	Using GTL+ standard	—	1.50	—	1.50	—	1.50	—	1.50	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

ispMACH 51024VG Timing Adders (Continued)

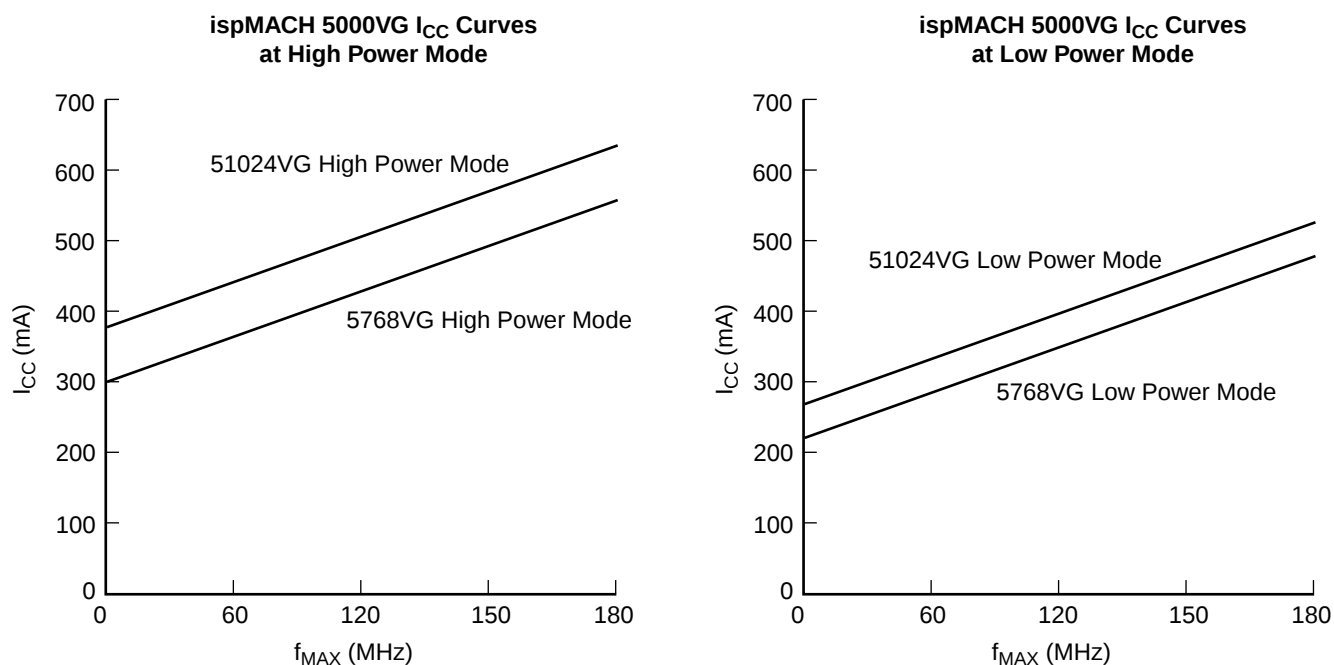
Adder Type	Base Parameter	Description	-5		-75		-10		-12		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
SSTL2_I_out	t_{BUF} t_{EN} , t_{DIS}	Using SSTL2_I standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
SSTL2_II_out	t_{BUF} t_{EN} , t_{DIS}	Using SSTL2_II standard	—	-0.25	—	-0.25	—	-0.25	—	-0.25	ns
CTT33_out	t_{BUF} t_{EN} , t_{DIS}	Using CCT3.3 standard	—	0.0	—	0.0	—	0.0	—	0.0	ns
CTT25_out	t_{BUF} t_{EN} , t_{DIS}	Using CCT2.5 standard	—	0.25	—	0.25	—	0.25	—	0.25	ns
HSTL_I_out	t_{BUF} t_{EN} , t_{DIS}	Using HSTL_I standard	—	-0.30	—	-0.30	—	-0.30	—	-0.30	ns
HSTL_III_out	t_{BUF} t_{EN} , t_{DIS}	Using HSTL_III standard	—	0.00	—	0.00	—	0.00	—	0.00	ns
GTL+_out	t_{BUF} t_{EN} , t_{DIS}	Using GTL+ standard	—	0.30	—	0.30	—	0.30	—	0.30	ns

Note: Open drain timing is the same as corresponding LVCMOS timing.

Timing v.1.10

Power Consumption

ispMACH 5000VG Typical Power vs. Frequency



Note: The devices are configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V, 25° C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	I_{DC} (mA)	I_{DCO} (mA)
ispMACH 5768VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	65	20
ispMACH 51024VG	0.0014	0.0014	0.054	1.5	0.152	0.105	5.0	80	20

Note: For further information about the use of these coefficients, refer to Technical Note TN1002, *Power Estimation in ispMACH 5000VG Devices*.

K0 = average current per product term in high power/MHz

K1 = average current per product term in low power/MHz

K2 = average current per GRP line/MHz

K3 = average current per PLL/MHz

K4 = DC current per product terms in high power

K5 = DC current per product terms in low power

K6 = Static DC current per PLL

I_{DC} = Static device current with all product terms powered off

I_{DCO} = Static I/O bank current

I_{CC} estimates are based on typical conditions ($V_{CC} = 3.3V$, room temperature) and an assumption of one GLB load on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

ispMACH 5768VG Power Supply and NC Connections¹

Signal	256-Ball fpBGA ²	484-Ball fpBGA ²
V _{CC}	F8, F9, H6, H11, J6, J11, L8, L9	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6
V _{CCO0}	C3, C7, G3	B5, D7, E2, E6, E9, F5, G4, J5
V _{CCO1}	K3, P3, P7	P5, U5, V6, V9, Y3
V _{CCO2}	K14, P10, P14	P18, U18, V14, V17, Y20
V _{CCO3}	C10, C14, G14	B18, D16, E14, E17, E21, F18, G19, J18
V _{CCP0}	H1	L7
V _{CCP1}	H16	N18
V _{CCJ}	J1	P4
V _{REF0}	E7	A9
V _{REF1}	M7	AA10
V _{REF2}	R13	AA13
V _{REF3}	A8	A15
GND PLL 0	H7	L6
GND PLL 1	J10	L16
GND	A1, C5, C12, E3, E14, G7, G8, G9, G10, H8, H9, H10, J7, J8, J9, K7, K8, K9, K10, M3, M14, P5, P12	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22
NC ³	—	AA1

1. All grounds must be electrically connected at the board level.

2. Not all grounds internally connected within the device.

3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 51024 Power Supply and NC Connections¹

Signal	484-Ball fpBGA ²	676-Ball fpBGA ²
V _{CC}	B17, B2, B21, B6, C14, C9, E18, E5, F2, F21, J20, J3, P20, P3, U2, U21, Y14, Y9, AA17, AA2, AA21, AA6	B29, D6, D10, D12, D19, D21, D25, F4, F27, K4, K27, M4, M27, W4, W27, AA4, AA27, AE4, AE27, AG6, AG10, AG12, AG19, AG21, AG25, AJ2
V _{CCO0}	B5, D7, E2, E6, E9, F5, G4, J5	E5, E7, E9, E11, F10, G5, J5, K6, L5
V _{CCO1}	P5, U5, V6, V9, Y3	Y5, AA6, AB5, AD5, AE10, AF5, AF7, AF9, AF11
V _{CCO2}	P18, U18, V14, V17, Y20	Y26, AA25, AB26, AD26, AE21, AF20, AF22, AF24, AF26
V _{CCO3}	B18, D16, E14, E17, E21, F18, G19, J18	E20, E22, E24, E26, F21, G26, J26, K25, L26
V _{CCP0}	L7	P5
V _{CCP1}	N18	N26
V _{CCJ}	P4	U6
V _{REF0}	A9	C11
V _{REF1}	AA10	AK10
V _{REF2}	AA13	AJ21
V _{REF3}	A15	E19
GND PLL 0	L6	R6
GND PLL 1	L16	P25
GND	A1, A22, C3, C20, D4, D19, E7, E16, G5, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G18, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, K7, K8, K9, K10, K11, K12, K13, K14, K15, K16, L8, L9, L10, L11, L12, L13, L14, L15, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, T4, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T19, W7, W16, AB1, AB22	A1, A30, B2, C3, C28, D8, D23, F7, F9, F11, F12, F19, F20, F22, F24, G6, G25, H4, H27, J6, J25, L6, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L25, M6, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M25, N11, N12, N13, N14, N15, N16, N17, N18, N19, N20, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, T11, T12, T13, T14, T15, T16, T17, T18, T19, T20, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, W6, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W25, Y6, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y25, AB6, AB25, AC4, AC27, AD6, AD25, AE7, AE9, AE11, AE12, AE19, AE20, AE22, AE24, AG8, AG23, AH3, AH28, AK1, AK30
NC ³	AA1	A14, A15, A16, A17, B14, B15, B16, B17, C13, C14, C15, C16, C17, C18, D13, D14, D15, D16, D17, D18, E13, E14, E15, E16, E17, E18, F13, F14, F15, F16, F17, F18, AE13, AE14, AE15, AE16, AE17, AE18, AF13, AF14, AF15, AF16, AF17, AF18, AG13, AG14, AG15, AG16, AG17, AG18, AH14, AH15, AH16, AH17, AH18, AJ14, AJ15, AJ16, AJ17, AJ18, AK14, AK15, AK16, AK17

1. All grounds must be electrically connected at the board level.
2. Not all grounds internally connected within the device.
3. NC pins are not to be connected to any active signals, VCC or GND.

ispMACH 5768VG Logic Signal Connections

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0C-30	C8	D11
0	0C-28	B6	B11
0	0C-26	A5	E12
0	0C-24	D8	C11
0	0C-22	E8	F12
0	0C-20	B5	B10
0	GNDIO0	GND	GND
0	0C-18	A4	A10
0	0C-16	D7	D10
0	0C-14/VREF0	E7	A9
0	0C-12	C6	E11
0	0C-10	B4	B9
0	0C-8	A3	F11
0	0C-6	NC	A8
0	0C-4	NC	C10
0	0C-2	NC	A7
0	0C-0	NC	E10
0	0D-30	NC	B8
0	0D-28	NC	C8
0	GNDIO0	GND	GND
0	0D-26	NC	F10
0	0D-24	NC	A6
0	0D-22	NC	F9
0	0D-20	NC	C7
0	0D-18	NC	D9
0	0D-16	NC	B7
0	0D-14	D6	E8
0	0D-12	E6	A5
0	0D-10	A2	F8
0	0D-8	B3	C6
0	0D-6	C4	D8
0	0D-4	D5	A3
0	GNDIO0	GND	GND
0	0D-2	NC	A2
0	0D-0	NC	A4
0	0A-0	NC	F7
0	0A-2	NC	C5
0	0A-4	NC	F6
0	0A-6	NC	B3
0	0A-8	NC	NC
0	0A-10	NC	NC
0	GNDIO0	GND	GND
0	0A-12	NC	NC

Bank No.	Signal	256 fpBGA	484 fpBGA
0	0A-14	NC	NC
0	0A-16	NC	B4
0	0A-18	NC	D5
0	0A-20	NC	B1
0	0A-22	NC	D6
0	0A-24	NC	C4
0	0A-26	NC	E4
0	GNDIO0	GND	GND
0	0A-28	B2	C2
0	0A-30	B1	C1
0	0B-30	C2	D1
0	0B-28	C1	D2
0	0B-26	NC	D3
0	0B-24	NC	E1
0	0B-22	NC	E3
0	0B-20	NC	F4
0	0B-18	NC	F1
0	0B-16	NC	F3
0	0B-14	NC	G6
0	0B-12	NC	G1
0	GNDIO0	GND	GND
0	0B-10	NC	G2
0	0B-8	NC	H1
0	0B-6	NC	G3
0	0B-4	NC	H2
0	0B-2	NC	H5
0	0B-0	NC	H6
0	1A-0	F7	J1
0	1A-2	F6	K1
0	1A-4	E5	H3
0	1A-6	D4	J2
0	1A-8	D3	H4
0	1A-10	D2	K2
0	GNDIO0	GND	GND
0	1A-12	D1	J6
0	1A-14	E4	L1
0	1A-16	NC	K3
0	1A-18	NC	J4
0	1A-20	NC	L2
0	1A-22	NC	M1
0	1A-24	NC	K6
0	1A-26	NC	K4
0	1A-28	NC	L3

ispMACH 5768VG Logic Signal Connections (Continued)

Bank No.	Signal	256 fpBGA	484 fpBGA
3	5C-20	C9	A13
3	5C-22	E9	B12
3	5C-24	D9	C13
3	5C-26	B8	A12
3	5C-28	A6	C12
3	5C-30	B7	A11
—	GCLK0	H4	P6
—	GCLK1	J4	R6
—	GCLK2	H14	P17
—	GCLK3	H13	P19
—	GOE0	J15	R18
—	GOE1	H15	R17
—	RESETB	J14	R19
—	TCK	J3	R3
—	TDI	H3	R2
—	TDO	J2	R4
—	TMS	H2	T1
—	TOE	J13	T18

ispMACH 51024VG Logic Signal Connections

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0C-30	D11	A13
0	0C-28	B11	B13
0	0C-26	E12	A12
0	0C-24	C11	B12
0	0C-22	F12	C12
0	0C-20	B10	A11
0	GNDIO0	GND	GND
0	0C-18	A10	B11
0	0C-16	D10	A10
0	0C-14/VREF0	A9	C11
0	0C-12	E11	E12
0	0C-10	B9	B10
0	0C-8	F11	D11
0	0C-6	A8	A9
0	0C-4	C10	C10
0	0C-2	A7	B9
0	0C-0	E10	A8
0	0D-30	B8	C9
0	0D-28	C8	B8
0	GNDIO0	GND	GND
0	0D-26	F10	E10
0	0D-24	A6	A7
0	0D-22	F9	D9
0	0D-20	C7	C8
0	0D-18	D9	B7
0	0D-16	B7	A6
0	0D-14	E8	C7
0	0D-12	A5	B6
0	0D-10	F8	A5
0	0D-8	C6	C6
0	0D-6	D8	D7
0	0D-4	A3	E8
0	GNDIO0	GND	GND
0	0D-2	A2	B5
0	0D-0	A4	A4
0	0A-0	F7	A3
0	0A-2	C5	B4
0	0A-4	F6	C5
0	0A-6	B3	F8
0	0A-8	NC	A2
0	0A-10	NC	B3
0	GNDIO0	GND	GND
0	0A-12	NC	C4

Bank No.	Signal	484 fpBGA	676 fpBGA
0	0A-14	NC	D5
0	0A-16	B4	E6
0	0A-18	D5	D4
0	0A-20	B1	B1
0	0A-22	D6	C2
0	0A-24	C4	F6
0	0A-26	E4	D3
0	GNDIO0	GND	GND
0	0A-28	C2	E4
0	0A-30	C1	F5
0	0B-30	D1	C1
0	0B-28	D2	D2
0	0B-26	D3	E3
0	0B-24	E1	D1
0	0B-22	E3	E2
0	0B-20	F4	H6
0	0B-18	F1	F3
0	0B-16	F3	E1
0	0B-14	G6	G4
0	0B-12	G1	F2
0	GNDIO0	GND	GND
0	0B-10	G2	H5
0	0B-8	H1	G3
0	0B-6	G3	F1
0	0B-4	H2	G2
0	0B-2	H5	H3
0	0B-0	H6	G1
0	1A-0	J1	H2
0	1A-2	K1	J4
0	1A-4	H3	H1
0	1A-6	J2	J3
0	1A-8	H4	K5
0	1A-10	K2	J2
0	GNDIO0	GND	GND
0	1A-12	J6	J1
0	1A-14	L1	K3
0	1A-16	K3	K2
0	1A-18	J4	K1
0	1A-20	L2	L4
0	1A-22	M1	L3
0	1A-24	K6	L2
0	1A-26	K4	M5
0	1A-28	L3	L1

Signal Configuration

ispMACH 5768VG 256-ball fpBGA

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF3	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	I/O	I/O	I/O	I/O	I/O/ CLK_OUT1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	B
C	I/O	I/O	VCCO3	I/O	GND	I/O	VCCO3	I/O	I/O	VCCO0	I/O	GND	I/O	VCCO0	I/O	I/O	C
D	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	D
E	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF0	I/O	I/O	I/O	GND	I/O	I/O	E
F	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ PLL_RST0	F
G	I/O	I/O/ PLL_FBK1	VCCO3	I/O	I/O	I/O	GND	GND	GND	GND	I/O/ CLK_OUT0	I/O	I/O	VCCO0	I/O/ PLL_FBK0	I/O	G
H	VCCP1	GOE1	GCLK2	GCLK3	I/O/ PLL_RST1	VCC	GND	GND	GND	GNDP0	VCC	I/O	GCLK0	TDI	TMS	VCCP0	H
J	I/O	GOE0	RESETB	TOE	I/O	VCC	GNDP1	GND	GND	GND	VCC	I/O	GCLK1	TCK	TDO	VCCJ	J
K	I/O	I/O	VCCO2	I/O	I/O	I/O	GND	GND	GND	GND	I/O	I/O	I/O	VCCO1	I/O	I/O	K
L	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	L
M	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O/ VREF1	I/O	I/O	I/O	GND	I/O	I/O	M
N	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	N
P	I/O	I/O	VCCO2	I/O	GND	I/O	VCCO2	I/O	I/O	VCCO1	I/O	GND	I/O	VCCO1	I/O	I/O	P
R	I/O	I/O	I/O	I/O/ VREF2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	R
T	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	T
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 5768VG

256fpBGA/5768VG

Bottom View

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispMACH 5768VG and 51024VG 484-ball fpBGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O / VREF3	I/O	I/O	I/O	I/O	I/O	I/O / VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	A
B	I/O	VCC	I/O	I/O	VCC03	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	VCC00	I/O	I/O	VCC	I/O	B
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	C
D	I/O	I/O	I/O	GND	I/O	I/O	VCC03	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC00	I/O	I/O	GND	I/O	I/O	I/O	D
E	I/O	VCC03	I/O	I/O	VCC	VCC03	GND	I/O	VCC03	I/O	I/O	I/O	I/O	VCC00	I/O	GND	VCC00	VCC	I/O	I/O	VCC00	I/O	E
F	I/O	VCC	I/O	I/O	VCC03	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC00	I/O	I/O	VCC	I/O	F
G	I/O	I/O	I/O	VCC03	GND	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	GND	VCC00	I/O	I/O	I/O	G
H	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	H
J	I/O	I/O	VCC	I/O	VCC03	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	VCC00	I/O	VCC	I/O	I/O	J
K	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O	I/O	I/O	I/O	K
L	I/O	I/O	I/O / CLK_OUT1	I/O	I/O	I/O	GNDP1	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCCP0	GNDP0	I/O	I/O	I/O	I/O	L
M	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O / PLL_RST0	I/O	I/O	I/O	M
N	I/O	I/O	I/O / PLL_RST1	I/O	VCCP1	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	I/O / PLL_FBK0	I/O	I/O	I/O / CLK_OUT0	N
P	I/O	I/O / PLL_FBK1	VCC	GCLK3	VCC02	GCLK2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK0	VCC01	VCCJ	VCC	I/O	I/O	P
R	I/O	I/O	I/O	RESETB	GOE0	GOE1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GCLK1	I/O	TDO	TCK	TDI	I/O	R
T	I/O	I/O	I/O	GND	TOE	I/O	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I/O	I/O	GND	I/O	I/O	TMS	T
U	I/O	VCC	I/O	I/O	VCC02	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC01	I/O	I/O	VCC	I/O	U
V	I/O	I/O	I/O	I/O	I/O	VCC02	I/O	I/O	VCC02	I/O	I/O	I/O	I/O	VCC01	I/O	I/O	VCC01	I/O	I/O	I/O	I/O	I/O	V
W	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	W
Y	I/O	I/O	VCC02	I/O	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	VCC01	I/O	I/O	Y
AA	I/O	VCC	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O / VREF2	I/O	I/O	I/O / VREF1	I/O	I/O	I/O	VCC	I/O	I/O	I/O	VCC	NC ¹	AA
AB	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	AB
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispMACH 5768VG and 51024VG

484BGA/51024VG

Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Signal Configuration

ispMACH 51024VG 676-ball fpBGA

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
A	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	A	
B	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	B	
C	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O/VREF0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	C	
D	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	D	
E	I/O	I/O	I/O	I/O	VCC03	I/O	VCC03	I/O	VCC03	I/O	VCC03	I/O/VREF3	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	VCC00	I/O	VCC00	I/O	VCC00	I/O	VCC00	I/O	I/O	I/O	I/O	I/O	E
F	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCC03	GND	GND	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	GND	GND	VCC00	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	I/O	F
G	I/O	I/O	I/O	I/O	VCC03	GND																	GND	VCC00	I/O	I/O	I/O	I/O	G			
H	I/O	I/O	I/O	GND	I/O	I/O																	I/O	I/O	GND	I/O	I/O	I/O	H			
J	I/O	I/O	I/O	I/O	VCC03	GND																	GND	VCC00	I/O	I/O	I/O	I/O	J			
K	I/O	I/O	I/O	VCC	I/O	VCC03																	VCC00	I/O	VCC	I/O	I/O	I/O	K			
L	I/O	I/O	I/O	I/O	VCC03	GND																	GND	VCC00	I/O	I/O	I/O	I/O	L			
M	I/O	I/O/CLK_OUT1	I/O	VCC	I/O	GND																	GND	I/O	VCC	I/O	I/O/CLK_OUT0	I/O	M			
N	I/O	I/O	I/O	I/O	VCCP1	I/O																	I/O	I/O	I/O	I/O	I/O	I/O	N			
P	I/O	I/O	I/O	I/O	GCLK3	GNDP1																	I/O	VCCP0	I/O	I/O	I/O	I/O/PLL_RST0	P			
R	I/O	I/O	I/O/PLL_RST1	I/O/PLL_FBK1	GOE1	GCLK2																	GNDP0	GCLK0	I/O/PLL_FBK0	I/O	I/O	I/O	R			
T	I/O	I/O	I/O	I/O	GOE0	RESETB																	GCLK1	TDI	TMS	I/O	I/O	I/O	T			
U	I/O	I/O	I/O	I/O	TOE	I/O																	VCCJ	TCK	I/O	I/O	I/O	I/O	U			
V	I/O	I/O	I/O	I/O	I/O	I/O																	I/O	TDO	I/O	I/O	I/O	I/O	V			
W	I/O	I/O	I/O	VCC	I/O	GND																	GND	I/O	VCC	I/O	I/O	I/O	W			
Y	I/O	I/O	I/O	I/O	VCC02	GND																	GND	VCC01	I/O	I/O	I/O	I/O	Y			
AA	I/O	I/O	I/O	VCC	I/O	VCC02																	VCC01	I/O	VCC	I/O	I/O	I/O	AA			
AB	I/O	I/O	I/O	I/O	VCC02	GND																	GND	VCC01	I/O	I/O	I/O	I/O	AB			
AC	I/O	I/O	I/O	GND	I/O	I/O																	I/O	I/O	GND	I/O	I/O	I/O	AC			
AD	I/O	I/O	I/O	I/O	VCC02	GND																	GND	VCC01	I/O	I/O	I/O	I/O	AD			
AE	I/O	I/O	I/O	VCC	I/O	I/O	GND	I/O	GND	VCC02	GND	GND	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	GND	GND	VCC01	GND	I/O	GND	I/O	I/O	VCC	I/O	I/O	I/O	AE	
AF	I/O	I/O	I/O	I/O	VCC02	I/O	VCC02	I/O	VCC02	I/O	VCC02	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	VCC01	I/O	VCC01	I/O	VCC01	I/O	VCC01	I/O	I/O	I/O	I/O	AF	
AG	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	VCC	I/O	VCC	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	VCC	I/O	VCC	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	AG	
AH	I/O	I/O	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	I/O	I/O	AH	
AJ	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O/VREF2	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O	AJ
AK	GND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC ¹	NC ¹	NC ¹	NC ¹	I/O	I/O	I/O	I/O/VREF1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	GND	AK	
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		

ispMACH 51024VG

Bottom View

ispMACH 51024VG

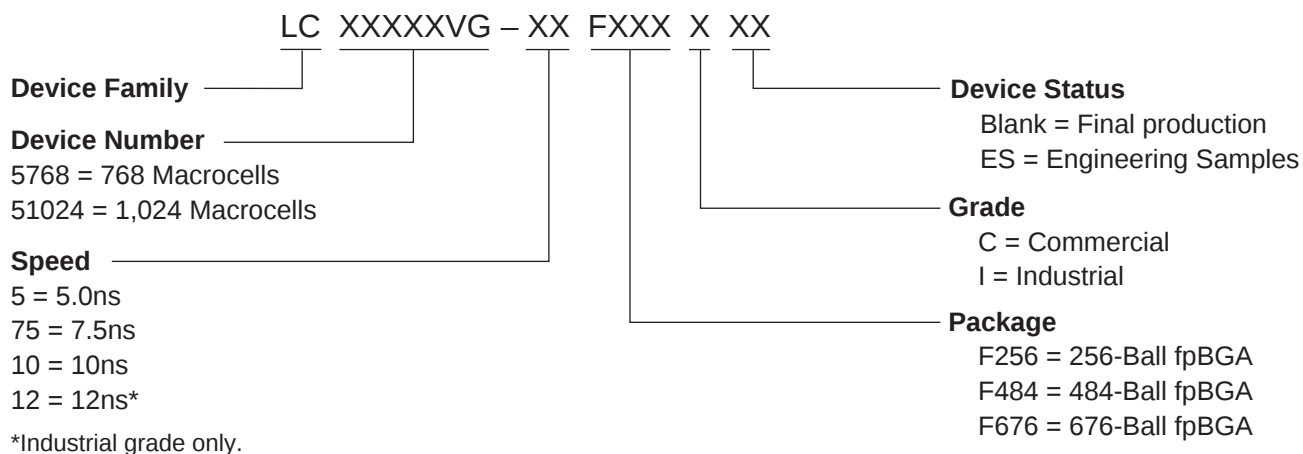
Bottom View

676BGA/51024VG

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/ispM5vg

Ordering Information

Commercial

Part Number	Package	Pin Count	Macrocells	Tpd	Voltage
LC51024VG-5F484C	fpBGA	484	1024	5	3.3
LC51024VG-75F484C	fpBGA	484	1024	7.5	3.3
LC51024VG-10F484C	fpBGA	484	1024	10	3.3
LC51024VG-5F676C	fpBGA	676	1024	5	3.3
LC51024VG-75F676C	fpBGA	676	1024	7.5	3.3
LC51024VG-10F676C	fpBGA	676	1024	10	3.3
LC5768VG-5F256C	fpBGA	256	768	5	3.3
LC5768VG-75F256C	fpBGA	256	768	7.5	3.3
LC5768VG-10F256C	fpBGA	256	768	10	3.3
LC5768VG-5F484C	fpBGA	484	768	5	3.3
LC5768VG-75F484C	fpBGA	484	768	7.5	3.3
LC5768VG-10F484C	fpBGA	484	768	10	3.3

Note: the ispMACH 5000VG family is dual-marked with both Commercial and Industrial grades. The Commercial speed grade is one speed grade faster (i.e. LC51024VG-75F484C) than the Industrial speed grade (i.e. LC51024VG-10F484I).