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onsemi - LC88FC3K0AUTJ-2H Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	Xstormy16
Core Size	16-Bit
Speed	10MHz
Connectivity	I ² C, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	47.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc88fc3k0autj-2h

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Function Details

- Xstromy16 CPU
 - 4G-byte address space
 - General-purpose registers : 16 bits × 16 registers

Flash ROM

- 786432 × 8 bits
- Programming voltage level : 2.7 to 3.6V.
- Block-erasable in 2K byte units.
- Data written in 2-byte units.
- RAM
 - 48640 × 8 bits
- Minimum instruction cycle time (tCYC)
 100 ns (10 MHz), V_{DD} = 2.7 to 3.6V
- Ports
 - Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1 bit units : 86 (P0n P1n, P2n, P3n, P4n, P5n, P6n, P7n, PAn PB0 to PB6, PC2, PD0 to PD5)

: 4 (PC0, PC1, PC3, PC4)

: 8 (VSS1 to 4, VDD1 to 4)

: 1 (RESB)

: 1 (TEST)

- Oscillation/normal withstand voltage I/O ports
- Reset pins
- TEST pins
- Power pins

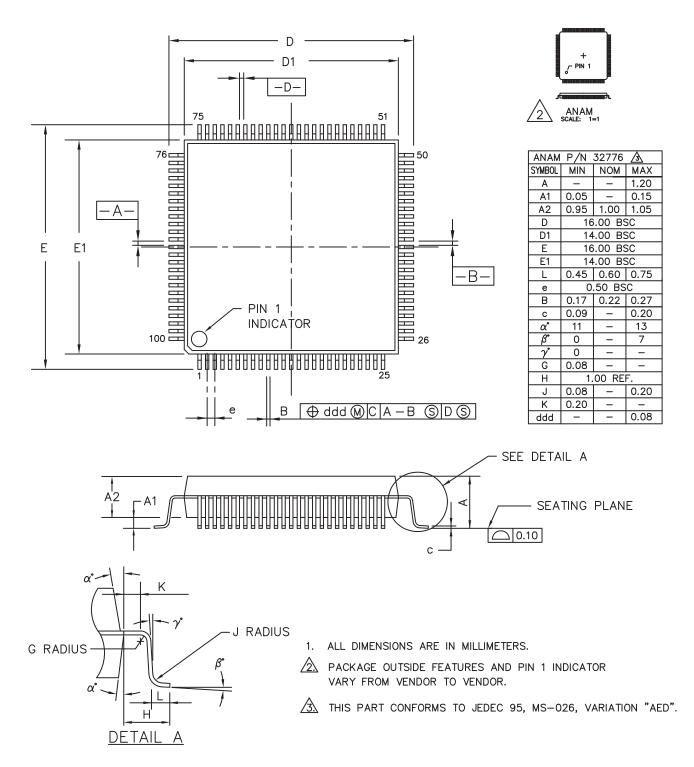
Timers

- Timer 0 : 16-bit timer that supports PWM/toggle outputs
 - <1> 5-bit prescaler
 - <2> 8-bit PWM \times 2, 8-bit timer + 8-bit PWM mode selectable
 - <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator.
- Timer 1 : 16-bit timer with capture registers
 - <1> 5-bit prescaler
 - <2> May be divided into 2 channels of 8-bit timer
 - <3> Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 2 : 16-bit timer with capture registers
 - <1>4-bit prescaler
 - <2> May be divided into 2 channels of 8-bit timer
 - <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3 : 16-bit timer that shpports PWM/toggle outputs
 - <1> 8-bit prescaler
 - <2> 8-bit timer× 2ch or 8-bit timer+8-bit PWM mode selectable
 - <3> Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4 : 16-bit timer that supports toggle outputs
- <1> Clock source selectable from system clock and prescaler 0
- Timer 5 : 16-bit timer that supports toggle output
 - <1> Clock source selectable from system clock and prescaler 0
- Timer 6 : 16-bit timer that supports toggle outputs
 - <1> Clock source selectable from system clock and prescaler 1
- Timer 7 : 16-bit timer that supports toggle output
 - ${<}1{>}\operatorname{Clock}$ source selectable from system clock and prescaler 1
 - *Prescaler 0 and 1 are consisted of 4bits and can choose their clock source from OSC0 or OSC1.
- Base timer
 - <1> Clock may be selected from OSC0 (32.768 kHz crystal oscillator) and frequency-divided output of system clock.
 - <2> Interrupts can be generated in 7 timing schemes.

- Real time clock
 - <1> Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leapyear calculation function.
 - <2> Consisted of Indipendent second-minuit-hour-day-month-yeare-century counters.
- Serial interfaces
 - SIO0 : 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
 - SIO1 : 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
 - SIO4 : 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
 - SMIIC0 : Single master I²C/8-bit synchronous SIO
 - Mode 0 : Single-master mode communication
 - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
 - SMIIC1 : Single master I²C/8-bit synchronous SIO Mode 0 : Single-master mode communication Mode 1 : Synchronous 8-bit serial I/O (MSB first)
 - SLIIC0 : Slave I²C/8-bit synchronous SIO
 - Mode $0 : I^2C$ slave mode communication
 - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
 - Note: usable only with the external clock source

Package Dimensions unit : mm

TQFP 100, 14x14 CASE 932AN-01 ISSUE O



Pin Description

Pin Name	I/O	Description
VSS1, VSS2,	_	– power sources
VSS3, VSS4		
VDD1, VDD2,	-	+ power sources
VDD3, VDD4		
Port 0	I/O	• 8-bit I/O port
P00 to P07		• I/O specifiable in 1-bit units
100 10 10,		• Pull-up resistors can be turned on and off in 1 bit units
		• HOLD release input (P00 to P03, P04, P05)
		• Port 0 interrupt input (P00 to P03, P04, P05)
		Pin functions
		P06 : Timer 0L output
		P07 : Timer 0L output/UART0 clock input
Port 1	I/O	• 8-bit I/O port
P10 to P17		• I/O specifiable in 1-bit units
110 00 11,		• Pull-up resistors can be turned on and off in 1 bit units
		Pin functions
		P10 : SIO0 data output
		P11 : SIO0 data input/pulse input/output
		P12 : SIO0 clock input/output
		P13 : UART0 transmit
		P14 : Timer 3L output/UART0 receive
		P15 : Timer 3H output
		P16 : UART2 receive
		P17 : UART2 transmit
Port 2	I/O	• 8-bit I/O port
P20 to P27		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions
		P20 : INT4 input/HOLD release input/timer 3 event input/
		timer 2L capture input/timer 2H capture input
		P21 : INT5 input/HOLD release input/timer 3 event input/
		timer 2L capture input/timer 2H capture input
		P22 : SMIIC0 clock input/output
		P23 : SMIIC0 bus input/output/data input
		P24 : SMIIC0 data output (used in 3-wire SIO mode)
		P25 : Timer 4 output
		P26 : Timer 5 output
		Interrupt acknowledge type
		INT4, INT5 : H level, L level, H edge, L edge, both edges

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Pin Name	I/O	Description
Port 3	I/O	• 8-bit I/O port
P30 to P37		• I/O specifiable in 1-bit units
150 10 157		• Pull-up resistors can be turned on and off in 1 bit units
		Pin functions
		P30 : INTO input/HOLD release/timer 2L capture input
		P31 : INT1 input/HOLD release/timer 2H capture input P32 : INT2 input/HOLD release/timer 2 event input/timer 2L capture input/
		Infrared Remote Controller Receiver input
		P33 : INT3 input/HOLD release/timer 2 event input/timer 2H capture input
		P34 : UART3 receive
		P35 : UART3 transmit
		P36 : Timer 6 output P37 : Timer 7 output
		Interrupt acknowledge type
		INTO to INT3 : H level, L level, H edge, L edge, both edges
Port 4	I/O	• 8-bit I/O port
P40 to P47		• I/O specifiable in 1-bit units
P40 to P47		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions
		P40 : INT6 input/HOLD release input
		P41 : INT7 input/HOLD release input
		P43 : SIO1 data output P44 : SIO1 data input/bus input/output
		P45 : SIO1 clock input/output
		P46 : PWM0A output
		P47 : PWM0Boutput
		Interrupt acknowledge type
		INT6, INT7 : H level, L level, H edge, L edge, both edges
Port 5	I/O	• 8-bit I/O port
P50 to P57		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units
		• HOLD release input
		Port 0 interrupt input
Port 6	I/O	• 8-bit I/O port
P60 to P67		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions ANO $(D(0))$ to ANZ $(D(7))$ AD convertes inset port
Dort 7	1/0	AN0 (P60) to AN7 (P67) : AD converter input port
Port 7	I/O	• 8-bit I/O port
P70 to P77		 I/O specifiable in 1-bit units Pull-up resistors can be turned on and off in 1 bit units
		• Puil-up resistors can be turned on and off in 1 bit units
		AN8 (P70) to AN15 (P77) : AD converter input port
		Ano (170) to Alvis (177). AD converter input polt

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Pin Name	I/O	Description
Port A	I/O	• 8-bit I/O port
PA0 to PA7		• I/O specifiable in 1-bit units
1110 to 1117		Pull-up resistors can be turned on and off in 1 bit units
		 Multiplexed pin functions
		PA0 : SIO4 data output
		PA1 : SIO4 data input/pulse input/output
		PA2 : SIO4 clock input/output
		PA3 : SIO4 chip select input
		PA4 : SLIIC0 clock input
		PA5 : SLIIC0 bus input/output/data input PA6 : SLIIC0 data output (used in 3-wire SIO mode)
Port B	I/o	• 7-bit I/O port
	1/0	• I/O specifiable in 1-bit units
PB0 to PB6		 Pull-up resistors can be turned on and off in 1 bit units
	• Multiplexed pin functions	
		PB4 : SMIIC1 clock input/output
		PB5 : SMIIC1 bus input/output/data input
		PB6 : SMIIC1 data output (used in 3-wire SIO mode)
Port C	I/O	• 5-bit I/O port
PC0 to PC4		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units(PC2)
		• Pin functions
		PC0 : 32.768 kHz crystal oscillator input
		PC1 : 32.768 kHz crystal oscillator output
		PC2 : FILT of VCO
		PC3 : Ceramic oscillator input
	- 10	PC4 : Ceramic oscillator output/VCO output
Port D	I/O	• 6-bit I/O port
PD0 to PD5		• I/O specifiable in 1-bit units
TEGT	L/O	Pull-up resistors can be turned on and off in 1 bit units
TEST	I/O	• TEST pin
		• Used to communicate with on-chip debugger.
DECD	L/O	Connects an external 100 kΩ pull-down resistor.
RESB	I/O	Reset pin

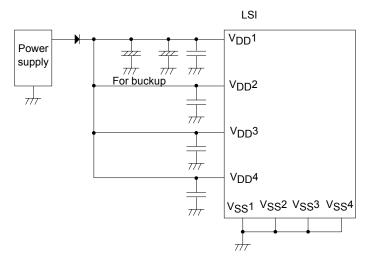
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Output Type	Pull-up Resistor
P00 to P07		CMOS	
P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 PA0 to PA7 PB0 to PB6	1 bit	Able to program special functions'output type from CMOS output or Nch-opendrain	Programmable
P60 to P67 P70 to p77 PD0 to PD5 PC2		CMOS	
PC0	-	N-channel open drain (32.768 kHz crystal oscillator input)	None
PC1	_	Nch-open drain (32.768k kHz crystal oscillator output)	None
PC3	_	CMOS (ceramic oscillator input)	None
PC4	_	CMOS (ceramic oscillator output)	None

* Make the following connection to minimize the noise input to the VDD1 pin and prolong the backup time. Be sure to electrically short the VSS1, VSS2, VSS3 and VSS4 pins.

Example 1 : When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Electrical Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Pin	Conditions			Specific	ation	-
Farameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High level input current	IIH (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B,C, D RESB	Output disabled Pull-up resistor off VIN=VDD (including output Tr. off leakage current)	2.7 to 3.6			1	
Low level input current	IIL (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB	Output disabled Pull-up resistor off VIN=VSS (including output Tr. off leakage current)	2.7 to 3.6	-1			μΑ
High level output voltage	VOH (1)	Ports 0, 1, 2, 3 Ports 5, 6	IOH=-0.4mA	3.0 to 3.6	V _{DD} -0.4			
	VOH (2)	Ports A, D, PC2 P40 to P45 PB2 to PB6	IOH=-0.2mA	2.7 to 3.6	V _{DD} -0.4			
		P46, P47	IOH=-1.6mA	3.0 to 3.6	V _{DD} -0.4			
	VOH (4)	PB0, PB1	IOH=-1.0mA	2.7 to 3.6	V _{DD} -0.4			
	VOH (5)	PC0, PC1,	IOH=-1.0mA	3.0 to 3.6	V _{DD} -0.4			
	VOH (6)	PC3, PC4,	IOH=-0.4mA	2.7 to 3.6	V _{DD} -0.4			
Low level output voltage	VOL (1)	Ports 0, 1, 3, 4 Ports 5, 6, 7, D PC2	IOL=1.6mA	3.0 to 3.6			0.4	v
	VOL (2)	P20 to P21, P24 to P27 PA0 to PA3 PA6 to PA7 PB0 to PB3, PB6	IOL=1.0mA	2.7 to 3.6			0.4	
	VOL (3)	P22, P23,	IOL=3.0mA	3.0 to 3.6			0.4	
	VOL (4)	PA4, PA5, PB4, PB5	IOL=1.3mA	2.7 to 3.6			0.4	
	VOL (5)	PC0, PC1,	IOL=1.0mA	3.0 to 3.6			0.4	
	VOL (6)	PC3, PC4,	IOL=0.4mA	2.7 to 3.6			0.4	
Pull-up resistor	Rpu (1)	Ports 0, 1, 2, 3 Ports 4, 5, 6, 7	VOH=0.9V _{DD}	3.0 to 3.6	15	35	80	kΩ
	Rpu (2)	Ports A, B, D, PC2		2.7 to 3.6	15	35	100	Nº 2
Hysteresis voltage	VHYS	RESB When ports 1, 2, 3, 4, A, B PnFSAn=1		2.7 to 3.6		0.1V _{DD}		v
Pin capacitance	СР	All pins	Pins other than that under test VIN=VSS f=1 MHz Ta=25°C	2.7 to 3.6		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

• Serial I/O Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$ Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

г	Doromotor	Symbol	Applicable	Conditions			Specif	ication	-
r	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Inpu	Period	tSCK (1)	SCK0 (P12)	• See Fig. 6.		4			
ıt clock	Low level pulse width	tSCKL (1)				2			
	High level	tSCKH(1)				2			
	pulse width	tSCKHA (1)	•	 Automatic communication mode See Fig. 6. 	2.7 to 3.6	6			
	Period	tSCKHBSY (1a)		 Automatic communication mode See Fig. 6. 		23			tCYC
		tSCKHBSY (1b)		 Mode other than automatic communication mode See Fig. 6. 		4			-
Output	Period	tSCK (2)	SCK0 (P12)	• CMOS output selected • See Fig. 6.		4			
clock	Low level pulse width	tSCKL (2)				1/2			tSCK
	High level pulse width	tSCKH (2)					1/2		IJCK
		tSCKHA (2)		 Automatic communication mode CMOS output selected See Fig. 6. 	2.7 to 3.6	6			
		tSCKHBSY (2a)		 Automatic communication mode CMOS output selected See Fig. 6. 		4		23	tCYC
		tSCKHBSY (2b)		 Mode other than automatic communication mode See Fig. 6. 		4			
Da	ta setup time	tsDI (1)	SI0 (P11), SB0 (P11)	rising edge of SIOCLK		0.03			
Da	ta hold time	thDI (1)		• See Fig. 6.	2.7 to 3.6	0.03			
Input clock	Output delay time	tdD0 (1)	SO0 (P10), SB0 (P11)	• (Note 4-1-2)				1tCYC +0.05	μs
Output clock		tdDO (2)		• (Note 4-1-2)	2.7 to 3.6			1tCYC +0.05	
	Input clock Da Da Input clock Da Da Input clock	Low level pulse width High level pulse width High level pulse width Low level pulse width Low level pulse width High level pulse width Data hold time Input clock Input clock	$\begin{array}{ c c c c } \hline \begin{tabular}{ c c c c } \hline Period & tSCK (1) \\ \hline Low level & tSCK (1) \\ \hline low level & tSCKL (1) \\ \hline pulse width & tSCKH (1) \\ \hline pulse width & tSCKHA (1) \\ \hline \\ $	ParameterSymbolPin/RemarksInput lowPeriodtSCK (1)SCK0 (P12)Low level pulse widthtSCKL (1)tSCK1 (1)High level pulse widthtSCKH (1)tSCKHA (1)TSCKHBSY (1a)tSCKHBSY (1b)tSCK0 (P12)Output cokPeriodtSCK (2)Low level pulse widthtSCKL (2)Low level pulse widthtSCKL (2)Low level pulse widthtSCKH (2)Data setup timetSDI (1)Data setup timetSDI (1)Data hold timethDI (1)Input clockOutput delay timetimetdD0 (1)SB0 (P11)	Parameter Symbol Pin/Remarks Conditions Image: Conditions tSCK (1) SCK0 (P12) * See Fig. 6. Low level pulse width tSCKH (1) * Automatic communication mode * Automatic communication mode Image: Conditions tSCKHA (1) * See Fig. 6. * Automatic communication mode Image: Conditions tSCKHBSY (1a) * SCK0 (P12) * Automatic communication mode Vertice tSCKHBSY (1b) * SCK0 (P12) * Automatic communication mode Vertice tSCKL (2) SCK0 (P12) * CMOS output selected Vertice tSCKL (2) SCK0 (P12) * Automatic communication mode Vertice tSCKL (2) * SCK0 (P12) * Automatic communication mode Vertice tSCKHA (2) * SCKHA (2) * Automatic communication mode Vertice tSCKHBSY (2b) * Sold output selected * See Fig. 6. Data setup time tsD1 (1) SB0 (P11) * Specified with respect to rising edge of SIOCLK Tota tdD0 (1) SO0 (P10), time * (Note 4-1-2)	ParameterSymbolPin/RemarksConditions $V_{DD}[V]$ \overline{Pur} tSCK (1)SCK 0 (P12)'See Fig. 6.'Automatic communication mode2.7 to 3.6 \overline{Pur} tSCKH1(1) pulse widthtSCKH1(1) tSCKHA (1)'Automatic communication mode'See Fig. 6.2.7 to 3.6 \overline{Pur} tSCKHBSY (1a)tSCK1 (2) (1b)'SCK0 (P12)'CMOS output selected ·See Fig. 6.'Automatic communication mode2.7 to 3.6 \overline{Pur} tSCKL (2) pulse widthtSCKL (2) pulse widthSCK0 (P12)'CMOS output selected ·See Fig. 6.'Automatic communication mode \overline{Pur} tSCKHA (2) pulse widthtSCKL (2) pulse widthSCK0 (P12)'Automatic communication mode2.7 to 3.6 \overline{Pur} tSCKHA (2) pulse widthtSCKH2SCK0 (P12)'Automatic communication mode2.7 to 3.6 \overline{Pur} tSCKHBSY (2a)'See Fig. 6.'Automatic communication mode2.7 to 3.6 \overline{Pur} tSCKHBSY (2a)'See Fig. 6.'Automatic communication mode \overline{Data} setup timetSD (1) sB0 (P11)SB0 (P10) SB0 (P11)'Specified with respect to rising edge of SIOCLK ·See Fig. 6.2.7 to 3.6 \overline{Pur} tdD0 (1) sB0 (P10) sB0 (P11)'(Note 4-1-2)2.7 to 3.6	Parameter Symbol Pin/Remarks Conditions V _{DD} [V] min Image: period tSCK (1) SCK0 (P12) * See Fig. 6. 4 2 Image: period tSCK1 (1) tSCK1 (1) * See Fig. 6. 2.7 to 3.6 6 Image: period tSCK1 (1) tSCK1 (1) * Automatic communication mode 2.7 to 3.6 6 * See Fig. 6. * Automatic communication mode * See Fig. 6. 23 23 * See Fig. 6. * Mode other than automatic communication mode * See Fig. 6. 23 * Conditions mode * See Fig. 6. * Automatic communication mode 23 * See Fig. 6. * CMOS output selected * See Fig. 6. 4 Image: pulse width tSCKH (2) * Automatic communication mode 2.7 to 3.6 6 * See Fig. 6. * See Fig. 6. * Automatic communication mode * See Fig. 6. 4 * See Fig. 6. * See Fig. 6. * Automatic communication mode * CMOS output selected * See Fig. 6. 4 * See Fig. 6. * Mode other than automatic communication mode <t< td=""><td>ParameterSymbolPrin/RemarksConditionsV_{DD} [V]mintypPeriodiSCK (1)SCK0 (P12)'See Fig. 6.422Low level pulse widthiSCKH (1)iSCKH (1)'Automatic communication mode ·See Fig. 6Automatic communication mode ·See Fig. 6.2.7 to 3.6623PeriodtSCKH BSY (1a)iSCKD (P12)'CMOS output selected ·See Fig. 6CMOS output selected ·See Fig. 6.2.7 to 3.66PeriodtSCK1 (2) pulse widthSCK0 (P12)'CMOS output selected ·See Fig. 6CMOS output selected ·See Fig. 6.4Image: Sign (2a)iSCKH (2) pulse widthiSCKH (2) pulse widthSCK0 (P12)'Automatic communication mode ·See Fig. 61/2Image: Sign (2a)iSCKH (2) pulse widthiSCKH (2) pulse widthSCK0 (P12)'Automatic communication mode ·CMOS output selected ·See Fig. 61/2Image: Sign (2a)iSCKH (2) pulse widthiSCKH (2) pulse widthSign (P11) ising edge of SIGCLK-1/2Image: Data setup timeisD1 (1) ising (2b)Sign (P11) ising edge of SIGCLKSoce Fig. 6.0.03Image: Data hold timeidD0 (1) timeSO0 (P10), SB0 (P11)'(Note 4-1-2)0.030.03</td><td>$\begin{array}{ c$</td></t<>	ParameterSymbolPrin/RemarksConditions V_{DD} [V]mintypPeriodiSCK (1)SCK0 (P12)'See Fig. 6.422Low level pulse widthiSCKH (1)iSCKH (1)'Automatic communication mode ·See Fig. 6Automatic communication mode ·See Fig. 6.2.7 to 3.6623PeriodtSCKH BSY (1a)iSCKD (P12)'CMOS output selected ·See Fig. 6CMOS output selected ·See Fig. 6.2.7 to 3.66PeriodtSCK1 (2) pulse widthSCK0 (P12)'CMOS output selected ·See Fig. 6CMOS output selected ·See Fig. 6.4Image: Sign (2a)iSCKH (2) pulse widthiSCKH (2) pulse widthSCK0 (P12)'Automatic communication mode ·See Fig. 61/2Image: Sign (2a)iSCKH (2) pulse widthiSCKH (2) pulse widthSCK0 (P12)'Automatic communication mode ·CMOS output selected ·See Fig. 61/2Image: Sign (2a)iSCKH (2) pulse widthiSCKH (2) pulse widthSign (P11) ising edge of SIGCLK-1/2Image: Data setup timeisD1 (1) ising (2b)Sign (P11) ising edge of SIGCLKSoce Fig. 6.0.03Image: Data hold timeidD0 (1) timeSO0 (P10), SB0 (P11)'(Note 4-1-2)0.030.03	$ \begin{array}{ c $

Note 4-1-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

	п	arameter	Saurah a l	Applicable	Conditions			Specif	ication	
	Р	arameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Seria	Inpu	Period	tSCK (6)	SCK1 (P45)	SCK1 (P45) • See Fig. 6.		2			
Serial clock		tSCKL (6)				1				
		High level	tSCKH (6)			2.7 to 3.6	1			tCYC
]	pulse width	tSCKHBSY (6)				2			
Serial input	Dat	Data setup time tsDI (4		SI1 (P44), SB1 (P44)	• Specified with respect to rising edge of SIOCLK		0.03			
input	Dat	ta hold time	thDI (4)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Input clock	Output delay time	tdD0 (6)	SO1 (P43), SB1 (P44)	• (Note 4-4-2)	2.7 to 3.6			1tCYC +0.05	μs

SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)

Note 4-4-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

				Applicable				Specif	ication	
	P	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (10)	SM0CK (P22)	See Fig. 6.		4			
clock	clock	Low level pulse width	tSCKL (10)			2.7 to 3.6	2			~~~~
	pulse wid	High level pulse width	tSCKH (10)				2			tCYC
	Outpu	Period	tSCK (11)	SM0CK (P22)	CMOS output selected See Fig. 6.		4			
	0	Low level pulse width	tSCKL (11)			2.7 to 3.6	1/2			- COV
		High level pulse width	tSCKH (11)					1/2		tSCK
Serial input	Dat	ta setup time	tsDI (7)	SM0DA (P23),	• Specified with respect to rising edge of SIOCLK		0.03			
input	Dat	ta hold time	thDI (7)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output			tdD0 (10)	SM0DO (P24), SM0DA (P23)	 Specified with respect to falling edge of SIOCLK Specified as interval up to time when output state starts changing. See Fig. 6. 	2.7 to 3.6			1tCYC +0.05	μs

SMIIC0 Simple SIO Mode Input/Output Characteristics (Note 4-7-1)

 Note 4-7-1 : These specifications are theoretical values. Add margin depending on its use.

SMIIC0 I²C Mode Input/Output Characteristics (Note 4-8-1) (Note 4-8-2) (Note 4-8-4)

	р	arameter		Symbol	Applicable Conditions			Specif	ication	1		
	1	arameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Clock	Input clock	Period		tSCL	SM0CK (P22)	• See Fig. 8.		5				
	lock	Low level pulse widt	h	tSCLL			2.7 to 3.6	2.5			TEL	
		High level pulse widt		tSCLH				2			Tfilt	
	Output clock	Period		tSCLx	SM0CK (P22)	• Specified as interval up to time when output state starts		10				
	t clock	Low level pulse width		tSCLLx		changing.	2.7 to 3.6	1/2				
		High level pulse widt		tSCLHx					1/2		tSCL	
pin	is inp	K and SM0E out spike ssion time	nd SM0DA tsp SM0CK (P22) • See Fig. 8. spike SM0DA (P23) 2.7 to 3.6		Tfilt							
Bus release time between start and		Input	tBUF	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		2.5			Tfilt		
		etween start and		tBUFx	SM0CK (P22) SM0DA (P23)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	5.5				
stop	tput			fput				High-speed clock mode Specified as interval up to time when output state starts changing.		1.6		
			lı	tHD;STA	SM0CK (P22) SM0DA (P23)	When SMIIC register control bit, I2CSHDS=0 · See Fig. 8.	-	2.0				
	urt/re		Input			When SMIIC register control bit I2CSHDS=1 · See Fig. 8.		2.5			Tfilt	
tim		on hold	Ou	tHD;STAx	SM0CK (P22) SM0DA (P23)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	4.1				
			Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.0			μs	
			Input	tSU;STA	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		1.0			Tfilt	
		condition me	Out	tSU;STAx	SM0CK (P22) SM0DA (P23)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	5.5				
	etup tir	up time		Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.6			– μs

			0 1 1	Applicable	e Conditions			Specific	cation	
	ł	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (13)	SL0CK (PA4)	Ũ		4			
clock	clock	Low level pulse width	tSCKL (13)			2.7 to 3.6	2			tCYC
		High level pulse width	tSCKH (13)				2			
Serial input	1		tsDI (9)	SL0DA (PA5),	• Specified with respect to rising edge of SIOCLK		0.03			
input	Da	ta hold time	thDI (9)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output			tdD0 (13)	SL0DO (PA6), SL0DA (PA5)	 Specified with respect to falling edge of SIOCLK Specified as interval up to time when output state starts changing. See Fig. 6. 	2.7 to 3.6			1tCYC +0.05	μs

SLIIC0 Simple SIO Mode Input/Output Characteristics (Note 4-11-1)

Note 4-11-1 : These specifications are theoretical values. Add margin depending on its use.

D (Applicable			Specification			
Parameter		Symbol	Pin/Remarks	Conditions	$V_{DD}[V]$	Min	typ	max	Unit
	Input	tF	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6			300	
SL0CK and SL0DA pins fall time	Output	tF	SLOCK (PA4) SLODA (PA5)	When SLIIC0 register control bits PSLW=1, PHV=1	3	20+0.1Cb (Note 4-12-3)		250	ns
	put			 SL0CK, SL0DA port output FAST mode Cb ≤ 100pF 	3.0 to 3.6			100	

Note 4-12-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-12-2 : The value of Tfilt is determined by the values of the register SLICOPCNT, bits 5 and 4 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range : $250 \text{ ns} \ge \text{Tfilt} > 140 \text{ ns}$

Note 4-12-3: Cb represents the total loads (in pF) connected to the bus pins. $Cb \le 100 \text{ pF}$

_	-		~~~	~~ ~~	~~			
Parameter	Symbol	Applicable			Specification			
Parameter	Symbol	Pin/Remarks		V _{DD} [V]	min	typ	max	unit
Transfer rate	UBR0	U0RX (P13), U0TX (P14), U0BRG (P07)		2.7 to 3.6	4		8	tBGCYC

UART0 Operating Conditions at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

Note 4-9 : tBGCYC denotes one cycle of the baudrate clock source.

UART2 Operating Conditions at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable Conditions				Speci	fication	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Transfer rate	UBR2	U2RX (P16), U2TX (P17),		2.7 to 3.6	8		4096	tBGCYC

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

UART3 Operating Conditions at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol Applicable					Speci	fication	
Farameter	Symbol	Pin/Remarks	Conditions	$V_{DD}[V]$	min	typ	max	unit
Transfer rate	UBR3	U3RX (P34), U3TX (P35),		2.7 to 3.6	8		4096	tBGCYC

Note 4-10 : tBGCYC denotes one cycle of the baudrate clock source.

■ Pulse Input Conditions at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V

Daramatar	Symbol	Amplicable Din/Demorita	oplicable Pin/Remarks Conditions			Specif	ication	
Parameter	Symbol	Applicable Pli/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH (1) tPIL (1)	INT0 (P30), INT1 (P31), INT2 (P32), INT3 (P33), INT4 (P20), INT5 (P21), INT6 (P40), INT7 (P41)	 Interrupt source flag can be set. Event inputs for timers 2 and 3 are enabled. 	2.7 to 3.6	2			tCYC
	tPIL (2)	RESB	Resetting is enabled.	2.7 to 3.6	10			μs

■ AD Converter Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$ 12-bit AD Conversion Mode

Parameter	Seconda e l	Applicable Pin	Conditions		Specification			
	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	NAD	AN0 (P60) to AN7 (P67),		2.7 to 3.6		12		bit
Absolute accuracy	ETAD	AN8 (P70)	(Note 6-1)	2.7 to 3.6			±16	LSB
Conversion time	TCAD12	to AN15 (P77)	Conversion time calculated	3.0 to 3.6	64		115	
				2.7 to 3.6	128		230	μs
Analog input voltage range	VAIN			2.7 to 3.6	V _{SS}		V _{DD}	V
Analog port input current	IAINH		VAIN=V _{DD}	2.7 to 3.6			1	
input current	IAINL		VAIN=V _{SS}	2.7 to 3.6	-1			μA

- Conversion time calculation formula : TCAD12 = $\left(\frac{52}{\text{AD division ratio}} + 2\right) \times \text{tCYC}$

8-bit AD Conversion Mode

Parameter	Course of	Applicable Pin	Conditions		Specification			
	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	NAD	AN0 (P60) to AN7 (P67),		2.7 to 3.6		8		bit
Absolute accuracy	ETAD	AN8 (P70)	(Note 6-1)	2.7 to 3.6			±1.5	LSB
Conversion time	TCAD8	to AN15 (P77)	Conversion time calculated	3.0 to 3.6	39		71	
				2.7 to 3.6	79		140	μs
Analog input voltage range	VAIN			2.7 to 3.6	V _{SS}		V _{DD}	v
Analog port input current	IAINH		VAIN=VDD	2.7 to 3.6			1	
input current	IAINL		VAIN=V _{SS}	2.7 to 3.6	-1			μA

- Conversion time calculation formula : TCAD8 = $\left(\frac{52}{\text{AD division ratio}} + 2\right) \times \text{tCYC}$

Note 6-1 : The quantization error ($\pm 1/2$ LSB) is excluded from the absolute accuracy.

Note 6-2 : The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.

- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

■ Consumption Current Characteristics at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V typ : 3.3V

Demonster	Countral	Applicable	Contitions			Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP (1)	V_{DD1} $=V_{DD2}$ $=V_{DD3}$ $=V_{DD4}$	FmCF=10 MHz ceramic oscillator mode FmX'tal=32.768 kHz crystal oscillator mode System clock set to 10 MHz Internal RC oscillation stopped 1/1 frequency division mode	2.7 to 3.6		5.0	12.0	
	IDDOP (2)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768 kHz crystal oscillator mode System clock set to internal RC oscillation 1/1 frequency division mode	2.7 to 3.6		0.8	2.1	mA
	IDDOP (3)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768 kHz crystal oscillator mode System clock set to 32.768 kHz Internal RC oscillation stopped 1/1 frequency division mode	2.7 to 3.6		30	136	μΑ

Continued on next page.

D						Specification			
Parameter	Symbol	Pin/Remarks		Option selected voltage	min	typ	max	unit	
Por release	PORRL		• Select from option.	2.57V	2.47	2.57	2.72		
voltage			(Note 8-1)	2.87V	2.77	2.87	3.02		
Detction voltage unknown state	POUKS		• See Fig 10. (Note 8-2)			0.7	0.95	V	
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.6V.				100	ms	

■ Power-on Reset (POR) Characteristics at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

Note8-1 : The POR release level can be selected out of 2 levels only when the LVD reset function is disabled. Note8-2 : POR is in an unknown state before transistors start operation.

■ Low Voltage Detection Reset (LVD) Characteristics

at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

_						Specif	ication	
Parameter		Pin/Remarks		Option selected voltage	min	typ	max	unit
LVD reset voltage (Note 9-1)	LVDET		 Select from option. (Note 9-2) See Fig 11. 	2.81V	2.71	2.81	2.96	V
LVD hysteresis width	LVHYS			2.81V		60		mV
Detection voltage unknown state	LVUKS		• See Fig 11. (Note 9-3)			0.7	0.95	v
Low voltage detection minimum width (Replay sensitivity)	TLVDW		• LVDET-0.5V • See Fig 12.		0.2			ms

Note9-1 : LVD reset voltage specification values do not include hysteresis voltage.

Note9-2 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note9-3 : LVD is in an unknown state before transistors start operation.

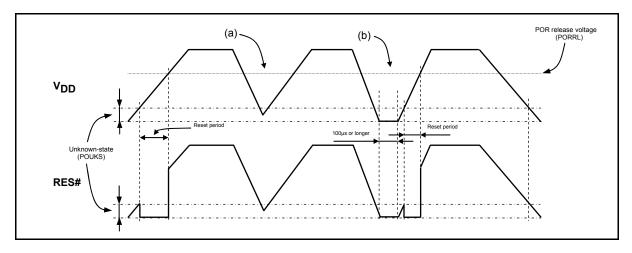


Figure 10. Waveform observed when only POR is used (LVD not used) (RESET pin : Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the VSS level.
- <u>No stable reset will be generated if power is turned on again when the power level does not go</u> <u>down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function</u> <u>together with the POR function or implement an external reset circuit.</u>
- <u>A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.</u>

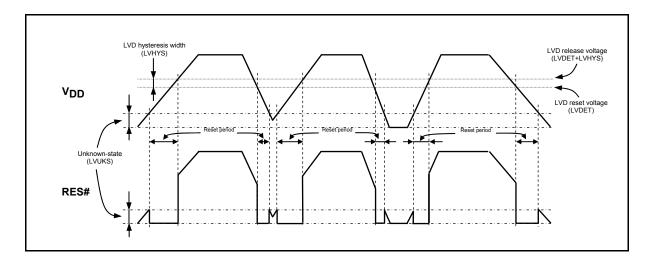
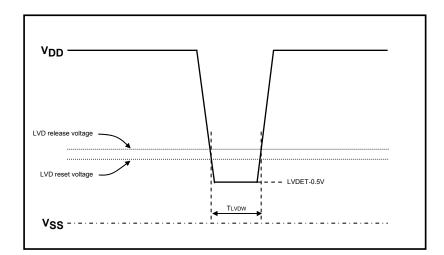
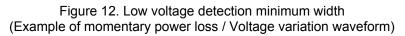


Figure 11. Waveform observed when both POR and LVD functions are used (RESET pin : Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- <u>A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.</u>





ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC88FC3K0AUTJ-2H	TQFP 100, 14x14 (Pb-Free / Halogen Free)	900 / Tray JEDEC

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