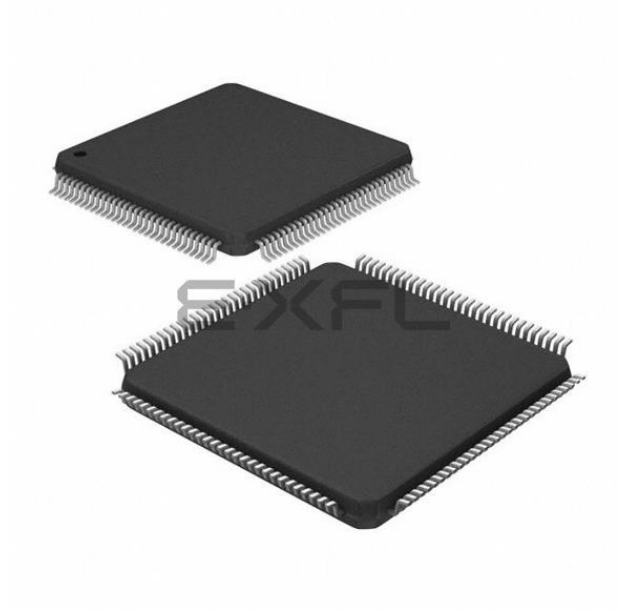

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Program Memory Type	FLASH
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2.2 CPU Operating Modes

The H8SX CPU has four operating modes: normal, middle, advanced and maximum modes. These modes can be selected by the mode pins of this LSI.

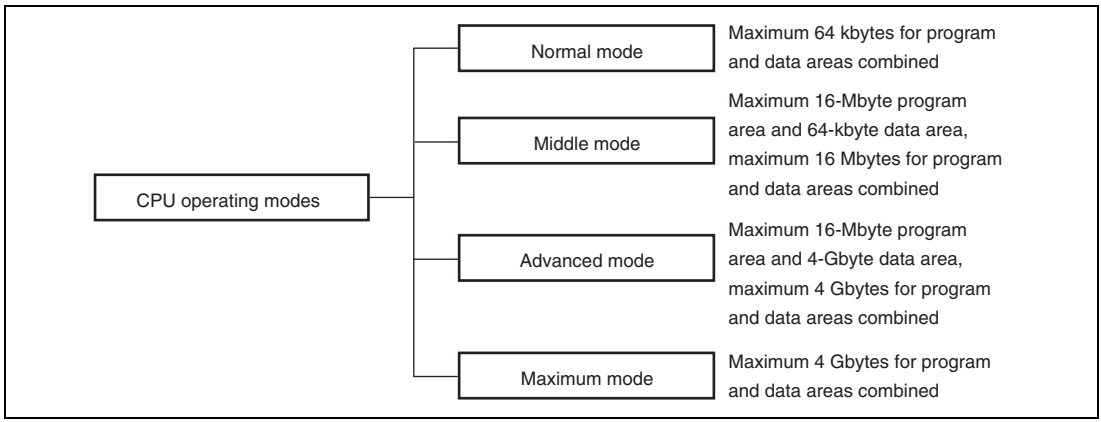

Figure 2.1 CPU Operating Modes

2.2.1 Normal Mode

The exception vector table and stack have the same structure as in the H8/300 CPU.

- Address Space

  The maximum address space of 64 kbytes can be accessed.
- Extended Registers (En)

  The extended registers (E0 to E7) can be used as 16-bit registers, or as the upper 16-bit segments of 32-bit registers. When the extended register En is used as a 16-bit register it can contain any value, even when the corresponding general register Rn is used as an address register. (If the general register Rn is referenced in the register indirect addressing mode with pre-/post-increment or pre-/post-decrement and a carry or borrow occurs, however, the value in the corresponding extended register En will be affected.)
- Instruction Set

  All instructions and addressing modes can be used. Only the lower 16 bits of effective addresses (EA) are valid.

9.2.2 Access State Control Register (ASTCR)

ASTCR designates each area in the external address space as either 2-state access space or 3-state access space and enables/disables wait cycle insertion.

Bit	15	14	13	12	11	10	9	8
Bit Name	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial Value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	7	6	5	4	3	2	1	0
Bit Name	—	—	—	—	—	—	—	—
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	AST7	1	R/W	Area 7 to 0 Access State Control
14	AST6	1	R/W	These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space. Wait cycle insertion is enabled or disabled at the same time.
13	AST5	1	R/W	
12	AST4	1	R/W	
11	AST3	1	R/W	0: Area n is designated as 2-state access space
10	AST2	1	R/W	Wait cycle insertion in area n access is disabled
9	AST1	1	R/W	1: Area n is designated as 3-state access space
8	AST0	1	R/W	Wait cycle insertion in area n access is enabled
				(n = 7 to 0)
7 to 0	—	All 0	R	Reserved
				These are read-only bits and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
6	W12	1	R/W	Area 1 Wait Control 2 to 0
5	W11	1	R/W	These bits select the number of program wait cycles when accessing area 1 while bit AST1 in ASTCR is 1.
4	W10	1	R/W	000: Program wait cycle not inserted
				001: 1 program wait cycle inserted
				010: 2 program wait cycles inserted
				011: 3 program wait cycles inserted
				100: 4 program wait cycles inserted
				101: 5 program wait cycles inserted
				110: 6 program wait cycles inserted
				111: 7 program wait cycles inserted
3	—	0	R	Reserved
				This is a read-only bit and cannot be modified.
2	W02	1	R/W	Area 0 Wait Control 2 to 0
1	W01	1	R/W	These bits select the number of program wait cycles when accessing area 0 while bit AST0 in ASTCR is 1.
0	W00	1	R/W	000: Program wait cycle not inserted
				001: 1 program wait cycle inserted
				010: 2 program wait cycles inserted
				011: 3 program wait cycles inserted
				100: 4 program wait cycles inserted
				101: 5 program wait cycles inserted
				110: 6 program wait cycles inserted
				111: 7 program wait cycles inserted

9.2.9 Endian Control Register (ENDIANCR)

ENDIANCR selects the endian format for each area of the external address space. Though the data format of this LSI is big endian, data can be transferred in the little endian format during external address space access.

Note that the data format for the areas used as a program area or a stack area should be big endian.

Bit	7	6	5	4	3	2	1	0
Bit Name	LE7	LE6	LE5	LE4	LE3	LE2	—	—
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	LE7	0	R/W	Little Endian Select
6	LE6	0	R/W	Selects the endian for the corresponding area.
5	LE5	0	R/W	0: Data format of area n is specified as big endian
4	LE4	0	R/W	1: Data format of area n is specified as little endian
3	LE3	0	R/W	(n = 7 to 2)
2	LE2	0	R/W	
1, 0	—	All 0	R	Reserved These are read-only bits and cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
9	BSWD01	0	R/W	Area 0 Burst Word Number Select
8	BSWD00	0	R/W	Selects the number of words in burst access to the area 0 burst ROM interface 00: Up to 4 words (8 bytes) 01: Up to 8 words (16 bytes) 10: Up to 16 words (32 bytes) 11: Up to 32 words (64 bytes)
7	BSRM1	0	R/W	Area 1 Burst ROM Interface Select Specifies the area 1 bus interface as a basic interface or a burst ROM interface. To set this bit to 1, clear bit BCSEL1 in SRAMCR to 0. 0: Basic bus interface or byte-control SRAM interface 1: Burst ROM interface
6	BSTS12	0	R/W	Area 1 Burst Cycle Select
5	BSTS11	0	R/W	Specifies the number of cycles of area 1 burst cycle
4	BSTS10	0	R/W	000: 1 cycle 001: 2 cycles 010: 3 cycles 011: 4 cycles 100: 5 cycles 101: 6 cycles 110: 7 cycles 111: 8 cycles
3	—	All 0	R	Reserved
2				These are read-only bits and cannot be modified.
1	BSWD11	0	R/W	Area 1 Burst Word Number Select
0	BSWD10	0	R/W	Selects the number of words in burst access to the area 1 burst ROM interface 00: Up to 4 words (8 bytes) 01: Up to 8 words (16 bytes) 10: Up to 16 words (32 bytes) 11: Up to 32 words (64 bytes)

Data Size	Access Address	Access Count	Bus Cycle	Data Size	Strobe signal LHWR/LUB, LLWR/LLB, RD; Data bus D15 D8 D7 D0
Byte	n	1	1st	Byte	7 0
Word	n	2	1st	Byte	7 0
			2nd	Byte	15 8
Longword	n	4	1st	Byte	7 0
			2nd	Byte	15 8
			3rd	Byte	23 16
			4th	Byte	31 24

Figure 9.11 Access Sizes and Data Alignment Control for 8-Bit Access Space (Little Endian)

(2) 16-Bit Access Space

With the 16-bit access space, the upper byte data bus (D15 to D8) and lower byte data bus (D7 to D0) are used for accesses. The amount of data that can be accessed at one time is one byte or one word.

Figures 8.12 and 8.13 illustrate data alignment control for the 16-bit access space. Figure 9.12 shows the data alignment when the data endian format is specified as big endian. Figure 9.13 shows the data alignment when the data endian format is specified as little endian.

In big endian, byte access for an even address is performed by using the upper byte data bus and byte access for an odd address is performed by using the lower byte data bus.

In little endian, byte access for an even address is performed by using the lower byte data bus, and byte access for an odd address is performed by using the third byte data bus.

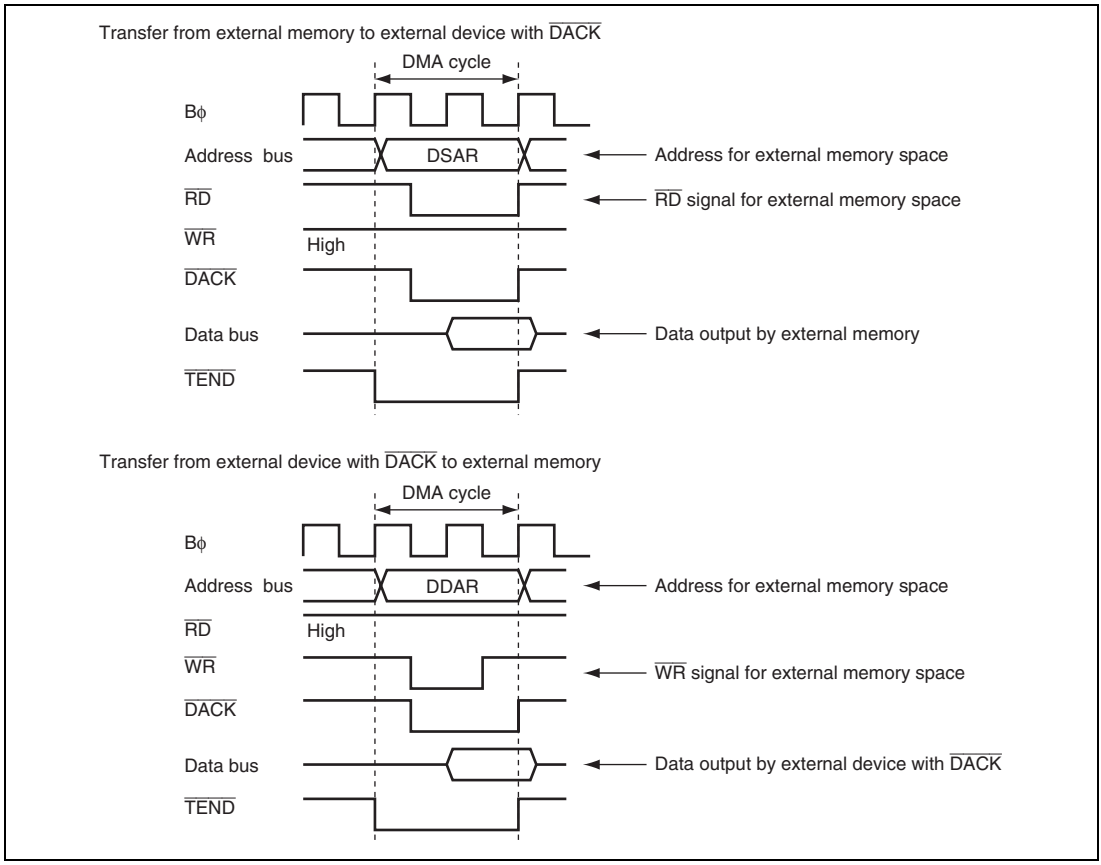

Figure 10.5 Example of Signal Timing in Single Address Mode

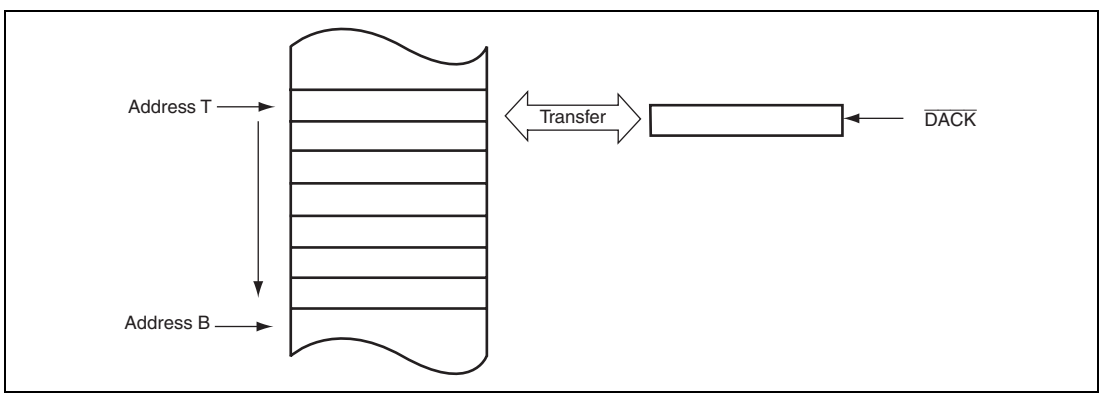

Figure 10.6 Operations in Single Address Mode

- EDMDR_1 to EDMDR_3

Bit	31	30	29	28	27	26	25	24
Bit Name	DTE	EDACKE	ETENDE	EDRAKE	DREQS	NRD	—	—
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Bit	23	22	21	20	19	18	17	16
Bit Name	ACT	—	—	—	—	—	ESIF	DTIF
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/(W)*	R/(W)*
Bit	15	14	13	12	11	10	9	8
Bit Name	DTSZ1	DTSZ0	MDS1	MDS0	TSEIE	—	ESIE	DTIE
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Bit Name	DTF1	DTF0	—	—	—	EDMAP2	EDMAP1	EDMAP0
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Note: * Only 0 can be written to this bit after having been read as 1, to clear the flag.

11.7 Ending EXDMA Transfer

The operation for ending EXDMA transfer depends on the transfer end conditions. When EXDMA transfer ends, the DTE bit and the ACT bit in EDMDR change from 1 to 0, indicating that EXDMA transfer has ended.

(1) Transfer End by EDTCR Change from 1, 2, or 4 to 0

When the value of EDTCR changes from 1, 2, or 4 to 0, EXDMA transfer ends on the corresponding channel. The DTE bit in EDMDR is cleared to 0, and the DTIF bit in EDMDR is set to 1. If the DTIE bit in EDMDR is set to 1 at this time, a transfer end interrupt request is generated by the transfer counter. EXDMA transfer does not end if the EDTCR value has been 0 since before the start of transfer.

(2) Transfer End by Transfer Size Error Interrupt

When the following conditions are satisfied while the TSEIE bit in EDMDR is set to 1, a transfer size error occurs and an EXDMA transfer is terminated. At this time, the DTE bit in EDMDR is cleared to 0 and the ESIF bit in EDMDR is set to 1.

- In normal transfer mode and repeat transfer mode, when the next transfer is requested while a transfer is disabled due to the EDTCR value less than the data access size.
- In block transfer mode, when the next transfer is requested while a transfer is disabled due to the EDTCR value less than the block size.
- In cluster transfer mode, when the next transfer is requested while a transfer is disabled due to the EDTCR value less than the cluster size.

When the TSEIE bit in EDMDR is cleared to 0, data is transferred until the EDTCR value reaches 0. A transfer size error is not generated. Operation in each transfer mode is described below.

- In normal transfer mode and repeat mode, when the EDTCR value is less than the data access size, data is transferred in bytes.
- In block transfer mode, when the EDTCR value is less than the block size, the specified size of data in EDTCR is transferred instead of transferring the block size of data. When the EDTCR value is less than the data access size, data is transferred in bytes.
- In cluster transfer mode, when the EDTCR value is less than the cluster size, the specified size of data in EDTCR is transferred instead of transferring the cluster size of data. When the EDTCR value is less than the data access size, data is transferred in bytes.

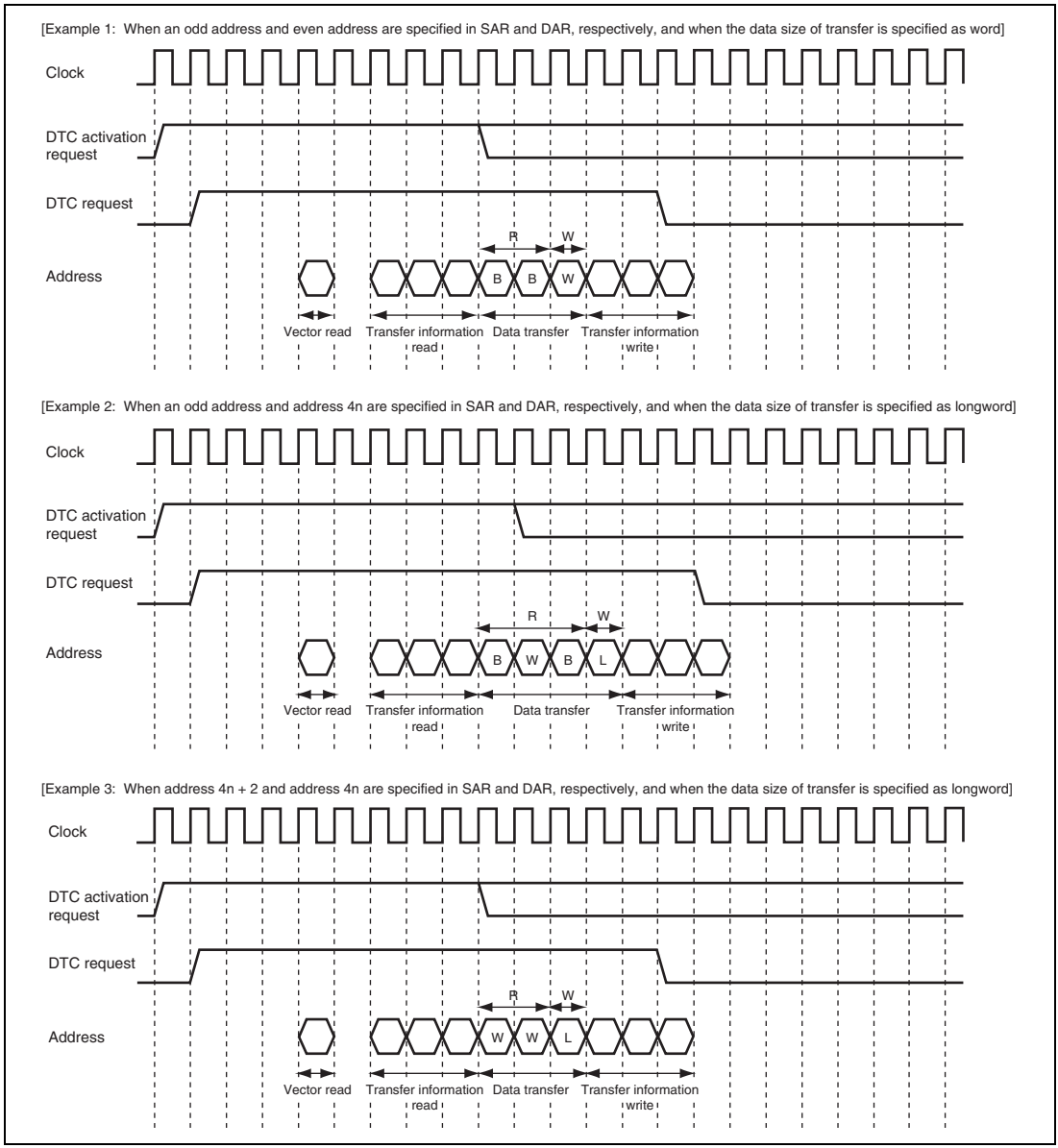

Figure 12.5 Bus Cycle Division Example

Table 14.32 TIORL_6 (Unit 1)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_6 Function**	**TIOCC6 Pin Function**
0	0	0	0	Output compare register*2	Output disabled
0	0	0	1		Initial output is 0 output. 0 output at compare match
0	0	1	0		Initial output is 0 output. 1 output at compare match
0	0	1	1		Initial output is 0 output. Toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is 1 output. 0 output at compare match
0	1	1	0		Initial output is 1 output. 1 output at compare match
0	1	1	1		Initial output is 1 output. Toggle output at compare match
1	0	0	0	Input capture register*2	Capture input source is TIOCC6 pin. Input capture at rising edge
1	0	0	1		Capture input source is TIOCC6 pin. Input capture at falling edge
1	0	1	x		Capture input source is TIOCC6 pin. Input capture at both edges
1	1	x	x		Capture input source is channel 1/count clock. Input capture at TCNT_7 count-up/count-down*1

[Legend]

x: Don't care

Note: 1. When the bits TPSC2 to TPSC0 in TCR_7 are set to B'000 and Pϕ/1 is used as the count clock of TCNT_7, this setting is invalid and input capture is not generated.

2. When the BFA bit in TMDR_6 is set to 1 and TGRC_6 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

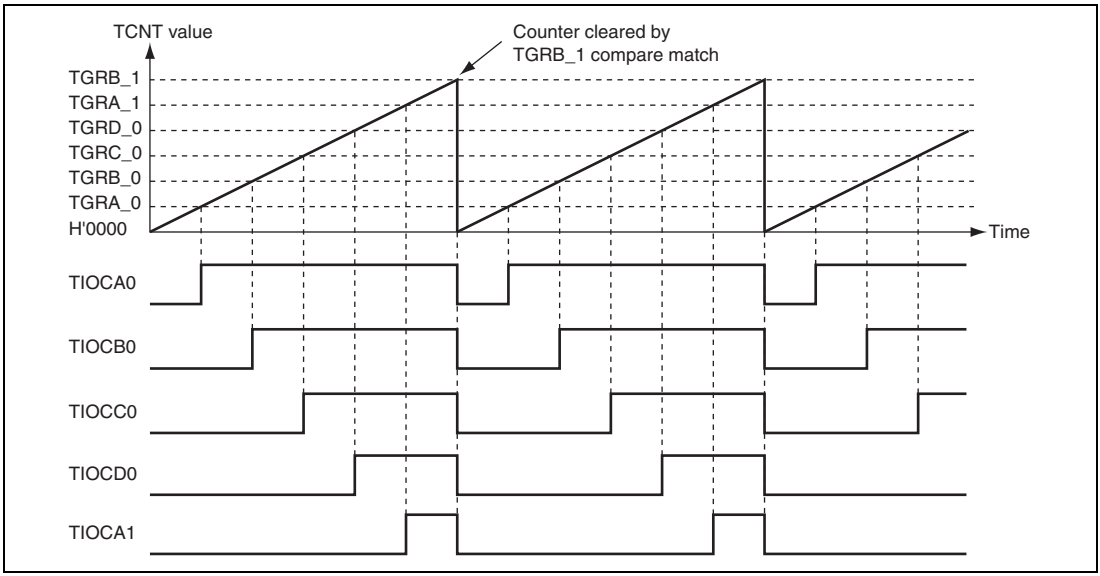

Figure 14.23 Example of PWM Mode Operation (2)

Figure 14.24 shows examples of PWM waveform output with 0% duty cycle and 100% duty cycle in PWM mode.

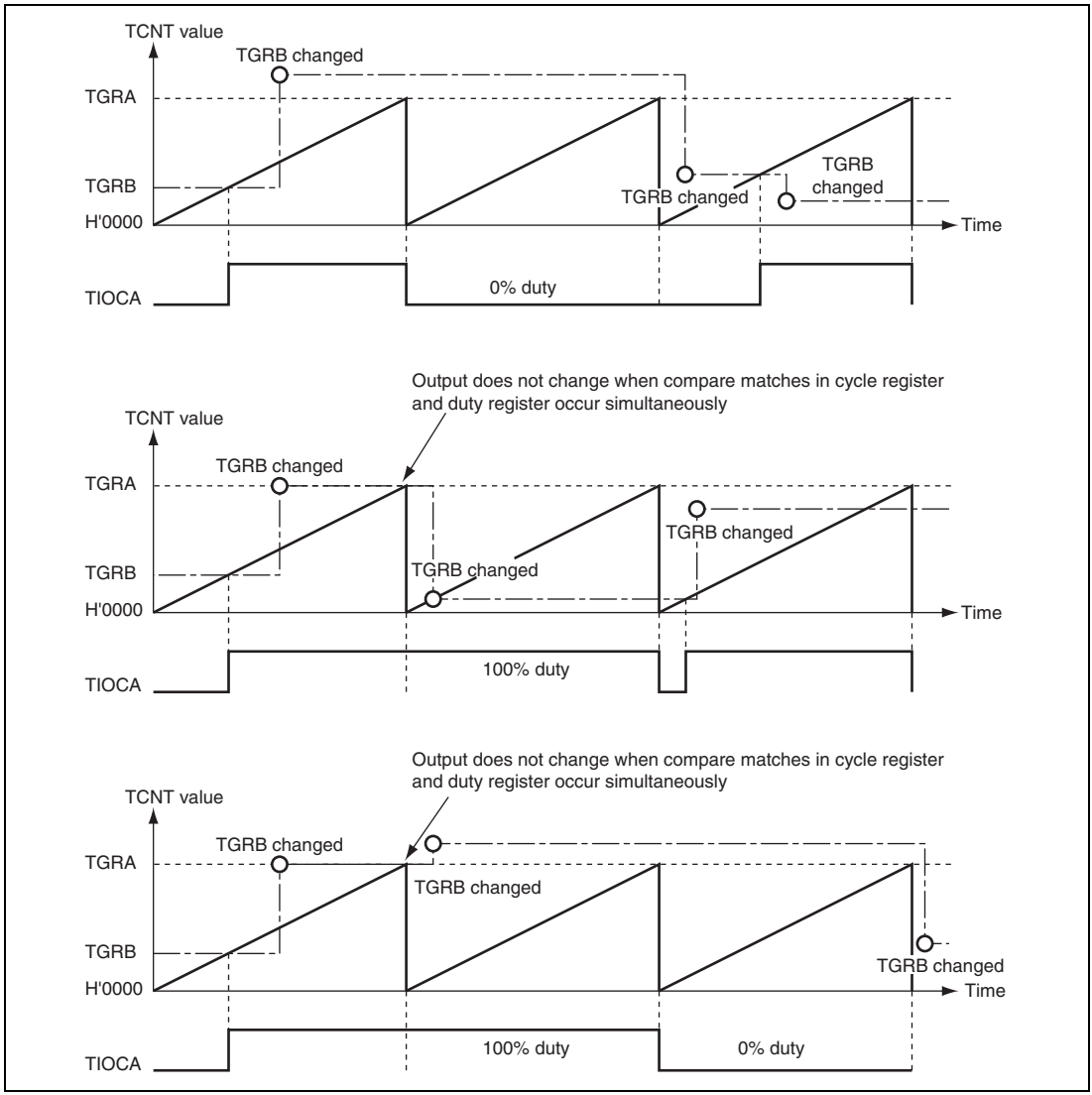

Figure 14.24 Example of PWM Mode Operation (3)

19.5 Operation

19.5.1 Cable Connection

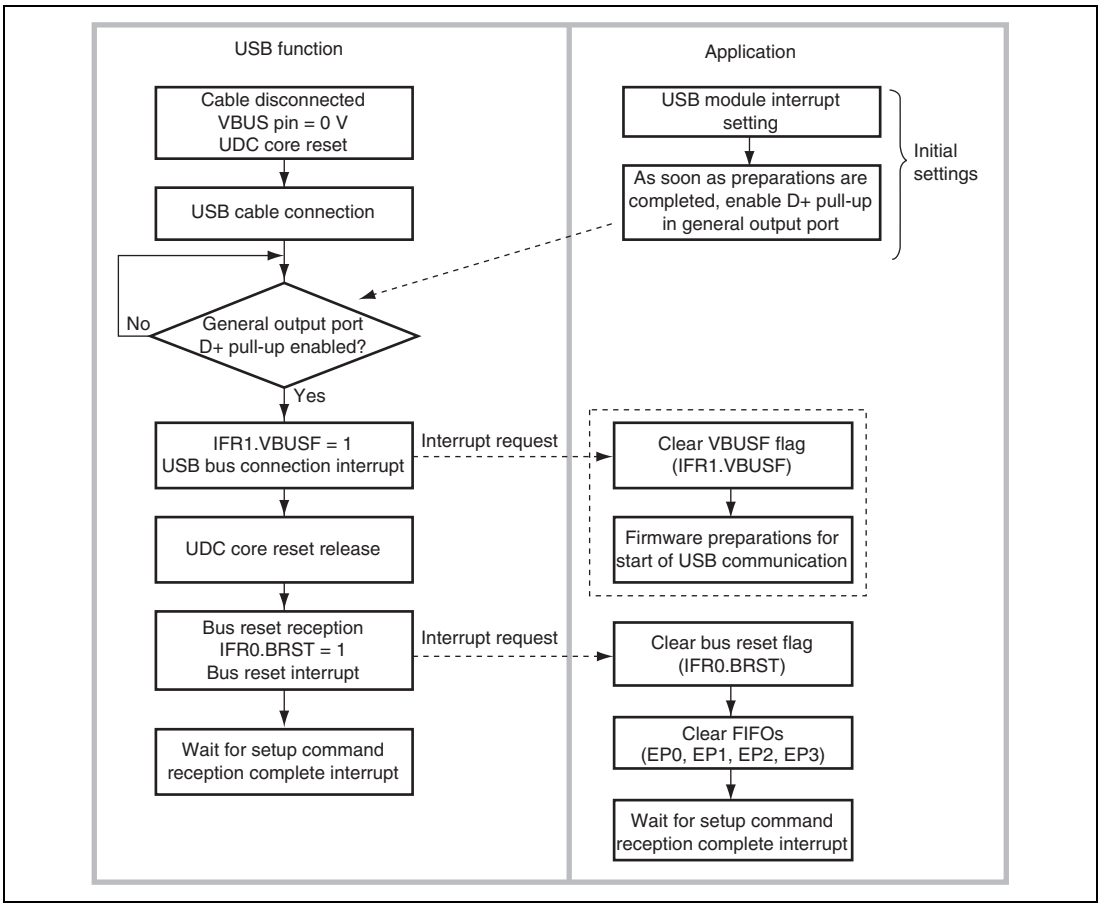

Figure 19.2 Cable Connection Operation

The above flowchart shows the operation in the case of in section 19.9, Example of USB External Circuitry.

In applications that do not require USB cable connection to be detected, processing by the USB bus connection interrupt is not necessary. Preparations should be made with the bus-reset interrupt.

25.6 Usage Notes

1. In serial transfer, data are input or output in LSB order (see figure 25.3).

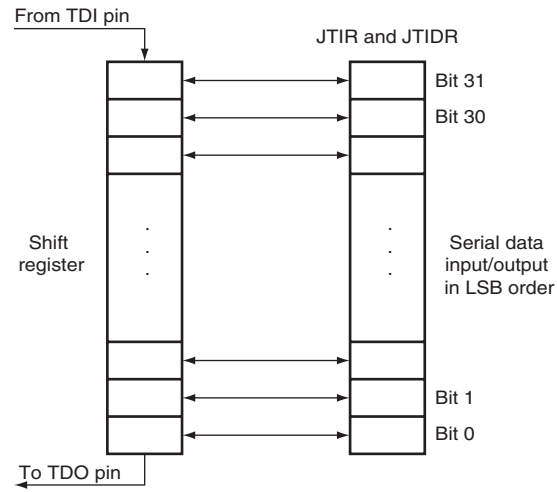

Figure 25.3 Serial Data Input/Output

2. If a pin with open-drain function is SAMPLEed while its open-drain function is enabled and while the corresponding OUT register is set to 1, the corresponding Control register is cleared to 0 (the pin status is Hi-Z). If the pin is SAMPLEed while the corresponding OUT register is cleared to 0, the corresponding Control register is 1 (the pin status is 0)
3. Pins of the boundary scan (TCK, TDI, TMS, and $\overline{\text{TRST}}$) have to be pulled up by pull-up resistors.
4. Power supply pins (V_{CC}, V_{CL}, V_{SS}, AV_{CC}, AV_{SS}, AVref, $PLLV_{CC}$, $PLLV_{SS}$, DrV_{CC}, and DrV_{SS}) cannot be boundary-scanned.
5. Clock pins (EXTAL and XTAL) cannot be boundary-scanned.
6. Reset and standby signals ($\overline{\text{RES}}$ and $\overline{\text{STBY}}$) cannot be boundary-scanned.
7. Boundary scan pins (TCK, TMS, $\overline{\text{TRST}}$, TDI, and TDO) cannot be boundary-scanned.
8. The boundary scan function is not available when this LSI are in the following states.

(1) Reset state

(2) Hardware standby mode, software standby mode, and deep software standby mode

29.3 DC Characteristics H8SX/1658M Group

Table 29.4 DC Characteristics (1)

Conditions: V_{CC} = $PLLV_{CC}$ = 2.95 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V*[1], T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	$\overline{IRQ}$ input pin, TPU input pin, TMR input pin, port 2, port J, port K	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.06$	—	—	V	
	$\overline{IRQ0}$-B to $\overline{IRQ7}$-B input pins	VT^-	$AV_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$AV_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$AV_{CC} \times 0.06$	—	—	V	
Input high voltage (except Schmitt trigger input pin)	MD, $\overline{RES}$, $\overline{STBY}$, EMLE, NMI	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} + 0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} + 0.3		
	Other input pins						
	Port 5		$AV_{CC} \times 0.7$	—	AV_{CC} + 0.3		
Input low voltage (except Schmitt trigger input pin)	MD, $\overline{RES}$, $\overline{STBY}$, EMLE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	EXTAL, NMI		–0.3	—	$V_{CC} \times 0.2$		
	Other input pins		–0.3	—	$V_{CC} \times 0.2$		
Output high voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—		I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\overline{RES}$	$\lvert I_{in} \rvert$	—	—	10.0	µA	V_{in} = 0.5 to V_{CC} – 0.5 V
	MD, $\overline{STBY}$, EMLE, NMI		—	—	1.0		
	Port 5		—	—	1.0		V_{in} = 0.5 to AV_{CC} – 0.5 V

Notes: 1. When the A/D and D/A converters are not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.
2. Current consumption values are for V_{IH}min = V_{CC} – 0.5 V and V_{IL}max = 0.5 V with all output pins unloaded and all input pull-up MOSs in the off state.
3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, V_{IH}min = $V_{CC} \times 0.9$, and V_{IL}max = 0.3 V.
4. I_{CC} depends on f as follows:
   I_{CC}max = 30 (mA) + 1.1 (mA/MHz) × f (normal operation)
   I_{CC}max = 35 (mA) + 0.5 (mA/MHz) × f (sleep mode)
5. The values are for reference.
6. This can be applied at power-on.

Table 29.5 Permissible Output Currents

Conditions: V_{CC} = $PLLV_{CC}$ = 2.95 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V*, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Applicable products: H8SX/1658M Group

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	Output pins	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Caution: To protect the LSI's reliability, do not exceed the output current values in table 29.5.

Note: * When the A/D and D/A converters are not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

Item	Page	Revision (See Manual for Details)
20.3.5 I^2C Bus Status Register (ICSR)	945	Deleted The description below for the bit 1 is deleted: [Clearing condition] When 0 is written to this bit after reading AAS = 1 (~~When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.~~)
	946	Deleted The description below for the bit 0 is deleted: [Clearing condition] When 0 is written to this bit after reading ADZ = 1 (~~When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.~~)
20.7 Usage Notes	964	Added 6. Setting of the module stop function
Section 21 A/D Converter 21.3.2 A/D Control/Status Register for Unit 0 (ADCSR_0)	971	Added Descriptions for bit 5 in the register table: Note: Do not write to ADST when activation is by an external trigger. For details, see section 21.7.3, Notes on A/D activation by an External Trigger.
21.3.3 A/D Control/Status Register for Unit 1 (ADCSR_1)	973	Added Descriptions for bit 5 in the register table: Note: Do not write to ADST when activation is by an external trigger. For details, see section 21.7.3, Notes on A/D activation by an External Trigger.
21.3.4 A/D Control/Status Register for Unit 2 (ADCR_0) Unit 0	975	Amended and added The description for bit 7,6, and 0 in the register table: 001: External trigger disabled Note: Do not write to ADST when activation is by an external trigger. For details, see section 21.7.3, Notes on A/D activation by an External Trigger.

Item	Page	Revision (See Manual for Details)
29.9 Power-On Reset Circuit and Voltage-Detection Circuit Characteristics (H8SX/1658M Group)	1293	Added Added due to the addition of the H8SX/1658M Group.
Appendix B. Product Lineup	1300	Replaced Replaced due to the addition of the H8SX/1658M Group
D. Treatment of Unused Pins	1302, 1303	Replaced Replaced due to the addition of the H8SX/1658M Group