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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

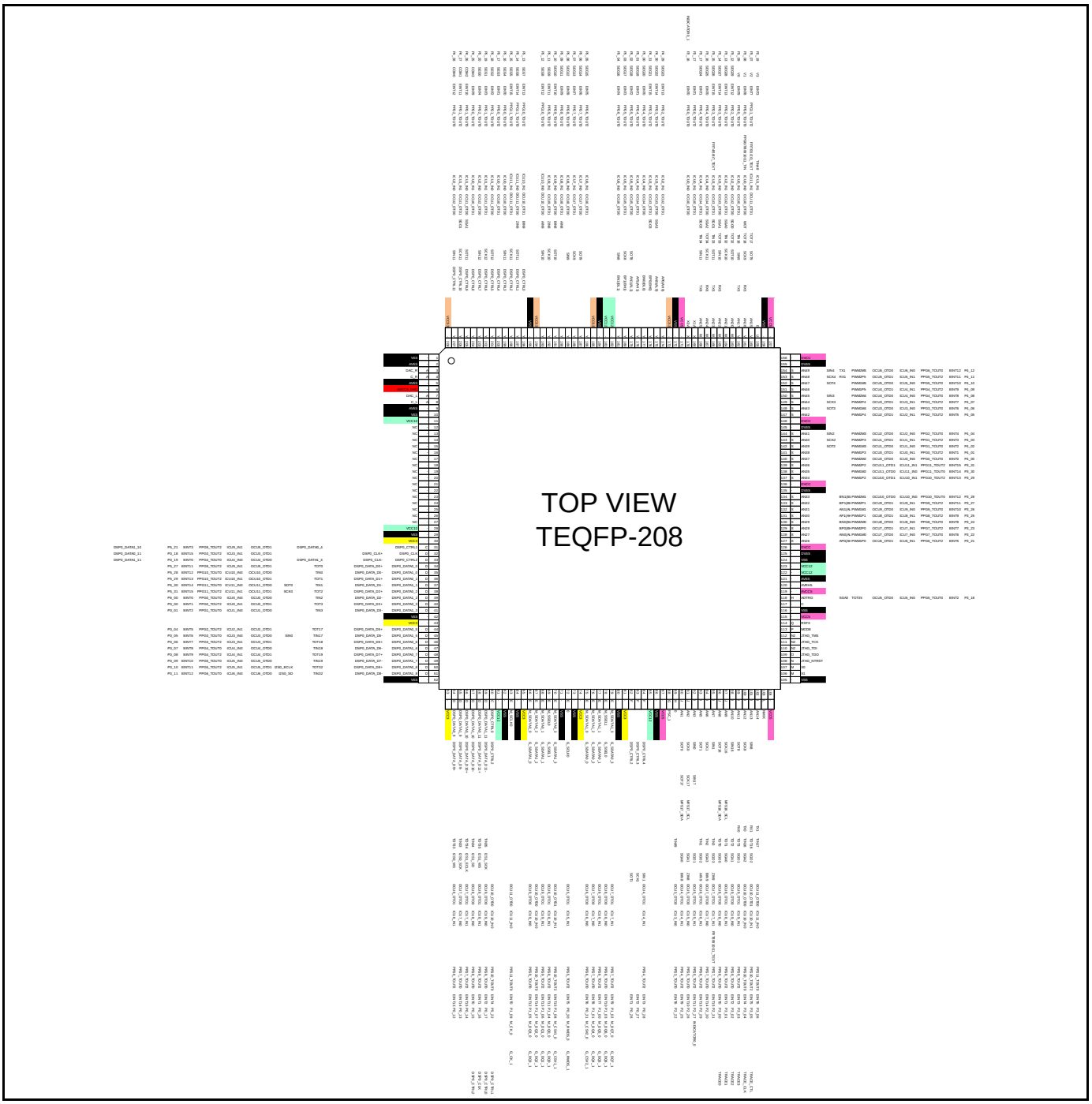
Applications of "Embedded - Microcontrollers"

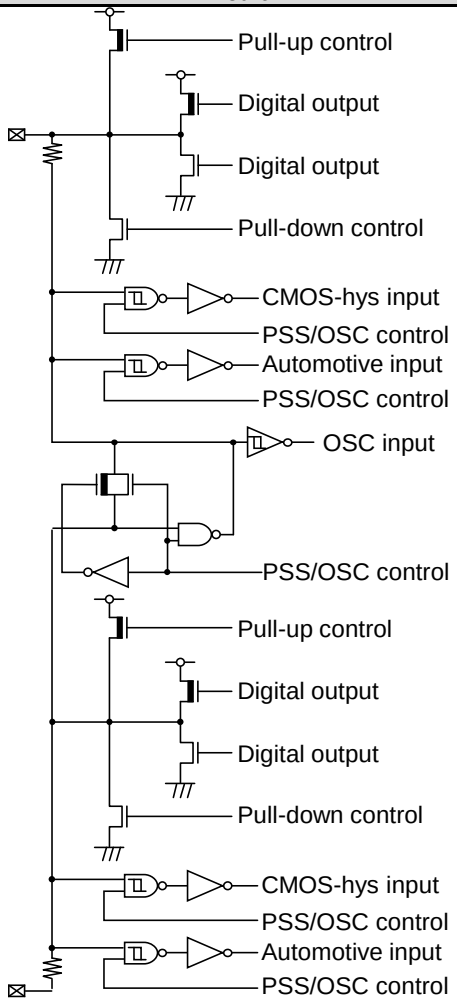
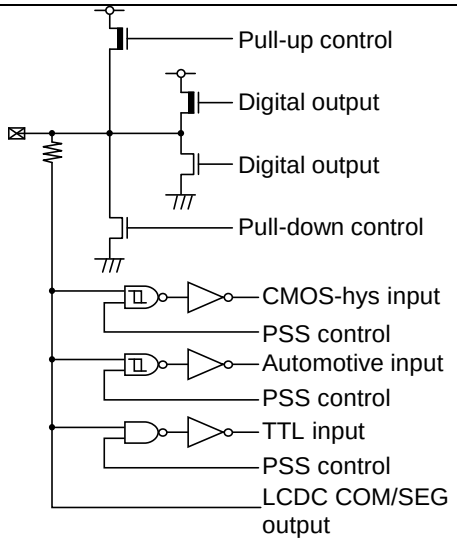
Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-R5F
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	CANbus, CSIO, Ethernet, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2.112MB (2.112M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.15V ~ 5.5V
Data Converters	A/D 50x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-TQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6j324cksmse20000

Table of Contents

Function	Description	Remark
Sound mixer	Option 1 unit x 10 inputs	See 2.2.1
Stereo audio DAC	Option 1 unit (L and R)	See 2.2.1
PCM-PWM	Option 1 unit (L and R)	See 2.2.1
Base timer	12 units (24 ch)	
Free-run timer	12 ch	
Input Capture Unit	12 unit (24channels of capture)	
Output Compare Unit	12unit (24 channels of compare match)	
Stepping motor controller (SMC)	For 6 gauges	
12 bit-A/D converter	Option 1 unit x 50 input ports (Max)	See 2.2.3
CRC	4 unit	
Programmable CRC	1 unit	
Source clock timer	4 ch	
NMI	Available	
External interrupt	16 ch	
Internal interrupt	512 vectors	
I2S	2 ch	One only supports an output as a function of the sound system.
DDR HSSPI	2 ch	A type of Quad SPI
HyperBus (RPC2)	Option	See 2.2.1 See AC specification on the datasheet.
Multi-function serial interface	12 ch	
CAN-FD	4 ch	
CAN-FD RAM (ECC supported)	16KB/ch It equivalents to 128 message buffer per channel of CCAN module	
Ethernet AVB	Option	See 2.2.1
Media-LB (MOST25)	Option	See 2.2.1
LCD controller	Option 4 COM x 32 SEG (Max)	See 2.2.3
Indicator PWM	1 ch	
MPU for AHB	1 unit	
MPU for AXI	1 unit	
Internal VRAM	Option	See 2.2.1
Graphic engine clock	Option	See 2.2.1
Graphic AXI clock	Option	See 2.2.1
Display clock	Option 80 MHz (ch.0), 50 MHz(ch.1)	See 2.2.1
Display clock source	Graphic display controller clock or external clock	
Target frame rate	60 fps	
Number of display outputs	Option Maximum 2 outputs simultaneously	See 2.2.1
TTL output (RGB888)	Option	See 2.2.1
RSDS/TCON support	1 output	
FPD-Link (LVDS)	Option 1 output, 350 Mbps (Max)	See 2.2.1
Video capture unit	Option	See 2.2.1
Video capture format	ITU656, YCbCr4:4:4, YCbCr4:2:2, RGB888, RGB666	
2D Graphic engine	1 unit	
2.5D support	Available	
Vector drawing on 2D engine	Available	
Warping	Available	
Scale/Rotate/Blend	Available	
2D Driver API	CYPRESS proprietary	

Figure 4-17: TEQFP-208 (S6J32xAKxx)



Type	Circuit	Remark
X		– Sub oscillation I/O shared General-purpose I/O port – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input
Y		– General-purpose I/O port with LCDC COM/SEG output – Output 1 mA, 2 mA or 5 mA selectable – 50 kΩ with pull-up resistor control – 50 kΩ with pull-down resistor control – CMOS hysteresis input – Automotive hysteresis input – TTL input

6. Port Description

6.1 Port Description List

The table shows the port function of description which is supported. The port function which is not described in the table is not supported for the product.

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
VCC12	+1.2-V power supply pin	11, 28, 61, 85, 122, 123, 182, 183	11, 28, 63, 87, 128, 129, 190, 191	
VCC5	+5.0-V power supply pin	87, 104, 115, 157, 171	89, 108, 119, 163, 179	
VCC3	+3.3-V power supply pin	30, 43, 53, 65, 74, 81	30, 43, 55, 67, 76, 83	
VCC53	+3.3 V/+5.0 V selection power supply pin	173, 185, 194, 208	181, 193, 202, 216	
VCC3_LVDS_Tx	LVDS Tx power supply pin	14, 27	14, 27	
VSS	GND	1, 10, 29, 42, 52, 62, 64, 71, 73, 80, 86, 105, 116, 124, 158, 172, 184, 195	1, 10, 29, 42, 54, 64, 66, 73, 75, 82, 88, 109, 120, 130, 164, 180, 192, 203	
VSS_LVDS_Tx	LVDS Tx GND	15, 26	15, 26	
AVCC3_DAC	Audio DAC power supply pin	6	6	
AVCC3_LVDS_PLL	LVDS PLL power supply pin	13	13	
AVSS_LVDS_PLL	LVDS PLL GND	12	12	
AVCC5	A/D converter analog power supply pin	119	125	
AVRH5	A/D converter upper limit reference voltage pin	120	126	
AVSS	A/D converter GND	2, 5, 9, 121	2, 5, 9, 127	
DVCC	SMC large current port power supply pin	126, 136, 146,156	132, 142, 152,162	
DVSS	SMC large current port GND	125, 135, 145,155	131, 141, 151, 161	
X1	Main clock oscillator output pin	106	110	
X0	Main clock oscillator input pin	107	111	
X1A	Sub-clock oscillator output	169	177	
X0A	Sub-clock oscillator input	170	178	
NMIX	Non-maskable interrupt input pin	103	107	
RSTX	External reset input pin	114	118	
PSC_1	External Power Supply Control pin	88	90	
MODE	Mode Pin	113	117	
C	External capacity connection output pin	117	121	
JTAG_NTRST	JTAG test reset input pin	108	112	
JTAG_TDO	JTAG test data output pin	109	113	
JTAG_TDI	JTAG test data input pin	110	114	
JTAG_TCK	JTAG test clock input pin	111	115	
JTAG_TMS	JTAG test mode state input pin	112	116	
TRACE0	Trace data 0 output pin	96	100	
TRACE1	Trace data 1 output pin	97	101	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
EINT11	External interrupt input pin	34, 50, 69, 92, 133, 153, 192, 206	34,52,71, 95,139,159, 170, 200, 214	
EINT12	External interrupt input pin	35, 51, 66, 134, 154, 163, 193, 207	35, 53, 68, 96, 140, 160, 171, 201, 215	
EINT13	External interrupt input pin	36, 54, 68, 93, 137, 164, 174, 196	36, 56, 70, 97, 143, 172, 182, 204	
EINT14	External interrupt input pin	37, 55, 67, 94, 138, 165, 175, 197	37, 57, 69, 98, 144, 173, 183, 205	
EINT15	External interrupt input pin	32, 38, 56, 70, 95, 139, 166, 176, 198	32, 38, 58, 72, 99, 145, 174, 184, 206	
MFS0_CS0	Multi-function serial ch.0 chip select 0 pin	148	154	
MFS0_CS1	Multi-function serial ch.0 chip select 1 pin	153	159	
MFS0_CS2	Multi-function serial ch.0 chip select 2 pin	154	160	
MFS0_CS3	Multi-function serial ch.0 chip select 3 pin	152	158	
MFS2_CS0	Multi-function serial ch.2 chip select 0 pin	149	155	
MFS2_CS1	Multi-function serial ch.2 chip select 1 pin	150	156	
MFS8_CS0	Multi-function serial ch.8 chip select 0 pin	163, 191	171, 199	
MFS8_CS1	Multi-function serial ch.8 chip select 1 pin	167, 198	175, 206	
MFS8_CS2	Multi-function serial ch.8 chip select 2 pin	168, 199	176, 207	
MFS8_CS3	Multi-function serial ch.8 chip select 3 pin	166, 197	174, 205	
MFS9_CS0	Multi-function serial ch.9 chip select 0 pin	164, 192	172, 200	
MFS9_CS1	Multi-function serial ch.9 chip select 1 pin	165, 193	173, 201	
SCK0	Multi-function serial ch.0 clock I/O pin	38, 91	38, 94	
SCK1	Multi-function serial ch.1 clock I/O pin	83, 94	85, 98	
SCK2	Multi-function serial ch.2 clock I/O pin	143	149	
SCK3	Multi-function serial ch.3 clock I/O pin	149	155	
SCK4	Multi-function serial ch.4 clock I/O pin	153	159	
SCK8	Multi-function serial ch.8 clock I/O pin	100, 180	104, 188	
SCK9	Multi-function serial ch.9 clock I/O pin	161, 188	167, 196	
SCK10	Multi-function serial ch.10 clock I/O pin	164, 192	172, 200	
SCK11	Multi-function serial ch.11 clock I/O pin	167, 198, 206	175, 206, 214	
SCK12	Multi-function serial ch.12 clock I/O pin	202	210	
SCK16	Multi-function serial ch.16 clock I/O pin	97	101	
SCK17	Multi-function serial ch.17 clock I/O pin	91	94	
SIN0	Multi-function serial ch.0 serial data input pin	45, 92	47, 95	
SIN1	Multi-function serial ch.1 serial data input pin	84, 95	86, 99	
SIN2	Multi-function serial ch.2 serial data input pin	144	150	
SIN3	Multi-function serial ch.3 serial data input pin	150	156	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
SIN4	Multi-function serial ch.4 serial data input pin	154	160	
SIN8	Multi-function serial ch.8 serial data input pin	101, 181	105, 189	
SIN9	Multi-function serial ch.9 serial data input pin	162, 189	168, 197	
SIN10	Multi-function serial ch.10 serial data input pin	165, 193	173, 201	
SIN11	Multi-function serial ch.11 serial data input pin	168, 199, 207	176, 207, 215	
SIN12	Multi-function serial ch.12 serial data input pin	203	211	
SIN16	Multi-function serial ch.16 serial data input pin	98	102	
SIN17	Multi-function serial ch.17 serial data input pin	92	95	
SOT0	Multi-function serial ch.0 serial data output pin	37, 90	37, 93	
SOT1	Multi-function serial ch.1 serial data output pin	82, 93	84, 97	
SOT2	Multi-function serial ch.2 serial data output pin	142	148	
SOT3	Multi-function serial ch.3 serial data output pin	148	154	
SOT4	Multi-function serial ch.4 serial data output pin	152	158	
SOT8	Multi-function serial ch.8 serial data output pin	99, 179	103, 187	
SOT9	Multi-function serial ch.9 serial data output pin	160, 187	166, 195	
SOT10	Multi-function serial ch.10 serial data output pin	163, 191	171, 199	
SOT11	Multi-function serial ch.11 serial data output pin	166, 197, 205	174, 205, 213	
SOT12	Multi-function serial ch.12 serial data output pin	201	209	
SOT16	Multi-function serial ch.16 serial data output pin	96	100	
SOT17	Multi-function serial ch.17 serial data output pin	90	93	
SCL4 (MFS4_SCL)	I^2C ch.4 clock I/O pin	153	159	
SCL10 (MFS10_SCL)	I^2C ch.10 clock I/O pin	192	200	
SCL12 (MFS12_SCL)	I^2C ch.12 clock I/O pin	202	210	
SCL16 (MFS16_SCL)	I^2C ch.16 clock I/O pin	97	101	
SCL17 (MFS17_SCL)	I^2C ch.17 clock I/O pin	91	94	
SDA4 (MFS4_SDA)	I^2C ch.4 serial data I/O pin	152	158	
SDA10 (MFS10_SDA)	I^2C ch.10 serial data I/O pin	191	199	
SDA12 (MFS12_SDA)	I^2C ch.12 serial data I/O pin	201	209	
SDA16 (MFS16_SDA)	I^2C ch.16 serial data I/O pin	96	100	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
OCU5_OTD1	Output compare 5 ch.1 output pin	50, 72, 92, 153, 180	52, 74, 95, 123, 159, 188	
OCU6_OTD0	Output compare 6 ch.0 output pin	51, 75, 154, 181	53, 77, 96, 124, 160, 189	
OCU6_OTD1	Output compare 6 ch.1 output pin	54, 77, 93, 127, 186	56, 79, 97, 133, 194	
OCU7_OTD0	Output compare 7 ch.0 output pin	55, 76, 94, 128, 187	57, 78, 98, 134, 195	
OCU7_OTD1	Output compare 7 ch.1 output pin	56, 79, 95, 129, 188	58, 81, 99, 135, 196	
OCU8_OTD0	Output compare 8 ch.0 output pin	57, 78, 96, 130, 189	59, 80, 100, 136, 197	
OCU8_OTD1	Output compare 8 ch.1 output pin	58, 69, 97, 131, 190	60, 71, 101, 137, 198	
OCU9_OTD0	Output compare 9 ch.0 output pin	59, 66, 98, 132, 191	61, 68, 102, 138, 199	
OCU9_OTD1	Output compare 9 ch.1 output pin	31, 34, 68, 99, 133, 192	31, 34, 70, 103, 139, 200	
OCU10_OTD0	Output compare 10 ch.0 output pin	35, 60, 67, 100, 134, 193	35, 62, 69, 104, 140, 201	
OCU10_OTD1	Output compare 10 ch.1 output pin	36, 70, 101, 137, 196	36, 72, 105, 143, 204	
OCU11_OTD0	Output compare 11 ch.0 output pin	37, 63, 102, 138, 197	37, 65, 106, 144, 205	
OCU11_OTD1	Output compare 11 ch.1 output pin	38, 139, 160, 198	38, 145, 166, 206	
ICU0_IN0	Input Capture 0 ch.0 input pin	39, 140, 161, 170, 199	39, 146, 167, 178, 207	
ICU0_IN1	Input Capture 0 ch.1 input pin	40, 141, 162, 169, 200, 204	40, 147, 168, 177, 208, 212	
ICU1_IN0	Input Capture 1 ch.0 input pin	41, 142, 201, 205	41, 148, 169, 209, 213	
ICU1_IN1	Input Capture 1 ch.1 input pin	143, 159, 202, 206	44, 149, 165, 170, 210, 214	
ICU2_IN0	Input Capture 2 ch.0 input pin	144, 163, 203, 207	45, 150, 171, 211, 215	
ICU2_IN1	Input Capture 2 ch.1 input pin	44, 147, 164, 174	46, 153, 172, 182	
ICU3_IN0	Input Capture 3 ch.0 input pin	45, 89, 148, 165, 175	47, 91, 154, 173, 183	
ICU3_IN1	Input Capture 3 ch.1 input pin	32, 46, 149, 166, 176	32, 48, 155, 174, 184	
ICU4_IN0	Input Capture 4 ch.0 input pin	33, 47, 150, 167, 177	33, 49, 92, 156, 175, 185	
ICU4_IN1	Input Capture 4 ch.1 input pin	48, 84, 90, 151, 168, 178	50, 86, 93, 157, 176, 186	
ICU5_IN0	Input Capture 5 ch.0 input pin	49, 91, 118, 152, 179	51, 94, 122, 158, 187	

Port Name	Description	Package Pin Number		Remark
		TEQFP208	TEQFP216	
P3_31	General-Purpose I/O port	139	145	
P4_00	General-Purpose I/O port	140	146	
P4_01	General-Purpose I/O port	141	147	
P4_02	General-Purpose I/O port	142	148	
P4_03	General-Purpose I/O port	143	149	
P4_04	General-Purpose I/O port	144	150	
P4_05	General-Purpose I/O port	147	153	
P4_06	General-Purpose I/O port	148	154	
P4_07	General-Purpose I/O port	149	155	
P4_08	General-Purpose I/O port	150	156	
P4_09	General-Purpose I/O port	151	157	
P4_10	General-Purpose I/O port	152	158	
P4_11	General-Purpose I/O port	153	159	
P4_12	General-Purpose I/O port	154	160	
P4_25	General-Purpose I/O port	204	212	
P4_26	General-Purpose I/O port	205	213	
P4_27	General-Purpose I/O port	206	214	
P4_28	General-Purpose I/O port	207	215	
P4_29	General-Purpose I/O port	174	182	
P4_30	General-Purpose I/O port	175	183	
P4_31	General-Purpose I/O port	176	184	
P5_00	General-Purpose I/O port	177	185	
P5_01	General-Purpose I/O port	178	186	
P5_02	General-Purpose I/O port	179	187	
P5_03	General-Purpose I/O port	180	188	
P5_04	General-Purpose I/O port	181	189	
P5_05	General-Purpose I/O port	186	194	
P5_06	General-Purpose I/O port	187	195	
P5_07	General-Purpose I/O port	188	196	
P5_08	General-Purpose I/O port	189	197	
P5_09	General-Purpose I/O port	190	198	
P5_10	General-Purpose I/O port	191	199	
P5_11	General-Purpose I/O port	192	200	
P5_12	General-Purpose I/O port	193	201	
P5_13	General-Purpose I/O port	196	204	
P5_14	General-Purpose I/O port	197	205	
P5_15	General-Purpose I/O port	198	206	
P5_16	General-Purpose I/O port	199	207	
P5_17	General-Purpose I/O port	200	208	
P5_18	General-Purpose I/O port	201	209	
P5_19	General-Purpose I/O port	202	210	
P5_20	General-Purpose I/O port	203	211	
P5_21	General-Purpose I/O port	31	31	
P5_22	General-Purpose I/O port	60	62	
P5_27	General-Purpose I/O port	34	34	
P5_28	General-Purpose I/O port	35	35	
P5_29	General-Purpose I/O port	36	36	
P5_30	General-Purpose I/O port	37	37	
P5_31	General-Purpose I/O port	38	38	

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this datasheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

Notes:

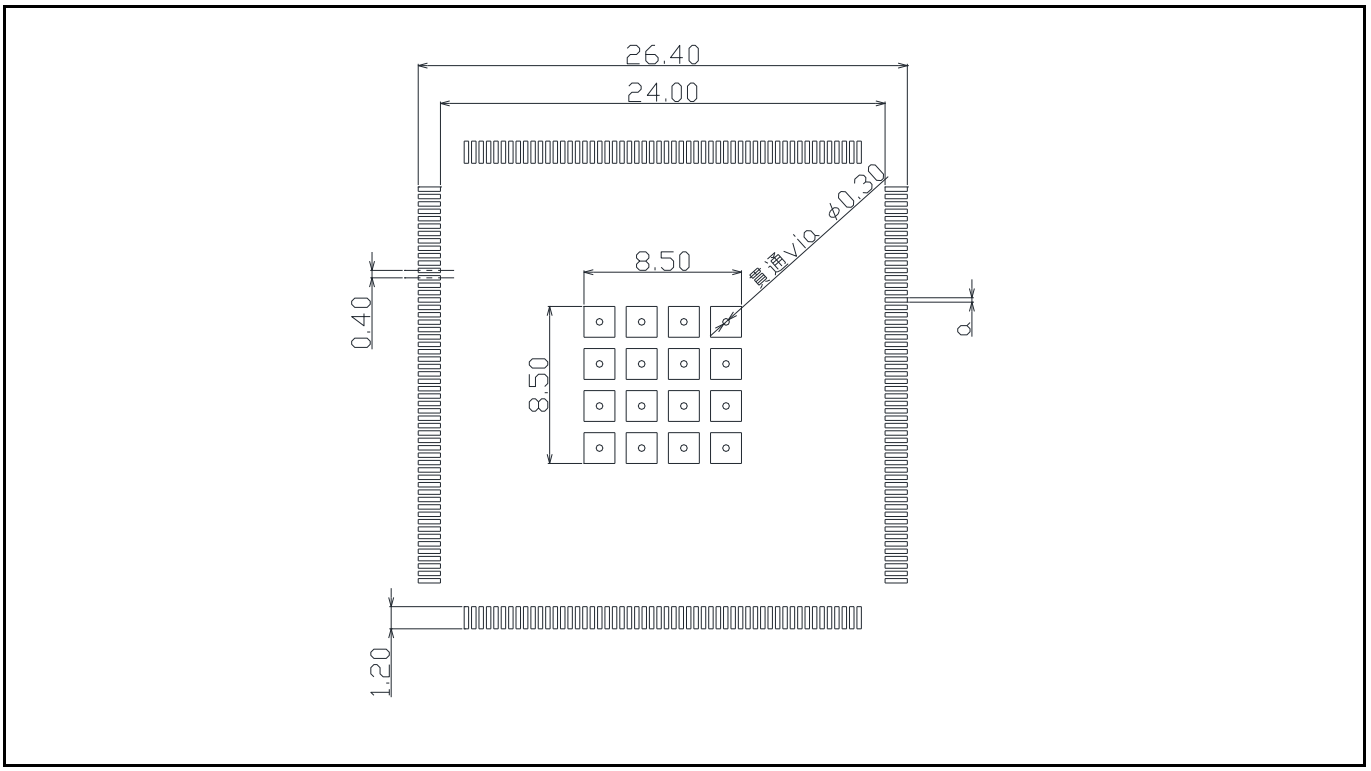
- *T_A: Ambient temperature (JEDEC)*
- *T_C: Case temperature (JEDEC), the maximum measured temperature of package case top.*
- *Both rating of T_A and T_C should simultaneously be satisfied as maximum operation temperature.*
- *The following condition should be satisfied in order to facilitate heat dissipation.*
    1. *Four or more layers PCB should be used.*
    2. *The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)*
    3. *One layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90% or more. The layer can be used for system ground.*
    4. *35% or more of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.*
    5. *The part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.*

Figure 8-1: Example thermal via holes on PCB.

Notes:

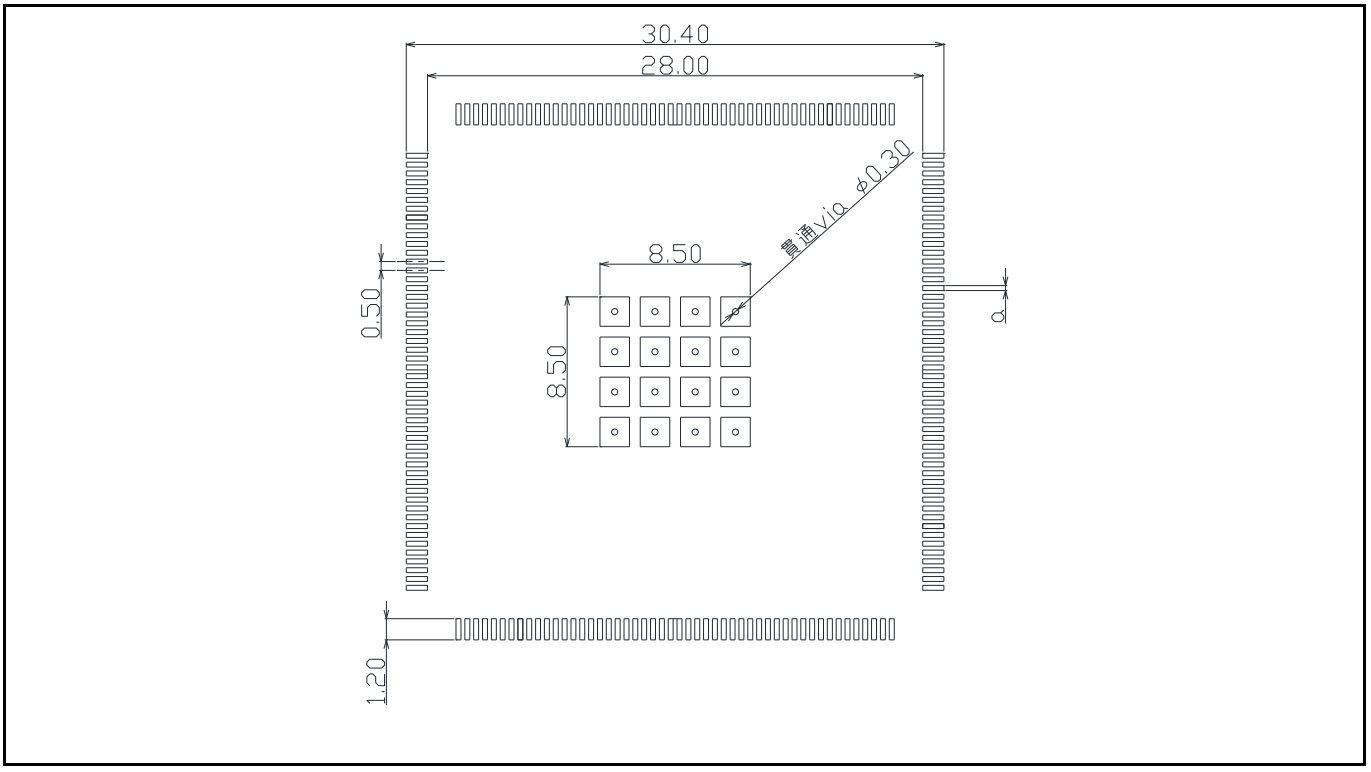
- *Figure 8-1 is a schematic diagram showing PCB in section.*
- *Figure 8-2, Figure 8-3, and Figure 8-4 in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.*
- *When thermal via holes cannot be with lands, the followings are recommended as represented by Figure 8-5 which is an example for LEQ216.*
- *(1). Increase pattern area size as much as possible inside the package outline.*
- *(2). Place thermal via holes to be with lands as close as possible.*
- *0.25 mm $\leq a \leq$ 0.30 mm in Figure 8-1, Figure 8-2, Figure 8-3, and Figure 8-4*
- *It is recommended to connect the land pattern to the VSS-ground level (GND plan of inner layer bellow the MCU) as thermal heat sink.*

Figure 8-2: Land Pattern and Thermal Via LEQ216

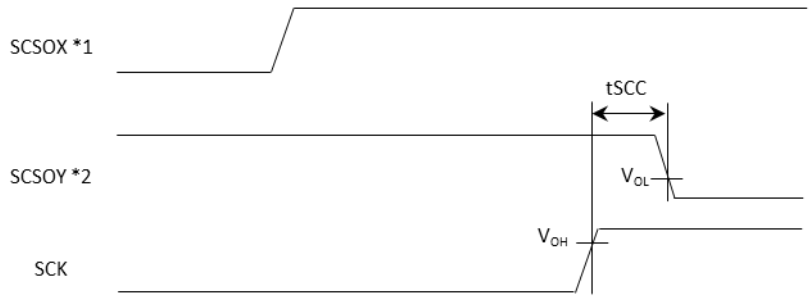


0.25 mm ≤ a ≤ 0.30 mm

Figure 8-3: Land Pattern and Thermal Via LET208



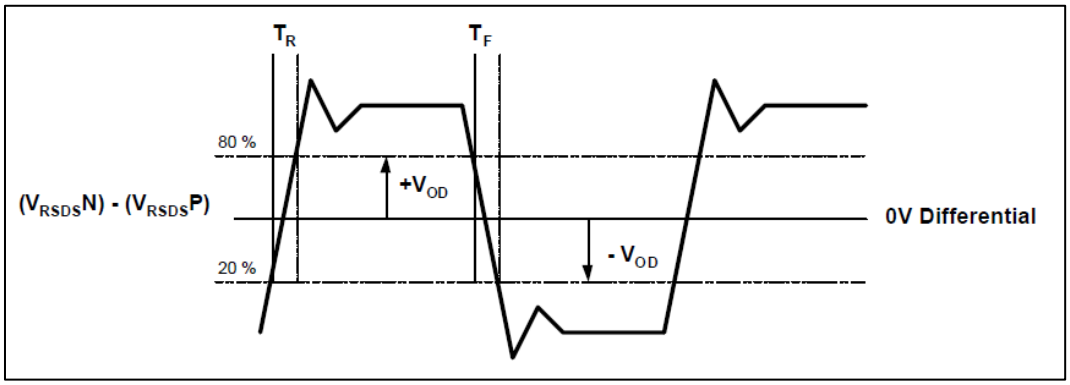
0.25 mm ≤ a ≤ 0.30 mm



Round Function (CSxSCINV=1, CSxLVL=1), (CSySCINV=0, CSyLVL=1)

*1: X is 0 to 3.

*2: Y is 0 to 3. However, Y and X is a different value.


T_R
T_F
80 %
20 %
$+V_{OD}$
$-V_{OD}$
$(V_{RSDS}N) - (V_{RSDS}P)$
0V Differential

8.4.21 QPRC

(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
"H" width of AIN	tAHL	AIN	—	4tCLK_LCP1A	—	ns	
"L" width of AIN	tALL	AIN	—	4tCLK_LCP1A	—		
"H" width of BIN	tBHL	BIN	—	4tCLK_LCP1A	—	ns	
"L" width of BIN	tBLL	BIN	—	4tCLK_LCP1A	—	ns	
Rising timing of BIN from "H" level of AIN	tAUBU	BIN	PC_Mode2 or PC_mode3	4tCLK_LCP1A	—	ns	
Falling timing of AIN from "H" level of BIN	tBUAD	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of BIN from "L" level of AIN	tADBD	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of AIN from "L" level of BIN	tBDAU	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of AIN from "H" level of BIN	tBUAU	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of BIN from "H" level of AIN	tAUBD	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Falling timing of AIN from "L" level of BIN	tBDAD	AIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
Rising timing of BIN from "L" level of AIN	tADBU	BIN	PC_Mode2 or PC_Mode3	4tCLK_LCP1A	—	ns	
"H" width of ZIN	tZHL	ZIN	QCR:CGSC="0"	4tCLK_LCP1A	—	ns	
"L" width of ZIN	tZLL	ZIN	QCR:CGSC="0"	4tCLK_LCP1A	—	ns	
Rising or falling timing of AIN/BIN from level valid timing of ZIN	tZABE	AIN/BIN	QCR:CGSC="1"	4tCLK_LCP1A	—	ns	
Level valid timing of ZIN from falling or rising timing of AIN/BIN	tABEZ	ZIN	QCR:CGSC="1"	4tCLK_LCP1A	—	ns	

Notes:

- *t is the period of peripheral clock(CLK)*

8.4.22 I2S

8.4.22.1 I2S Timing – Master mode (MSMD=1)

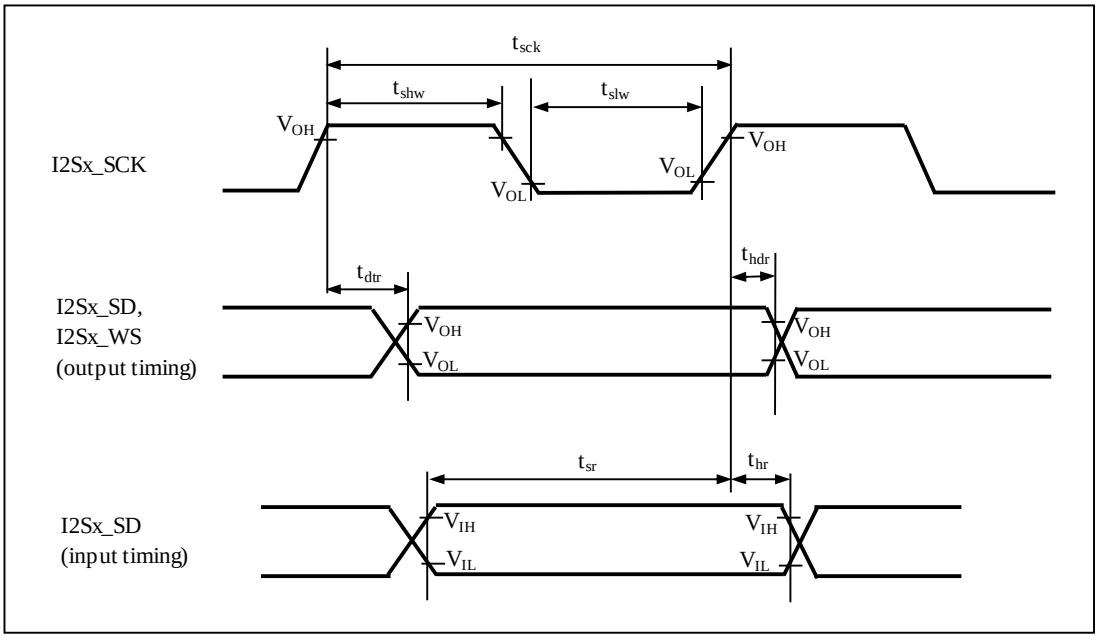
(Condition: See 8.2. Operation Assurance)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
ECLK0/ECLK1 clock cycle	t_{eck}	ECLK0, ECLK1	(CL = 20 pF, I_{OL}=-5 mA, I_{OH}=5 mA) CPOL=0, SMPL=1	20	-	ns	Only relevant if external ECLK input is selected. *1
ECLK0/ECLK1 clock "H" pulse width	t_{ehw}			0.40* t_{eck}	0.60* t_{eck}	ns	
ECLK0/ECLK1 clock "L" pulse width	t_{elw}			0.40* t_{eck}	0.60* t_{eck}	ns	
I2S clock cycle (output SCK)	t_{sck}	I2S0_SCK, I2S1_SCK		66.66	-	ns	
I2S clock "H" pulse width	t_{shw}			0.35* t_{sck}	0.65* t_{sck}	ns	
I2S clock "L" pulse width	t_{slw}			0.35* t_{sck}	0.65* t_{sck}	ns	
Sender delay time SCK↑ -> SD/WS valid	t_{dtr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD, I2S0_WS, I2S1_WS		-	26	ns	*2
Sender hold time SCK↑ -> SD/WS invalid	t_{htr}			-10	-	ns	*2
Receiver setup time SD valid -> SCK↑	t_{sr}	I2S0_SCK, I2S1_SCK, I2S0_SD, I2S1_SD		21	-	ns	*2
Receiver hold time SCK↑ -> SD valid	t_{hr}			10	-	ns	*2

Notes:

*1: ECKM = 1. Refer to the Resource Input Configuration chapter in TRM for required RESSEL register settings.

*2: Refer to the I2S register description chapter in TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values as per above table will remain the same.

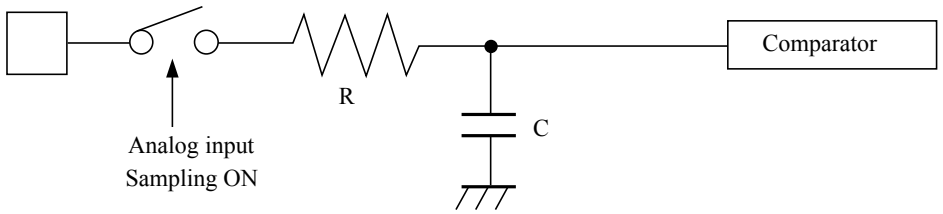


8.5.2 Notes on A/D Converters

About the Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 µF) to an analog input pin.

Analog input circuit model



R	C		
12-bit A/D	3.9 kilo ohms (max)	11.0 pF (max)	(4.5 V≤AV_{CC}≤5.5 V)

Note: Use the numerical values provided here simply as a guide.

8.5.3 Glossary

Resolution: Analog change that can be identified by an A/D converter

Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics

Includes zero transition error, full-scale transition error, and non-linearity error.

Differential linearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB

Total error: Difference between the actual value and the theoretical value.

8.5.4 Calibration Condition

Calibration Condition should be the followings.

- AVCC=5.0 V
- AVRH=5.0 V
- Ta=25℃
- system clock frequency (CLK_LCP1A)= 10 MHz

See A/D Converter Calibration in the S6J3200 hardware manual.

8.7 Flash Memory

8.7.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max*3		
Sector erase time	-	300	1100	ms	8kB sector*1 Internal preprogramming time included
	-	800	3700	ms	64kB sector*1 Internal preprogramming time included
8 bit write time	-	15	288	µs	System-level overhead time excluded*1
16 bit write time	-	19	384	µs	System-level overhead time excluded*1
32 bit write time	-	27	567	µs	System-level overhead time excluded*1
64 bit write time	-	45	945	µs	System-level overhead time excluded*1
8 bit (with ECC) write time	-	19	384	µs	System-level overhead time excluded*1
16 bit (with ECC) write time	-	23	483	µs	System-level overhead time excluded*1
32 bit (with ECC) write time	-	31	651	µs	System-level overhead time excluded*1
64 bit (with ECC) write time	-	49	1029	µs	System-level overhead time excluded*1
Erase count*2 / Data retention time	1,000/20 years 10,000/10 years 100,000/5 years	-	-	-	Temperature at write/erase time Average temperature T_A=+85 degrees Celsius

Notes:

- **1: Guaranteed value for up to 100,000 erases*
- **2: Number of erases for each sector*

8.7.2 Notes

□ For revision M

While the Flash memory is written or erased, shutdown of the external power (Vcc5 and Vcc12) is prohibited.

In the application system, where Vcc5 and Vcc12 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function or external reset (RSTX).

For external power supply voltage stability conditions please see chapter 8.4.4.2 and 8.4.10.4.

□ For except revision M

While the Flash memory is written or erased, shutdown of the external power (V_{CC}5 and Vcc12) is prohibited.

In the application system where V_{CC}5 and Vcc12 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC}5 at 2.7 V or more and Vcc12 at 1.1 V or more within the duration calculated by the following expression:

Td*1 [µs] + (1 / F_{CRF}*2[MHz]) x 1029 + 25 [µs]

*1: See "8.4.10 Low-Voltage Detection"

*2: See "8.4.1 Source Clock "

9. Abbreviation

Abbreviation	Definition	Remark
A/D converter	Analog to Digital Converter	
ADC	Analog to Digital Converter	
AHB	Advanced High performance Bus	
AMBATM	Advanced Microcontroller Bus Architecture	
APB	Advanced Peripheral Bus	
ATCM	TCM-A port	
AXI	Advanced eXtensible Interface	
B0TCM	TCM B0 port	
B1TCM	TCM B1 port	
BBU	Bit Banding Unit	
BDR	Boot Description Record	
BT	Base Timer	
BTL	Bridge-Tied Load	
CAN	Control Area Network	
CD	Clock Domain	
CPU	Central Processing Unit	
CR	CR Oscillator	
CRC	Cyclic Redundancy Check	
CSV	Clock SuperVisor	
DAC	Digital Analog Converter	
DAP	Debug Access Port	
DED	Dual Error Detection	
DMA	Direct Memory Access	
DMAC	DMA Controller	
EAM	Exclusive Access Memory	
ECC	Error Correction Code	
ETM	Embedded Trace Macro	
EXT-IRC	External InteRrupt Controller	
FIQ	Fast Interrupt Request	
FPU	Floating Point Unit	
FRT	Free-Run Timer	
GPIO	General Purpose I/O	
HPM	High Performance Matrix	
HW-WDT	Hardware Watchdog Timer	
I/O	Input or Output	
I2S	Inter-IC Sound	
ICU	Input Capture Unit	
IPCU	Inter-Processor Communication Unit	
IRC	InteRrupt Controller	
IRQ	InteRrupt Request	
ISR	Interrupt Service Routine	
JTAG	Joint Test Action Group	
LLPP	Low Latency Peripheral Port	
LVD	Low Voltage Detector	
MCU	MicroController Unit	
MFS	Multi-Function Serial interface	
MLB	Media LB	

Summary	Error Page	Error	Correct Page	Correct	ID
Original document code: DS708-00003-0v04-E, Previous document code: DS708-00003-0v03-E					
Rev. 1.0 June 30, 2015					
FPD-Link port definition	45	-	60-61	TxCLK- LVDS clock output pin: Described as TXOUT4M in FPD-Link Converter TxCLK+ LVDS clock output pin: Described as TXOUT4P in FPD-Link Converter TxDOUT0- LVDS data output pin: Described as TXOUT0M in FPD-Link Converter TxDOUT0+ LVDS data output pin: Described as TXOUT0P in FPD-Link Converter TxDOUT1- LVDS data output pin: Described as TXOUT1M in FPD-Link Converter TxDOUT1+ LVDS data output pin: Described as TXOUT1P in FPD-Link Converter TxDOUT2- LVDS data output pin: Described as TXOUT2M in FPD-Link Converter TxDOUT2+ LVDS data output pin: Described as TXOUT2P in FPD-Link Converter TxDOUT3- LVDS data output pin: Described as TXOUT3M in FPD-Link Converter TxDOUT3+ LVDS data output pin: Described as TXOUT3P in FPD-Link Converter	#146
Non support port	21, 23	-	25, 27, 28, 29, 32, 34, 35, 36	(Added the Note for non-supported pin condition on PCB)	#215
Current consumption of FPD link	70	VCC3_LVDS_Tx, AVCC3_LVDS_PLL: 70 mA(max)	92	VCC3_LVDS_TX: 56mA(max) AVCC3_LVDS_PLL: 7mA(max)	#246
AVcc and AVRH description	58	(AVCC0, AVCC1, AVRH0, and AVRH1)	73	(AVCC,AVRH)	#250
TEQFP256 support	11	Pin count N:320	12	Pin count M:256	#272

Document History

Document Title: S6J3200 Series 32-bit Microcontroller Traveo™ Family
Document Number: 002-05682

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NNAS	09/30/2015	Migrated to Cypress and assigned document number 002-05682. No change to document contents or format.
*A	5234352	NNAS	04/22/2016	Updated formatting
*B	5340908	NNAS	07/08/2016	2. Function List 2.1 Function List [Improve] Corrected the number of CRC unit. (1unit -> 4unit)
				2. Function List 2.2.1 Basic Option 2.2.2 ID [Improve] Updated the "Option and Part Number", "Function Digit table" and "ID" table for adding new revision and improving readability.
				2. Function List 2.2.2 ID [Improve] Added the value of Platform ID in SYSC0_SYSPFIDR
				3. Product Description 3.2 Product Description [Enhancement] Added support for center spread mode with limited condition
				3. Product Description 3.2 Product Description [Improve] Added the description for "MK_CEER" of security
				3. Product Description 3.2 Product Description [Improve] Added the description for hot swap function of I2C
				3. Product Description 3.2 Product Description [Improve] Added the explanation for function of PSC1.
				3. Product Description 3.2 Product Description [Improve] Added the explanation for reset of EX5VRST.
				3. Product Description 3.2 Product Description [Improve] Added the information of main oscillation stabilization wait time.
				3. Product Description 3.2 Product Description [Improve] Added the register information of "Interrupt Enable Register" (HYPERBUSIn_IEN) for clarifying "not support".
				3. Product Description 3.2 Product Description [Improve] Corrected the number of I2C support ports for MFS.
				3. Product Description 3.2 Product Description [Improve] Corrected the revision digit information for Ethernet AVB.
				3. Product Description 3.2 Product Description [Improve] Corrected the stabilization time for embedded CR oscillation.
				3. Product Description 3.2 Product Description [Improve] For convenience to understand power domain definition.