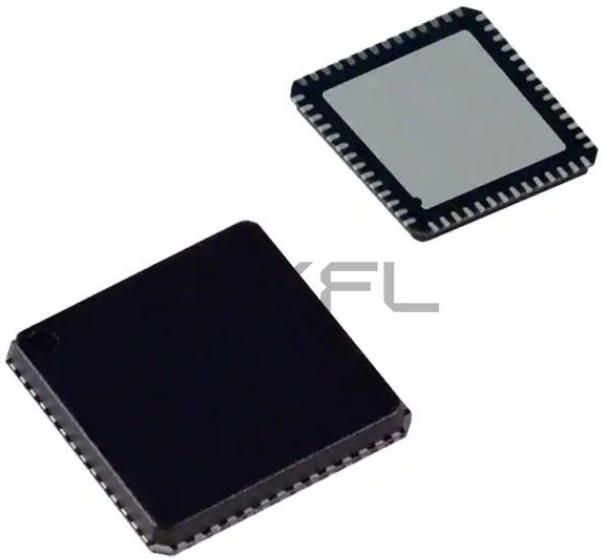

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc845bcpz8-5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Normal Mode Rejection 50 Hz/60 Hz[2]					
On AIN	75			dB	50 Hz/60 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off
Analog Input Current[2]			±1	nA	T_{MAX} = 85°C, buffer on
			±5	nA	T_{MAX} = 125°C, buffer on
Analog Input Current Drift		±5		pA/°C	T_{MAX} = 85°C, buffer on
		±15		pA/°C	T_{MAX} = 125°C, buffer on
Average Input Current		±125		nA/V	±2.56 V range, buffer bypassed
Average Input Current Drift		±2		pA/V/°C	Buffer bypassed
Absolute AIN Voltage Limits[2]	A_{GND} + 0.1		AV_{DD} − 0.1	V	AIN1 … AIN10 and AINCOM with buffer enabled
Absolute AIN Voltage Limits[2]	A_{GND} − 0.03		AV_{DD} + 0.03	V	AIN1 … AIN10 and AINCOM with buffer bypassed
EXTERNAL REFERENCE INPUTS					
REFIN(+) to REFIN(–) Voltage		2.5		V	REFIN refers to both REFIN and REFIN2
REFIN(+) to REFIN(–) Range[2]	1		AV_{DD}	V	REFIN refers to both REFIN and REFIN2
Average Reference Input Current		±1		µA/V	Both ADCs enabled
Average Reference Input Current Drift		±0.1		nA/V/°C	
NOXREF Trigger Voltage	0.3		0.65	V	NOXREF (ADCSTAT.4) bit active if V_{REF} > 0.3 V, and inactive if V_{REF} > 0.65 V
Common-Mode Rejection					
DC Rejection		125		dB	AIN = 1 V, range = ±2.56 V
50 Hz/60 Hz Rejection[2]	90			dB	50 Hz/60 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 82
Normal Mode Rejection 50 Hz/60 Hz[2]	75			dB	50 Hz/60 Hz ±1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop off
AUXILIARY ADC (ADuC845 Only)					
Conversion Rate	5.4		105	Hz	Chop on
	16.06		1365	Hz	Chop off
No Missing Codes[2]	24			Bits	≤26.7 Hz update rate, chop enabled
	24			Bits	80.3 Hz update rate, chop disabled
Resolution	See Table 19 and Table 21				
Output Noise	See Table 18 and Table 20				Output noise varies with selected update rates.
Integral Nonlinearity			±15	ppm of FSR	1 LSB_{16}
Offset Error[3]		±3		µV	Chop on
		±0.25		LSB_{16}	Chop off
Offset Error Drift[2]		10		nV/°C	Chop on
		200		nV/°C	Chop off
Full-Scale Error[4]		±0.5		LSB_{16}	
Gain Error Drift[4]		±0.5		ppm/°C	
Power Supply Rejection	80			dB	AIN = 1 V, range = ±2.56 V, chop enabled
		80		dB	AIN = 1 V, range = ±2.56 V, chop disabled

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PWM					
–Fxtal		3		µA	
–Fvco		0.5		mA	
TIC		1		µA	
3 V Power Consumption					2.7 V < DV_{DD} < 3.6 V, AV_{DD} = 3.6 V
Normal Mode[11, 12]					
DV_{DD} Current			4.8	mA	Core clock = 1.57 MHz
		9	11	mA	Core clock = 6.29 MHz (CD = 1)
AV_{DD} Current			180	µA	ADC not enabled
Power-Down Mode[11, 12]					
DV_{DD} Current		20	26	µA	T_{MAX} = 85°C; OSC on; TIC on
		29		µA	T_{MAX} = 125°C; OSC on; TIC on
		14	20	µA	T_{MAX} = 85°C; OSC off
		21		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off

[1] Temperature range is for ADuC845BS; for the ADuC847BS and ADuC848BS (MQFP package), the range is –40°C to +125°C. Temperature range for ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) is –40°C to +85°C.
[2] These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[3] System zero-scale calibration can remove this error.
[4] Gain error drift is a span drift. To calculate full-scale error drift, add the offset error drift to the gain error drift times the full-scale input.
[5] In general terms, the bipolar input voltage range to the primary ADC is given by the ADC range = ±(V_{REF} 2^{RN})/1.25, where: V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected. RN = decimal equivalent of RN2, RN1, RN0. For example, if V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0, respectively, then the ADC range = ±1.28 V. In unipolar mode, the effective range is 0 V to 1.28 V in this example.
[6] 1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0/XREF1 or AXREF bits in ADC0CON2 and ADC1CON, respectively. (AXREF is available only on the ADuC845.)
[7] In bipolar mode, the auxiliary ADC can be driven only to a minimum of AGND – 30 mV as indicated by the auxiliary ADC absolute AIN voltage limits. The bipolar range is still –V_{REF} to +V_{REF}.
[8] DAC linearity and ac specifications are calculated using a reduced code range of 48 to 4095, 0 V to V_{REF}, reduced code range of 100 to 3950, 0 V to V_{DD}.
[9] Endurance is qualified to 100 kcycle per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 kcycles.
[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.
[11] Power supply current consumption is measured in normal mode following the power-on sequence, and in power-down modes under the following conditions: Normal mode: reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, core executing internal software loop. Power-down mode: reset = 0.4 V, all P0 pins and P1.2 to P1.7 pins = 0.4 V. All other digital I/O pins are open circuit, core Clk changed via CD bits in PLLCON, PCON.1 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[12] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

General Notes about Specifications

- DAC gain error is a measure of the span error of the DAC.
- The ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) have been qualified and tested with the base of the LFCSP package floating. The base of the LFCSP package should be soldered to the board, but left floating electrically, to ensure good mechanical stability.
- Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
9	9	P1.4/AIN5	I	On power-on default, P1.4/AIN5 is configured as the AIN5 analog input. AIN5 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN6. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
10	10	P1.5/AIN6	I	On power-on default, P1.5/AIN6 is configured as the AIN6 analog input. AIN6 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN5. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
11	11	P1.6/AIN7/IEXC1	I/O	On power-on default, P1.6/AIN7 is configured as the AIN7 analog input. AIN7 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN8. One or both current sources can also be configured at this pin. P1.6 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
12	12	P1.7/AIN8/IEXC2	I/O	On power-on default, P1.7/AIN8 is configured as the AIN8 analog input. AIN8 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN7. One or both current sources can also be configured at this pin. P1.7 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
13	13	AINCOM/DAC	I/O	All analog inputs can be referred to this pin, provided that a relevant pseudo differential input mode is selected. This pin also functions as an alternative pin out for the DAC.
14	14	DAC	O	The voltage output from the DAC, if enabled, appears at this pin.
Not applicable	15	AIN9	I	AIN9 can be used as a pseudo differential analog input when used with AINCOM or as the positive input of a fully differential pair when used with AIN10 (LFCSP version only).
Not applicable	16	AIN10	I	AIN10 can be used as a pseudo differential analog input when used with AINCOM or as the negative input of a fully differential pair when used with AIN9 (LFCSP version only).
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. This pin has an internal weak pull-down and a Schmitt trigger input stage.
16 to 19, 22 to 25	18 to 21, 24 to 27	P3.0 to P3.7	I/O	P3.0 to P3.7 are bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active for one core clock period of the instruction cycle. Port 3 pins also have the various secondary functions described in this table.
16	18	P3.0/RxD		Receiver Data for UART Serial Port.
17	19	P3.1/TxD		Transmitter Data for UART Serial Port.
18	20	P3.2/$\overline{\text{INT0}}$		External Interrupt 0. This pin can also be used as a gate control input to Timer 0.
19	21	P3.3/$\overline{\text{INT1}}$		External Interrupt 1. This pin can also be used as a gate control input to Timer 1.
22	24	P3.4/T0		Timer/Counter 0 External Input.
23	25	P3.5/T1		Timer/Counter 1 External Input.
24	26	P3.6/$\overline{\text{WR}}$		External Data Memory Write Strobe. This pin latches the data byte from Port 0 into an external data memory.
25	27	P3.7/$\overline{\text{RD}}$		External Data Memory Read Strobe. This pin enables the data from an external data memory to Port 0.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
20, 34, 48	22, 36, 51	DV_{DD}	S	Digital Supply Voltage.
21, 35, 47	23, 37, 38, 50	DGND	S	Digital Ground.
26	28	SCLK (I^2C)	I/O	Serial Interface Clock for the I^2C Interface. As an input, this pin is a Schmitt-triggered input. A weak internal pull-up is present on this pin unless it is outputting logic low. This pin can also be controlled in software as a digital output pin.
27	29	SDATA	I/O	Serial Data Pin for the I^2C Interface. As an input, this pin has a weak internal pull-up present unless it is outputting logic low.
28 to 31, 36 to 39	30 to 33, 39 to 42	P2.0 to P2.7	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. Port 2 emits the middle and high-order address bytes during accesses to the 24-bit external data memory space. Port 2 pins also have the various secondary functions described in this table.
28	30	P2.0/SCLOCK (SPI)		Serial Interface Clock for the SPI Interface. As an input this pin is a Schmitt-triggered input. A weak internal pull-up is present on this pin unless it is outputting logic low.
29	31	P2.1/MOSI		Serial Master Output/Slave Input Data for the SPI Interface. A strong internal pull-up is present on this pin when the SPI interface outputs a logic high. A strong internal pull-down is present on this pin when the SPI interface outputs a logic low.
30	32	P2.2/MISO		Master Input/Slave Output for the SPI Interface. A weak pull-up is present on this input pin.
31	33	P2.3/$\overline{SS}$/T2		Slave Select Input for the SPI Interface. A weak pull-up is present on this pin. For both package options, this pin can also be used to provide a clock input to Timer 2. When enabled, Counter 2 is incremented in response to a negative transition on the T2 input pin.
36	39	P2.4/T2EX		Control Input to Timer 2. When enabled, a negative transition on the T2EX input pin causes a Timer 2 capture or reload event.
37	40	P2.5/PWM0		If the PWM is enabled, the PWM0 output appears at this pin.
38	41	P2.6/PWM1		If the PWM is enabled, the PWM1 output appears at this pin.
39	42	P2.7/PWMCLK		If the PWM is enabled, an external PWM clock can be provided at this pin.
32	34	XTAL1	I	Input to the Crystal Oscillator Inverter.
33	35	XTAL2	O	Output from the Crystal Oscillator Inverter. See the Hardware Design Considerations section for a description.
40	43	$\overline{EA}$		External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to F7FFH. No external program memory access is available on the ADuC845, ADuC847, or ADuC848. To determine the mode of code execution, the $\overline{EA}$ pin is sampled at the end of an external RESET assertion or as part of a device power cycle. $\overline{EA}$ can also be used as an external emulation I/O pin, and therefore the voltage level at this pin must not be changed during normal operation because this might cause an emulation interrupt that halts code execution.
41	44	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This function is not used on the ADuC845, ADuC847, or ADuC848. This pin remains high during internal program execution. $\overline{PSEN}$ can also be used to enable serial download mode when pulled low through a resistor at the end of an external RESET assertion or as part of a device power cycle.
42	45	ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit data address space accesses) of the address to external memory during external data memory access cycles. It can be disabled by setting the PCON.4 bit in the PCON SFR.

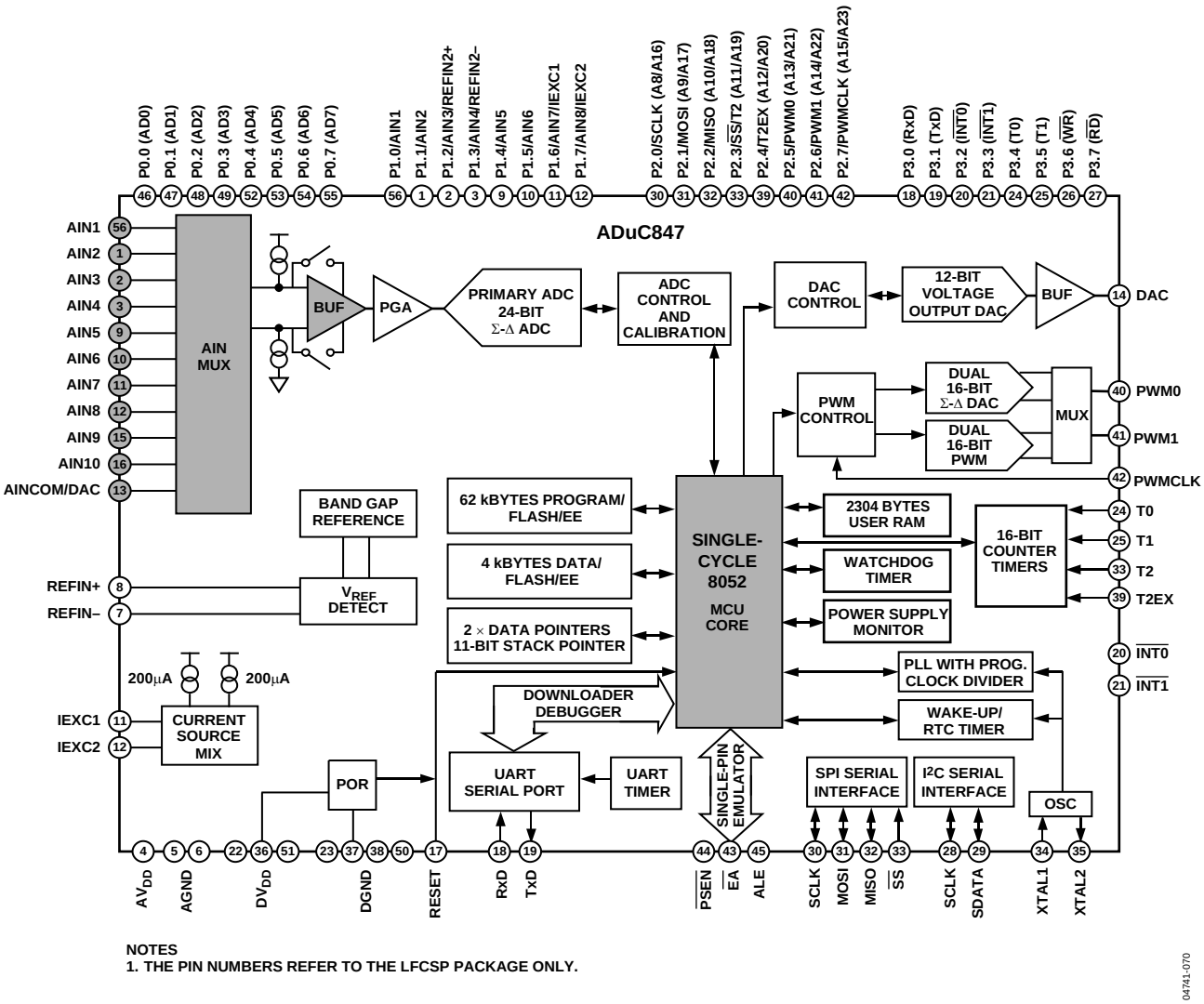


Figure 5. Detailed Block Diagram of the ADuC847

Mnemonic	Description	Bytes	Cycles[1]
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator ! = 0	2	3
DJNZ Rn,rel	Decrement register, JNZ relative	2	3
LJMP	Long jump unconditional	3	4
LCALL[3] addr16	Long jump to subroutine	3	4
JB bit,rel	Jump on direct bit = 1	3	4
JNB bit,rel	Jump on direct bit = 0	3	4
JBC bit,rel	Jump on direct bit = 1 and clear	3	4
CJNE A,dir,rel	Compare A, direct JNE relative	3	4
CJNE A,#data,rel	Compare A, immediate JNE relative	3	4
CJNE Rn,#data,rel	Compare register, immediate JNE relative	3	4
CJNE @Ri,#data,rel	Compare indirect, immediate JNE relative	3	4
DJNZ dir,rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

[1] One cycle is one clock.
[2] MOVX instructions are four cycles when they have 0 wait state. Cycles of MOVX instructions are 4 + *n* cycles when they have *n* wait states as programmed via EWAIT.
[3] LCALL instructions are three cycles when the LCALL instruction comes from an interrupt.

MEMORY ORGANIZATION

The ADuC845, ADuC847, and ADuC848 contain four memory blocks:

- 62 kbytes/32 kbytes/8 kbytes of on-chip Flash/EE program memory
- 4 kbytes of on-chip Flash/EE data memory
- 256 bytes of general-purpose RAM
- 2 kbytes of internal XRAM

Flash/EE Program Memory

The devices provide up to 62 kbytes of Flash/EE program memory to run user code. All further references to Flash/EE program memory assume the 62-kbyte option.

When $\overline{EA}$ is pulled high externally during a power cycle or a hardware reset, the devices default to code execution from their internal 62 kbytes of Flash/EE program memory. The devices do not support the rollover from internal code space to external code space. No external code space is available on the devices. Permanently embedded firmware allows code to be serially downloaded to the 62 kbytes of internal code space via the UART serial port while the device is in-circuit. No external hardware is required.

During run time, 56 kbytes of the 62-kbyte program memory can be reprogrammed. This means that the code space can be upgraded in the field by using a user-defined protocol running on the devices, or it can be used as a data memory. For details, see the Nonvolatile Flash/EE Memory Overview section.

Flash/EE Data Memory

The user has 4 kbytes of Flash/EE data memory available that can be accessed indirectly by using a group of registers mapped into the special function register (SFR) space. For details, see the Nonvolatile Flash/EE Memory Overview section.

General-Purpose RAM

The general-purpose RAM is divided into two separate memories, the upper and the lower 128 bytes of RAM. The lower 128 bytes of RAM can be accessed through direct or indirect addressing. The upper 128 bytes of RAM can be accessed only through indirect addressing because it shares the same address space as the SFR space, which must be accessed through direct addressing.

The lower 128 bytes of internal data memory are mapped as shown in Figure 8. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 to R7. The next 16 bytes (128 bits), locations 20H to 2FH above the register banks, form a block of directly addressable bit locations at Bit Addresses 00H to 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 2048 bytes.

Reset initializes the stack pointer to location 07H. Any call or push pre-increments the SP before loading the stack. Therefore, loading the stack starts from location 08H, which is also the first register (R0) of Register Bank 1. Thus, if one is going to use more than one register bank, the stack pointer should be initialized to an area of RAM not used for data storage.

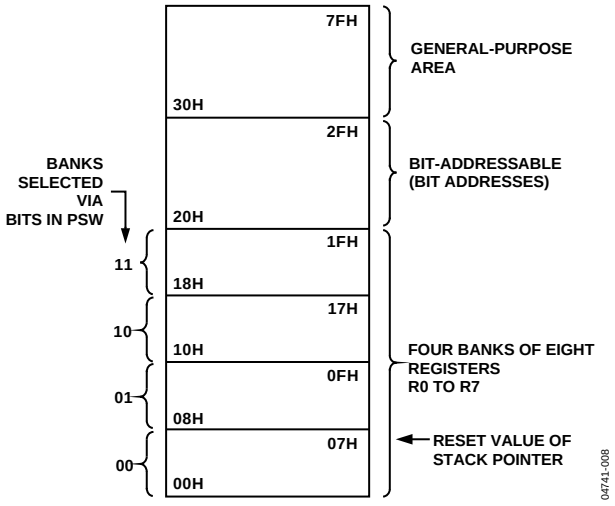


Figure 8. Lower 128 Bytes of Internal Data Memory

Internal XRAM

The ADuC845, ADuC847, and ADuC848 contain 2 kbytes of on-chip extended data memory. This memory, although on-chip, is accessed via the MOVX instruction. The 2 kbytes of internal XRAM are mapped into the bottom 2 kbytes of the external address space if the CFG84x.0 (Table 7) bit is set; otherwise, access to the external data memory occurs just like a standard 8051.

Even with the CFG84x.0 bit set, access to the external (off chip), XRAM occurs once the 24-bit DPTR is greater than 0007FFH.

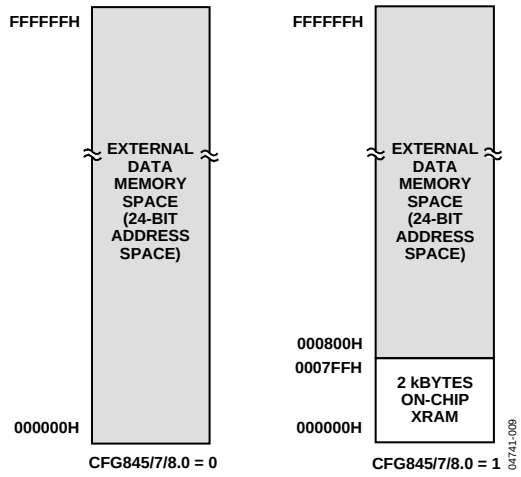


Figure 9. Internal and External XRAM

When enabled and when accessing the internal XRAM, the P0 and P2 port pin operations, as well as the $\overline{RD}$ and $\overline{WR}$ strobes, do not operate as a standard 8051 MOVX instruction. This allows the user to use these port pins as standard I/O. The internal XRAM can be configured as part of the extended 11-bit stack pointer. By default, the stack operates exactly like an 8052 in that it rolls over from FFH to 00H in the general-purpose RAM. On the ADuC845, ADuC847, and ADuC848, however, it is possible (by setting CFG845.7/ADuC847.7/ADuC848.7) to enable the 11-bit extended stack pointer. In this case, the stack rolls over from FFH in RAM to 0100H in XRAM.

The 11-bit stack pointer is visible in the SPH and SP SFRs. The SP SFR is located at 81H as with a standard 8052. The SPH SFR is located at B7H. The 3 LSBs of the SPH SFR contain the 3 extra bits necessary to extend the 8-bit stack pointer in the SP SFR into an 11-bit stack pointer.

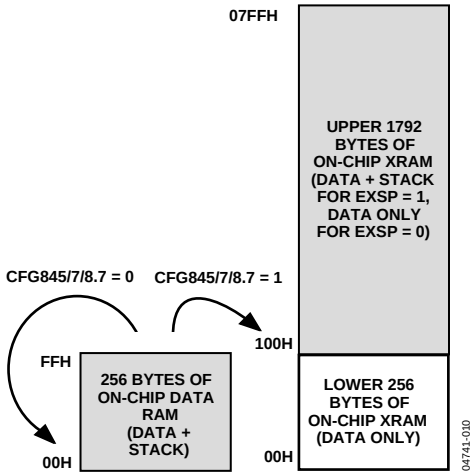


Figure 10. Extended Stack Pointer Operation

External Data Memory (External XRAM)

There is no support for external program memory access to the devices. However, just like a standard 8051-compatible core, the ADuC845/ADuC847/ADuC848 can access external data memory using a MOVX instruction. The MOVX instruction automatically outputs the various control strobes required to access the data memory. The devices, however, can access up to 16 Mbytes of external data memory. This is an enhancement of the 64 kbytes of external data memory space available on a standard 8051-compatible core. See the Hardware Design Considerations section for details.

When accessing external RAM, the EWAIT register might need to be programmed to give extra machine cycles to the MOVX operation. This is to account for differing external RAM access speeds.

EWAIT SFR

SFR Address:	9FH
Power-On Default:	00H
Bit Addressable:	No

This special function register (SFR), when programmed, dictates the number of wait states for the MOVX instruction. The value can vary between 0H and 7H. The MOVX instruction increases by one machine cycle (4 + *n*, where *n* = EWAIT number in decimal) for every increase in the EWAIT value.

that the internal calibration procedure for full-scale calibration automatically selects the reference in voltage at PGA = 1.

Therefore, the full-scale endpoint calibration automatically subtracts the offset calibration error, it is advisable to perform an offset calibration at the same gain range as that used for full-scale calibration. There is no penalty to the full-scale calibration in redoing the zero-scale calibration at the required PGA range because the full-scale calibration has very good matching at all the PGA ranges.

This procedure also applies when chop is disabled.

Note that for internal calibration to be effective, the AIN− pin should be held at a steady voltage, within the allowable common-mode range to keep it from floating during calibration.

System Calibration Example

With chop enabled, a system zero-scale or offset calibration should never be required. However, if a full-scale or gain calibration is required for any reason, use the following typical procedure for doing so.

1. Apply a differential voltage of 0 V to the selected analog inputs (AIN+ to AIN−) that are held at a common-mode voltage.

   Perform a system zero-scale or offset calibration by setting the MD2...0 bits in the ADCMODE register to 110B.

2. Apply a full-scale differential voltage across the ADC inputs again at the same common-mode voltage.

   Perform a system full-scale or gain calibration by setting the MD2...0 bits in the ADCMODE register to 111B.

Perform a system calibration at the required PGA range to be used since the ADC scales to the differential voltages that are applied to the ADC during the calibration routines.

In bipolar mode, the zero-scale calibration determines the mid-scale point of the ADC (800000H) or 0 V.

PROGRAMMABLE GAIN AMPLIFIER

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different ranges, which are programmed via the range bits (RN0 to RN2) in the ADC0CON1 register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V and 0 V to 2.56 V, while in bipolar mode the ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±64 0 mV, ±1.28 V, and ±2.56 V. These ranges should appear on the input to the on-chip PGA. The ADC range-matching specification of 2 µV (typical with chop enabled) means that calibration need only be carried out on a single range and need not be repeated when the ADC range is changed. This is a significant advantage compared to similar mixed-signal solutions available on the market. The auxiliary (ADuC845 only) ADC does not incorporate a PGA, and the gain is fixed at 0 V to 2.50 V in unipolar mode, and ±2.50 V in bipolar mode.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog inputs of the ADuC845/ADuC847/ADuC848 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the device can handle negative voltages with respect to system AGND, but rather with respect to the negative reference input. Unipolar and bipolar signals on the AIN(+) input on the ADC are referenced to the voltage on the respective AIN(−) input. AIN(+) and AIN(−) refer to the signals seen by the ADC.

For example, if AIN(−) is biased to 2.5 V (tied to the external reference voltage) and the ADC is configured for a unipolar analog input range of 0 mV to >20 mV, the input voltage range on AIN(+) is 2.5 V to 2.52 V. On the other hand, if AIN(−) is biased to 2.5 V (again the external reference voltage) and the ADC is configured for a bipolar analog input range of ±1.28 V, the analog input range on the AIN(+) is 1.22 V to 3.78 V, that is, 2.5 V ± 1.28 V.

The modes of operation for the ADC are fully differential mode or pseudo differential mode. In fully differential mode, AIN1 to AIN2 are one differential pair, and AIN3 to AIN4 are another pair (AIN5 to AIN6, AIN7 to AIN8, and AIN9 to AIN10 are the others). In differential mode, all AIN(−) pin names imply the negative analog input of the selected differential pair, that is, AIN2, AIN4, AIN6, AIN8, AIN10. The term AIN(+) implies the positive input of the selected differential pair, that is, AIN1, AIN3, AIN5, AIN7, AIN9. In pseudo differential mode, each analog input is paired with the AINCOM pin, which can be biased up or tied to AGND. In this mode, the AIN(−) implies AINCOM, and AIN(+) implies any one of the ten analog input channels.

The configuration of the inputs (unipolar vs. bipolar) is shown in Figure 17.

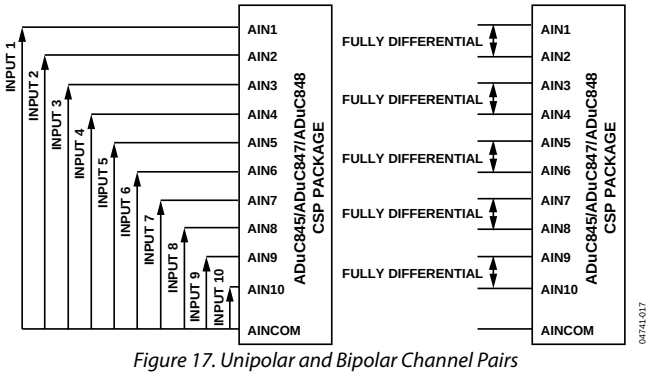


Figure 17. Unipolar and Bipolar Channel Pairs

ADC0CON1 (PRIMARY ADC CONTROL REGISTER)

ADC0CON1 is used to configure the primary ADC for buffer, unipolar, or bipolar coding, and ADC range configuration.

SFR Address: D2H
Power-On Default: 07H
Bit Addressable: No

Table 25. ADC0CON1 SFR Bit Designations

Bit No.	Name	Description			
7, 6	BUF1, BUF0	Buffer Configuration Bits.			
		BUF1	BUF0		Buffer Configuration
		0	0		ADC0+ and ADC0– are buffered
		0	1		Reserved
		1	0		Buffer Bypass
		1	1		Reserved
5	UNI	Primary ADC Unipolar Bit.			
		Set by the user to enable unipolar coding; zero differential input results in 000000H output.			
		Cleared by the user to enable bipolar coding; zero differential input results in 800000H output.			
4	–––	Not Implemented. Write Don't Care.			
3	–––	Not Implemented. Write Don't Care.			
2, 1, 0	RN2, RN1, RN0	Primary ADC Range Bits. Written by the user to select the primary ADC input range as follows:			
		RN2	RN1	RN0	Selected primary ADC input range (V_{REF} = 2.5 V)
		0	0	0	±20 mV (0 mV to 20 mV in unipolar mode)
		0	0	1	±40 mV (0 mV to 40 mV in unipolar mode)
		0	1	0	±80 mV (0 mV to 80 mV in unipolar mode)
		0	1	1	±160 mV (0 mV to 160 mV in unipolar mode)
		1	0	0	±320 mV (0 mV to 320 mV in unipolar mode)
		1	0	1	±640 mV (0 mV to 640 mV in unipolar mode)
		1	1	0	±1.28 V (0 V to 1.28 V in unipolar mode)
		1	1	1	±2.56 V (0 V to 2.56 V in unipolar mode)

DAC CIRCUIT INFORMATION

The ADuC845/ADuC847/ADuC848 incorporate a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF, and has two selectable ranges, 0 V to V_{REF} and 0 V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register, DACCON, and two data registers, DACH/L. The DAC output can be programmed to appear at Pin 14 (DAC) or Pin 13 (AINCOM).

In 12-bit mode, the DAC voltage output is updated as soon as the DACL data SFR is written; therefore, the DAC data registers should be updated as DACH first, followed by DACL. The 12-bit DAC data should be written into DACH/L right-justified such that DACL contains the lower 8 bits, and the lower nibble of DACH contains the upper 4 bits.

DACCON Control Register

SFR Address: FDH
Power-On Default: 00H
Bit Addressable: No

Table 33. DACCON—DAC Configuration Commands

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	–––	Not Implemented. Write Don't Care.
5	–––	Not Implemented. Write Don't Care.
4	DACPIN	DAC Output Pin Select. Set to 1 by the user to direct the DAC output to Pin 13 (AINCOM). Cleared to 0 by the user to direct the DAC output to Pin 14 (DAC).
3	DAC8	DAC 8-Bit Mode Bit. Set to 1 by the user to enable 8-bit DAC operation. In this mode, the 8 bits in DACL SFR are routed to the 8 MSBs of the DAC, and the 4 LSBs of the DAC are set to 0. Cleared to 0 by the user to enable 12-bit DAC operation. In this mode, the 8 LSBs of the result are routed to DACL, and the upper 4 MSB bits are routed to the lower 4 bits of DACH.
2	DACRN	DAC Output Range Bit. Set to 1 by the user to configure the DAC range of 0 V to AV_{DD}. Cleared to 0 by the user to configure the DAC range of 0 V to 2.5 V (V_{REF}).
1	DACCLR	DAC Clear Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to reset the DAC data registers DACL/H to 0.
0	DACEN	DAC Enable Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to power down the DAC.

DACH/DACL Data Registers

These DAC data registers are written to by the user to update the DAC output.

SFR Address: DACL (DAC data low byte)—FBH
DACH (DAC data high byte)—FCH
Power-On Default: 00H (both registers)
Bit Addressable: No (both registers)

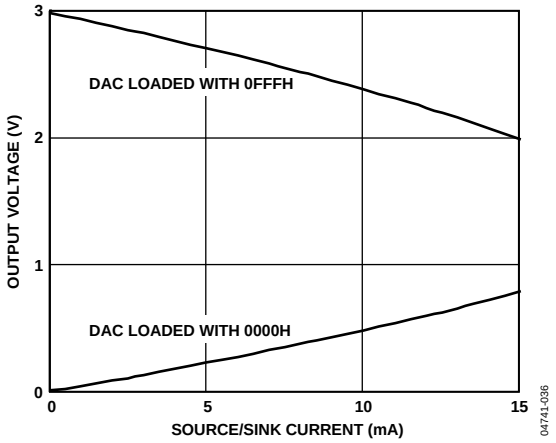


Figure 36. Source and Sink Current Capability with V_{REF} = AV_{DD} = 3 V

For larger loads, the current drive capability may not be sufficient. To increase the source and sink current capability of the DAC, an external buffer should be added as shown in Figure 37.

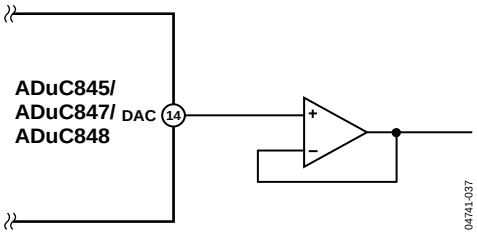


Figure 37. Buffering the DAC Output

The internal DAC output buffer also features a high impedance disable function. In the chip's default power-on state, the DAC is disabled and its output is in a high impedance state (or three-state) where it remains inactive until enabled in software. This means that if a zero output is desired during power-on or power-down transient conditions, a pull-down resistor must be added to each DAC output. Assuming that this resistor is in place, the DAC output remains at ground potential whenever the DAC is disabled.

PULSE-WIDTH MODULATOR (PWM)

The ADuC845/ADuC847/ADuC848 has a highly flexible PWM offering programmable resolution and an input clock. The PWM can be configured in six different modes of operation. Two of these modes allow the PWM to be configured as a Σ-Δ DAC with up to 16 bits of resolution. A block diagram of the PWM is shown in Figure 38.

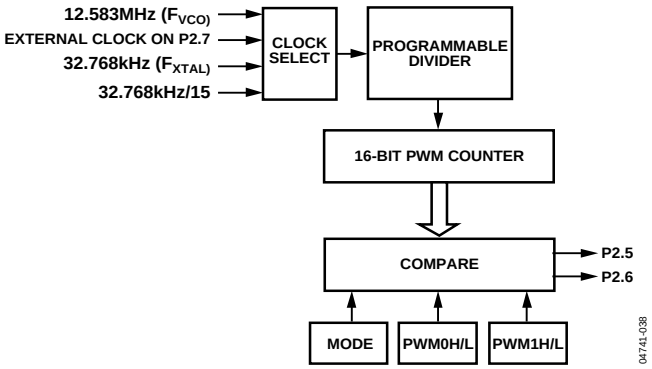


Figure 38. PWM Block Diagram

The PWM uses control SFR, PWMCON, and four data SFRs: PWM0H, PWM0L, PWM1H, and PWM1L.

PWMCON (as described in Table 34) controls the different modes of operation of the PWM as well as the PWM clock frequency. PWM0H/L and PWM1H/L are the data registers that determine the duty cycles of the PWM outputs at P2.5 and P2.6.

To use the PWM user software, first write to PWMCON to select the PWM mode of operation and the PWM input clock. Writing to PWMCON also resets the PWM counter. In any of the 16-bit modes of operation (Modes 1, 3, 4, 6), user software should write to the PWM0L or PWM1L SFRs first. This value is written to a hidden SFR. Writing to the PWM0H or PWM1H SFRs updates both the PWMxH and the PWMxL SFRs but does not change the outputs until the end of the PWM cycle in progress. The values written to these 16-bit registers are then used in the next PWM cycle.

Mode 5 (Dual 8-Bit PWM)

In Mode 5, the duty cycle and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

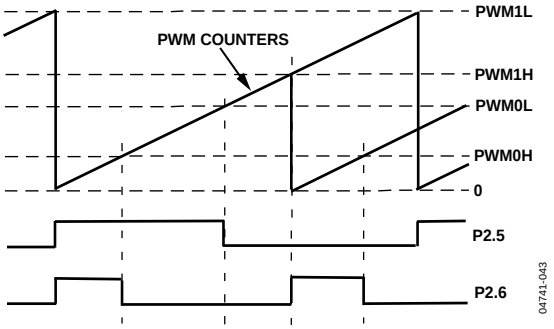


Figure 43. PWM Mode 5

Mode 6 (Dual RZ 16-Bit Σ-Δ DAC)

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4; however, the key difference is that Mode 6 provides return to zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. RZ mode ensures that any difference in the rise and fall times does not affect the Σ-Δ DAC INL. However, RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V– to AV_{DD} down to 0 V to $AV_{DD}/2$. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three full clocks (3 × 80 ns), high for one-half a clock (40 ns), and then low again for one-half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

The output resolution is set by the PWM1L and PWM1H SFRs for the P2.5 and P2.6 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P2.5 and P2.6, respectively. Both PWMs have the same clock source and clock divider.

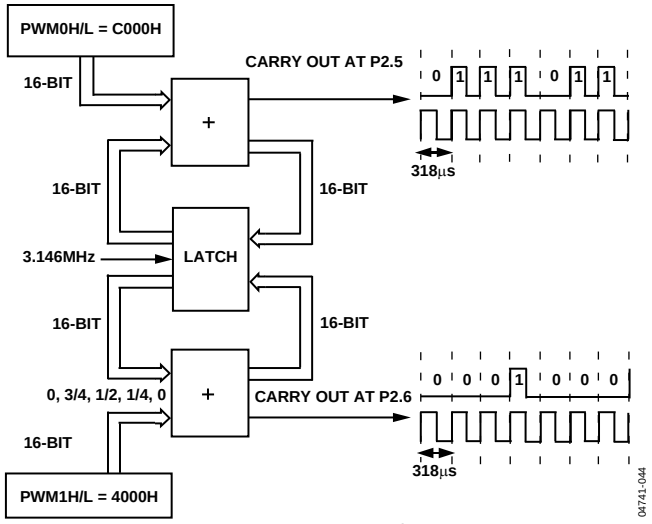


Figure 44. PWM Mode 6

Mode 7

In Mode 7, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal.

I2CADD—I²C Address Register 1

Function:	Holds one of the I²C peripheral addresses for the device. It may be overwritten by user code. The uC001 Application Note describes the format of the I²C standard 7-bit address.
SFR Address:	9BH
Power-On Default:	55H
Bit Addressable:	No

I2CADD1—I²C Address Register 2

Function:	Same as the I2CADD.
SFR Address:	F2H
Power-On Default:	7FH
Bit Addressable:	No

I2CDAT—I²C Data Register

Function:	The I2CDAT SFR is written to by user code to transmit data, or read by user code to read data just received by the I²C interface. Accessing I2CDAT automatically clears any pending I²C interrupt and the I2CI bit in the I2CCON SFR. User code should access I2CDAT only once per interrupt cycle.
SFR Address:	9AH
Power-On Default:	00H
Bit Addressable:	No

The main features of the MicroConverter I²C interface are

- Only two bus lines are required: a serial data line (SDATA) and a serial clock line (SCLOCK).
- An I²C master can communicate with multiple slave devices. Because each slave device has a unique 7-bit address, single master/slave relationships can exist at all times even in a multislave environment.
- The ability to respond to two separate addresses when operating in slave mode.
- On-chip filtering rejects <50 ns spikes on the SDATA and the SCLOCK lines to preserve data integrity.

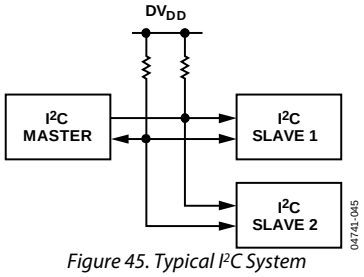


Figure 45. Typical I²C System

Software Master Mode

The ADuC845/ADuC847/ADuC848 can be used as an I²C master device by configuring the I²C peripheral in master mode and writing software to output the data bit-by-bit. This is referred to as a software master. Master mode is enabled by setting the I2CM bit in the I2CCON register.

To transmit data on the SDATA line, MDE must be set to enable the output driver on the SDATA pin. If MDE is set, the SDATA pin is pulled high or low depending on whether the MDO bit is set or cleared. MCO controls the SCLOCK pin and is always configured as an output in master mode. In master mode, the SCLOCK pin is pulled high or low depending on the whether MCO is set or cleared.

To receive data, MDE must be cleared to disable the output driver on SDATA. Software must provide the clocks by toggling the MCO bit and reading the SDATA pin via the MDI bit. If MDE is cleared, MDI can be used to read the SDATA pin. The value of the SDATA pin is latched into MDI on a rising edge of SCLOCK. MDI is set if the SDATA pin is high on the last rising edge of SCLOCK. MDI is cleared if the SDATA pin is low on the last rising edge of SCLOCK.

Software must control MDO, MCO, and MDE appropriately to generate the start condition, slave address, acknowledge bits, data bytes, and stop conditions. These functions are described in the uC001 Application Note.

SPICON—SPI Control Register

SFR Address: F8H
Power-On Default: 05H
Bit Addressable: Yes

Table 41. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user code to enable SPI functionality. Cleared by user code to enable standard Port 2 functionality.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user code to enable master mode operation (SCLOCK is an output). Cleared by user code to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Bit. Set by user code to enable SCLOCK idle high. Cleared by user code to enable SCLOCK idle low.
2	CPHA[1]	Clock Phase Select Bit. Set by user code if the leading SCLOCK edge is to transmit data. Cleared by user code if the trailing SCLOCK edge is to transmit data.
1, 0	SPR1, SPR0	SPI Bit-Rate Bits. SPR1 SPR0 Selected Bit Rate 0 0 $f_{core}/2$ 0 1 $f_{core}/4$ 1 0 $f_{core}/8$ 1 1 $f_{core}/16$

[1] The CPOL and CPHA bits should both contain the same values for master and slave devices.

Note that both SPI and I²C use the same ISR (Vector Address 3BH); therefore, when using SPI and I²C simultaneously, it is necessary to check the interfaces following an interrupt to determine which one caused the interrupt.

SPIDAT: SPI Data Register

SFR Address: 7FH
Power-On Default: 00H
Bit Addressable: No

Timer/Counter 2 Operating Modes

The following sections describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table 53.

Table 53. T2CON Operating Modes

RCLK (or) TCLK	CAP2	TR2	Mode
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	Off

16-Bit Autoreload Mode

Autoreload mode has two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. Autoreload mode is shown in Figure 56.

16-Bit Capture Mode

Capture mode has two options that are selected by Bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter that, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into Registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes Bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is shown in Figure 57. The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore, Timer 2 interrupts do not occur, so they do not have to be disabled. In this mode, the EXF2 flag can, however, still cause interrupts, which can be used as a third external interrupt. Baud rate generation is described as part of the UART serial port operation in the following section.

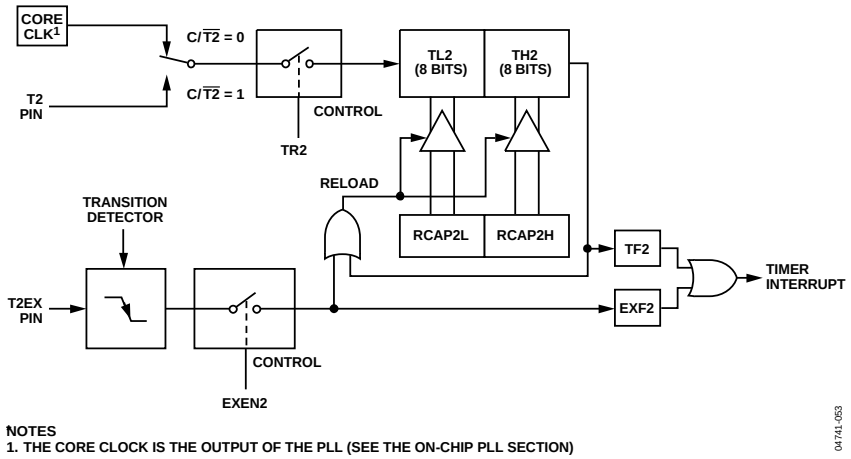


Figure 56. Timer/Counter 2, 16-Bit Autoreload Mode

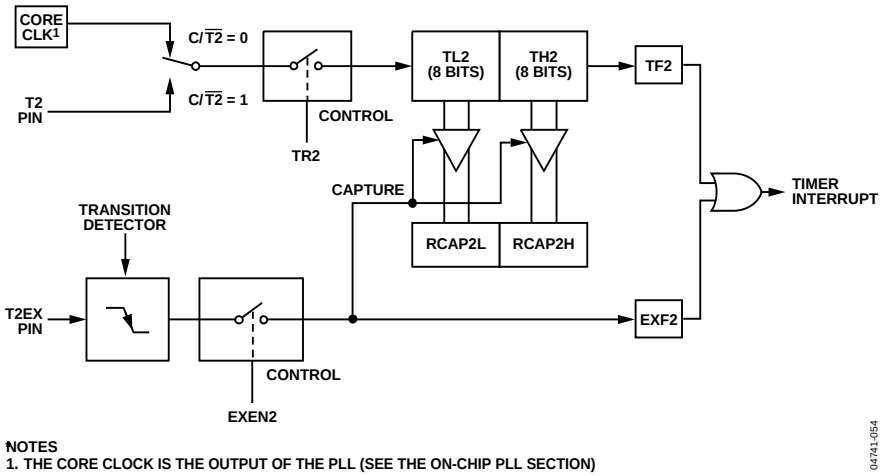


Figure 57. Timer/Counter 2, 16-Bit Capture Mode

INTERRUPT SYSTEM

The ADuC845/ADuC847/ADuC848 provide nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE Interrupt Enable Register
IP Interrupt Priority Register
IEIP2 Secondary Interrupt Enable Register

IE—Interrupt Enable Register

SFR Address: A8H
Power-On Default: 00H
Bit Addressable: Yes

Table 58. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	Set by the user to enable External Interrupt 1 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 1 ($\overline{INT0}$).
1	ET0	Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	Set by the user to enable External Interrupt 0 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 0 ($\overline{INT0}$).

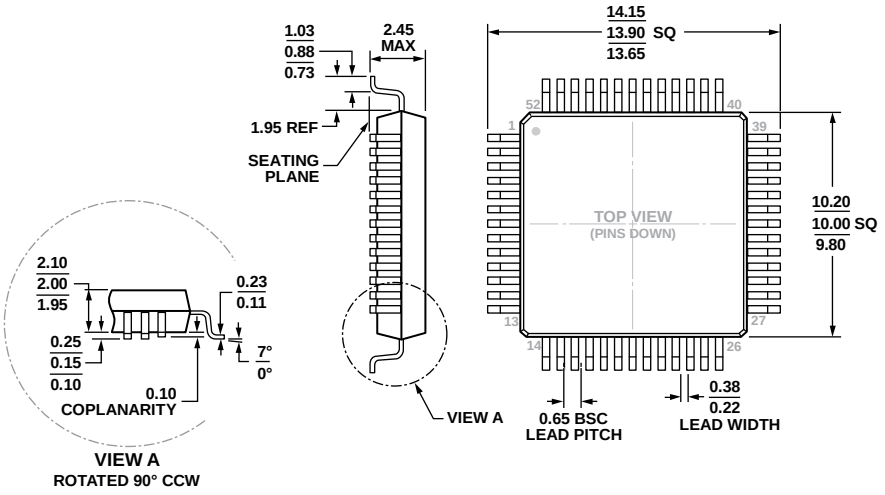
IP—Interrupt Priority Register

SFR Address: B8H
Power-On Default: 00H
Bit Addressable: Yes

Table 59. IP SFR Bit Designations

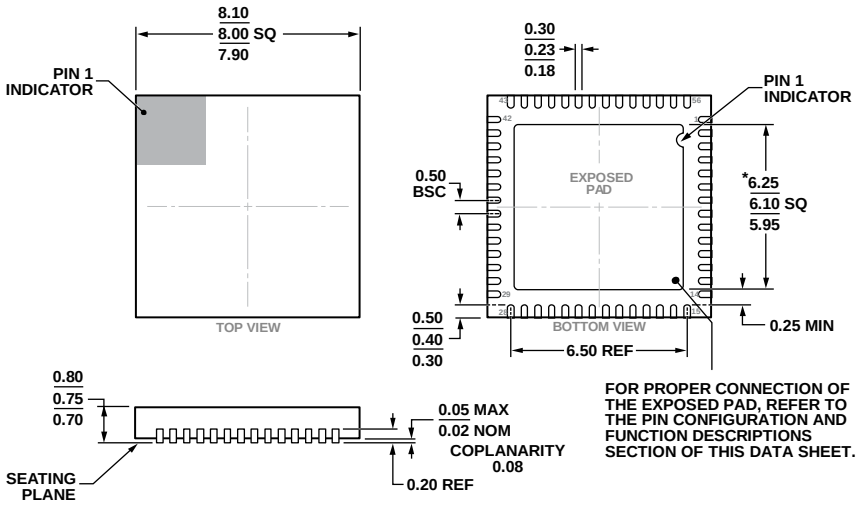
Bit No.	Name	Description
7	-----	Not Implemented. Write Don't Care.
6	PADC	ADC Interrupt Priority (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	PX1	$\overline{INT0}$ (External Interrupt 1) priority (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	PX0	$\overline{INT0}$ (External Interrupt 0) Priority (1 = High; 0 = Low).

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-112-AC-2

Figure 81. 52-Lead Metric Quad Flat Package [MQFP]
(S-52-2)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-WLLD-2
WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 82. 56-Lead Lead Frame Chip Scale Package [LFCSP]
8 mm × 8 mm Body and 0.75 mm Package Height
(CP-56-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADuC845BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC845BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC845BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC845BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC845BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC845BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC847BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC847BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC847BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC847BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC847BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC847BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC847BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC847BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC847BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC847BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC848BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC848BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC848BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC848BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC848BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC848BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC848BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC848BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC848BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC848BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
EVAL-ADuC845QSZ		QuickStart Development System	
EVAL-ADuC845QSPZ		QuickStart-PLUS Development System	
EVAL-ADuC847QSZ		QuickStart Development System	
EVAL-ADUC-CABLE1Z		ADuC Serial Downloader Cable for UART	

[1] The -3 and -5 in the Model column indicate the DV_{DD} operating voltage.
[2] Z = RoHS Compliant Part.
[3] The QuickStart Plus system can only be ordered directly from Accutron. It can be purchased from the website http://www.accutron.com.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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