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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc845bsz62-3

REVISION HISTORY

5/2016—Rev. C to Rev. D

Changed uC004 to AN-1074 ..... Throughout
Updated Outline Dimensions 108
Changes to Ordering Guide 109

12/2012—Rev. B to Rev. C

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Changes to Mode 4 (Dual NRZ 16-Bit Σ-Δ DAC) Section 58
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2/2005—Rev. A to Rev. B

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4/2004—Revision 0: Initial Version

SPECIFICATIONS[1]

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V, REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz crystal; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Input buffer on for primary ADC, unless otherwise noted. Core speed = 1.57 MHz (default CD = 3), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY ADC					
Conversion Rate	5.4		105	Hz	Chop on (ADCMODE.3 = 0)
	16.06		1365	Hz	Chop off (ADCMODE.3 = 1)
No Missing Codes[2]	24			Bits	≤26.7 Hz update rate with chop enabled
	24			Bits	≤80.3 Hz update rate with chop disabled
Resolution (ADuC845/ADuC847)	See Table 11 and Table 15				
Resolution (ADuC848)	See Table 13 and Table 17				
Output Noise (ADuC845/ADuC847)	See Table 10 and Table 14			µV (rms)	Output noise varies with selected update rates, gain range, and chop status.
Output Noise (ADuC848)	See Table 12 and Table 16			µV (rms)	Output noise varies with selected update rates, gain range, and chop status.
Integral Nonlinearity			±15	ppm of FSR	1 LSB_{16}
Offset Error[3]		±3		µV	Chop on
					Chop off, offset error is in the order of the noise for the programmed gain and update rate following a calibration.
Offset Error Drift vs. Temperature[2]		±10		nV/°C	Chop on (ADCMODE.3 = 0)
		±200		nV/°C	Chop off (ADCMODE.3 = 1)
Full-Scale Error[4]					
ADuC845/ADuC847		±10		µV	±20 mV to ±2.56 V
ADuC848		±10		µV	±20 mV to ±640 mV
		±0.5		LSB_{16}	±1.28 V to ±2.56 V
Gain Error Drift vs. Temperature[4]		±0.5		ppm/°C	
Power Supply Rejection					
	80			dB	AIN = 1 V, ±2.56 V, chop enabled
		113		dB	AIN = 7.8 mV, ±20 mV, chop enabled
		80		dB	AIN = 1 V, ±2.56 V, chop disabled[2]
PRIMARY ADC ANALOG INPUTS					
Differential Input Voltage Ranges[5, 6]					Gain = 1 to 128
Bipolar Mode (ADC0CON1.5 = 0)		±1.024 × V_{REF}/GAIN		V	V_{REF} = REFIN(+) – REFIN(–) or REFIN2(+) – REFIN2(–) (or Int 1.25 V_{REF})
Unipolar Mode (ADC0CON1.5 = 1)		0 – 1.024 × V_{REF}/GAIN		V	V_{REF} = REFIN(+) – REFIN(–) or REFIN2(+) – REFIN2(–) (or Int 1.25 V_{REF})
ADC Range Matching		±2		µV	AIN = 18 mV, chop enabled
Common-Mode Rejection DC					Chop enabled, chop disabled
On AIN	95			dB	AIN = 7.8 mV, range = ±20 mV
		113		dB	AIN = 1 V, range = ±2.56 V
Common-Mode Rejection 50 Hz/60 Hz[2]					50 Hz/60 Hz ± 1 Hz, 16.6 Hz and 50 Hz update rate, chop enabled, REJ60 enabled
On AIN	95			dB	AIN = 7.8 mV, range = ±20 mV
	90			dB	AIN = 1 V, range = ±2.56 V

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
43 to 46, 49 to 52	46 to 49, 52 to 55	P0.0 to P0.7	I/O	These pins are part of Port 0, which is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and, in that state, can be used as high impedance inputs. An external pull-up resistor is required on P0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low-order address and data bus during accesses to external data memory. In this application, Port 0 uses strong internal pull-ups when emitting 1s.
	EP	EPAD		Exposed Pad. For the LFCSP, the exposed paddle must be left unconnected.

[1] I = input, S = supply, I/O means input/output, and O = output.

Mnemonic	Description	Bytes	Cycles[1]
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry = 1	2	3
JNC rel	Jump on carry = 0	2	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator ! = 0	2	3
DJNZ Rn,rel	Decrement register, JNZ relative	2	3
LJMP	Long jump unconditional	3	4
LCALL[3] addr16	Long jump to subroutine	3	4
JB bit,rel	Jump on direct bit = 1	3	4
JNB bit,rel	Jump on direct bit = 0	3	4
JBC bit,rel	Jump on direct bit = 1 and clear	3	4
CJNE A,dir,rel	Compare A, direct JNE relative	3	4
CJNE A,#data,rel	Compare A, immediate JNE relative	3	4
CJNE Rn,#data,rel	Compare register, immediate JNE relative	3	4
CJNE @Ri,#data,rel	Compare indirect, immediate JNE relative	3	4
DJNZ dir,rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

[1] One cycle is one clock.
[2] MOVX instructions are four cycles when they have 0 wait state. Cycles of MOVX instructions are 4 + *n* cycles when they have *n* wait states as programmed via EWAIT.
[3] LCALL instructions are three cycles when the LCALL instruction comes from an interrupt.

MEMORY ORGANIZATION

The ADuC845, ADuC847, and ADuC848 contain four memory blocks:

- 62 kbytes/32 kbytes/8 kbytes of on-chip Flash/EE program memory
- 4 kbytes of on-chip Flash/EE data memory
- 256 bytes of general-purpose RAM
- 2 kbytes of internal XRAM

Flash/EE Program Memory

The devices provide up to 62 kbytes of Flash/EE program memory to run user code. All further references to Flash/EE program memory assume the 62-kbyte option.

When $\overline{EA}$ is pulled high externally during a power cycle or a hardware reset, the devices default to code execution from their internal 62 kbytes of Flash/EE program memory. The devices do not support the rollover from internal code space to external code space. No external code space is available on the devices. Permanently embedded firmware allows code to be serially downloaded to the 62 kbytes of internal code space via the UART serial port while the device is in-circuit. No external hardware is required.

During run time, 56 kbytes of the 62-kbyte program memory can be reprogrammed. This means that the code space can be upgraded in the field by using a user-defined protocol running on the devices, or it can be used as a data memory. For details, see the Nonvolatile Flash/EE Memory Overview section.

Flash/EE Data Memory

The user has 4 kbytes of Flash/EE data memory available that can be accessed indirectly by using a group of registers mapped into the special function register (SFR) space. For details, see the Nonvolatile Flash/EE Memory Overview section.

General-Purpose RAM

The general-purpose RAM is divided into two separate memories, the upper and the lower 128 bytes of RAM. The lower 128 bytes of RAM can be accessed through direct or indirect addressing. The upper 128 bytes of RAM can be accessed only through indirect addressing because it shares the same address space as the SFR space, which must be accessed through direct addressing.

The lower 128 bytes of internal data memory are mapped as shown in Figure 8. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 to R7. The next 16 bytes (128 bits), locations 20H to 2FH above the register banks, form a block of directly addressable bit locations at Bit Addresses 00H to 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 2048 bytes.

Reset initializes the stack pointer to location 07H. Any call or push pre-increments the SP before loading the stack. Therefore, loading the stack starts from location 08H, which is also the first register (R0) of Register Bank 1. Thus, if one is going to use more than one register bank, the stack pointer should be initialized to an area of RAM not used for data storage.

ADC Noise Performance with Chop Enabled ($\overline{CHOP}$ = 0)

Table 10, Table 11, Table 12, and Table 13 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates for the ADuC845, ADuC847, and ADuC848. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are in the same range as the bipolar figures, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution.

Table 10. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	1.75	1.30	1.65	1.5	2.1	3.1	7.15	13.3
23	59.36	1.25	0.95	1.08	0.94	1.0	1.87	3.24	7.1
27	50.56	1.0	1.0	0.85	0.85	1.13	1.56	2.9	3.6
69	19.79	0.63	0.68	0.52	0.7	0.61	1.1	1.3	2.75
255	5.35	0.31	0.38	0.34	0.32	0.4	0.45	0.68	1.22

Table 11. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	12	13	14	15	15.5	16	16	16
23	59.36	12	13.5	14.5	15.5	16.5	16.5	17	16.5
27	50.56	12.5	13.5	15	16	16.5	17	17	17.5
69	19.79	13	14	15.5	16	17.5	17.5	18	18
255	5.35	14.5	15	16	17	18	18.5	19	19.5

Table 12. ADuC848 Typical Output Noise (μV) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	1.75	1.30	1.65	1.5	2.1	3.1	7.15	13.3
23	59.36	1.25	0.95	1.08	0.94	1.0	1.87	3.24	7.1
27	50.56	1.0	1.0	0.85	0.85	1.13	1.56	2.9	3.6
69	19.79	0.63	0.68	0.52	0.7	0.61	1.1	1.3	2.75
255	5.35	0.31	0.38	0.34	0.32	0.4	0.45	0.68	1.22

Table 13. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	12	13	14	15	15.5	16	16	16
23	59.36	12	13.5	14.5	15.5	16	16	17	16
27	50.56	12.5	13.5	15	16	16	16	16	16
69	19.79	13	14	15.5	16	16	16	16	16
255	5.35	14.5	15	16	16	16	16	16	16

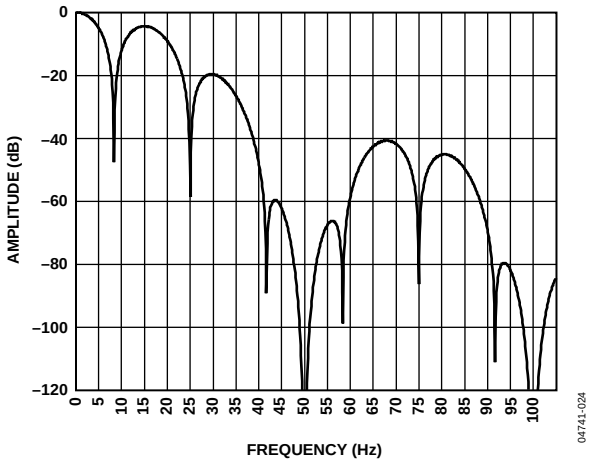

Figure 24. Chop On, Fadc = 16.6 Hz, SF = 52H

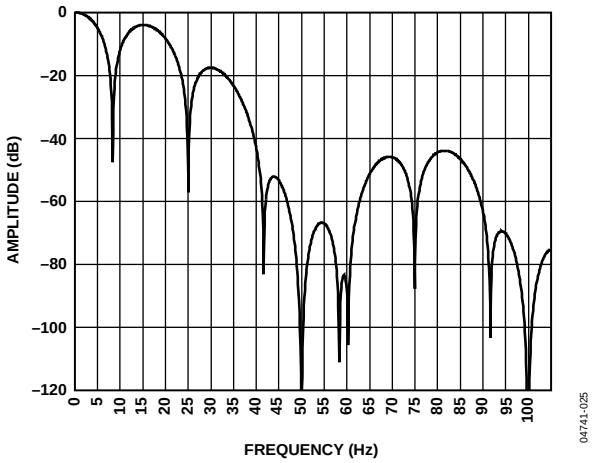

Figure 25. Chop On, Fadc = 16.6 Hz, SF = 52H, REJ60 Enabled

FUNCTIONAL DESCRIPTION

ADC SFR INTERFACE

The ADCs are controlled and configured via a number of SFRs that are mentioned here and described in more detail in the following sections.

Table 22. ADC SFR Interface

Name	Description
ADCSTAT	ADC Status Register. Holds the general status of the primary and auxiliary (ADuC845 only) ADCs.
ADCMODE	ADC Mode Register. Controls the general modes of operation for primary and auxiliary (ADuC845 only) ADCs.
ADC0CON1	Primary ADC Control Register 1. Controls the specific configuration of the primary ADC.
ADC0CON2	Primary ADC Control Register 2. Controls the specific configuration of the primary ADC.
ADC1CON	Auxiliary ADC Control Register. Controls the specific configuration of the auxiliary ADC. ADuC845 only.
SF	Sinc Filter Register. Configures the decimation factor for the Sinc^3 filter and, therefore, the primary and auxiliary (ADuC845 only) ADC update rates.
ICON	Current Source Control Register. Allows user control of the various on-chip current source options.
ADC0L/M/H	Primary ADC 24-bit (16-bit on the ADuC848) conversion result is held in these three 8-bit registers. ADC0L is not available on the ADuC848.
ADC1L/M/H	Auxiliary ADC 24-bit conversion result is held in these two 8-bit registers. ADuC845 only.
OF0L/M/H	Primary ADC 24-bit offset calibration coefficient is held in these three 8-bit registers. OF0L is not available on the ADuC848.
OF1L/H	Auxiliary ADC 16-bit offset calibration coefficient is held in these two 8-bit registers. ADuC845 only.
GN0L/M/H	Primary ADC 24-bit gain calibration coefficient is held in these three 8-bit registers. GN0L is not available on the ADuC848.
GN1L/H	Auxiliary ADC 16-bit gain calibration coefficient is held in these two 8-bit registers. ADuC845 only.

ADCMODE (ADC MODE REGISTER)

Used to control the operational mode of both ADCs.

SFR Address: D1H
Power-On Default: 08H
Bit Addressable: No

Table 24. ADCMODE SFR Bit Designations

Bit No.	Name	Description
7	---	Not Implemented. Write Don't Care.
6	REJ60	Automatic 60 Hz Notch Select Bit. Setting this bit places a notch in the frequency response at 60 Hz, allowing simultaneous 50 Hz and 60 Hz rejection at an SF word of 82 decimal. This 60 Hz notch can be set only if SF ≥68 decimal, that is, the regular filter notch must be ≤60 Hz. This second notch is placed at 60 Hz only if the device clock is at 32.768 kHz.
5	ADC0EN	Primary ADC Enable. Set by the user to enable the primary ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the primary ADC into power-down mode.
4	ADC1EN (ADuC845 only)	Auxiliary (ADuC845 only) ADC Enable. Set by the user to enable the auxiliary (ADuC845 only) ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the auxiliary (ADuC845 only) ADC in power-down mode.
3	$\overline{\text{CHOP}}$	Chop Mode Disable. Set by the user to disable chop mode on both the primary and auxiliary (ADuC845 only) ADC allowing a three times higher ADC data throughput. SF values as low as 3 are allowed with this bit set, giving up to 1.3 kHz ADC update rates. Cleared by the user to enable chop mode on both the primary and auxiliary (ADuC845 only) ADC.
2, 1, 0	MD2, MD1, MD0	Primary and Auxiliary (ADuC845 only) ADC Mode Bits. These bits select the operational mode of the enabled ADC as follows: MD2 MD1 MD0 0 0 0 ADC Power-Down Mode (Power-On Default). 0 0 1 Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided. 0 1 0 Single Conversion Mode. In single conversion mode, a single conversion is performed on the enabled ADC. Upon completion of a conversion, the ADC data registers (ADC0H/M/L and/or ADC1H/M/L (ADuC845 only)) are updated. The relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000. Note that ADC0L is not available on the ADuC848. 0 1 1 Continuous Conversion. In continuous conversion mode, the ADC data registers are regularly updated at the selected update rate (see the Sinc Filter SFR Bit Designations in Table 28). 1 0 0 Internal Zero-Scale Calibration. Internal short automatically connected to the enabled ADC input(s). 1 0 1 Internal Full-Scale Calibration. Internal or external REFIN± or REFIN2± V_{REF} (as determined by XREF bits in ADC0CON2 and/or AXREF (ADuC845 only) in ADC1CON (ADuC845 only) is automatically connected to the enabled ADC input(s) for this calibration. 1 1 0 System Zero-Scale Calibration. User should connect system zero-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers. 1 1 1 System Full-Scale Calibration. User should connect system full-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers.

USER DOWNLOAD MODE (ULOAD)

Figure 28 shows that it is possible to use the 62 kbytes of Flash/EE program memory available to the user as one single block of memory. In this mode, all the Flash/EE memory is read-only to user code.

However, most of the Flash/EE program memory can also be written to during run time simply by entering ULOAD mode. In ULOAD mode, the lower 56 kbytes of program memory can be erased and reprogrammed by the user software as shown in Figure 30. ULOAD mode can be used to upgrade the code in the field via any user-defined download protocol. By configuring the SPI port on the ADuC845/ADuC847/ADuC848 as a slave, it is possible to completely reprogram the 56 kbytes of Flash/EE program memory in under 5 s (see the AN-1074 Application Note).

Alternatively, ULOAD mode can be used to save data to the 56 kbytes of Flash/EE memory. This can be extremely useful in data logging applications where the devices can provide up to 60 kbytes of data memory on-chip (4 kbytes of dedicated Flash/EE data memory also exist).

The upper 6 kbytes of the 62 kbytes of Flash/EE program memory (8 kbytes on the 32-kbyte parts) are programmable only via serial download or parallel programming. This means that this space appears as read-only to user code; therefore, it cannot be accidentally erased or reprogrammed by erroneous code execution, making it very suitable to use the 6 kbytes as a bootloader. A bootload enable option exists in the Windows® serial downloader (WSD) to "Always RUN from E000H after Reset." If using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset.

Programming the Flash/EE program memory via ULOAD mode is described in the Flash/EE Memory Control SFR section of ECON and also in the AN-1074 Application Note.

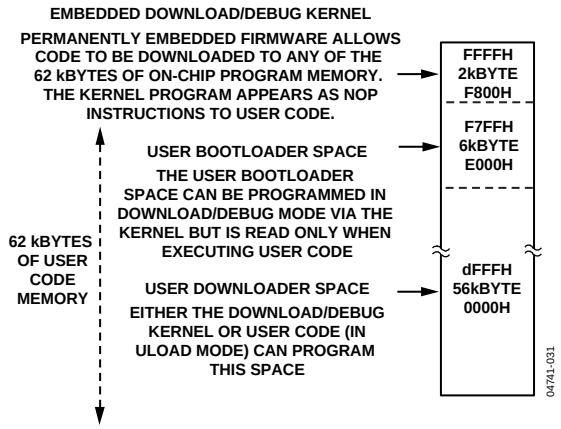

Figure 30. Flash/EE Program Memory Map in ULOAD Mode (62-kbyte Part)

The 32-kbyte memory parts have the user bootload space starting at 6000H. The memory mapping is shown in Figure 31.

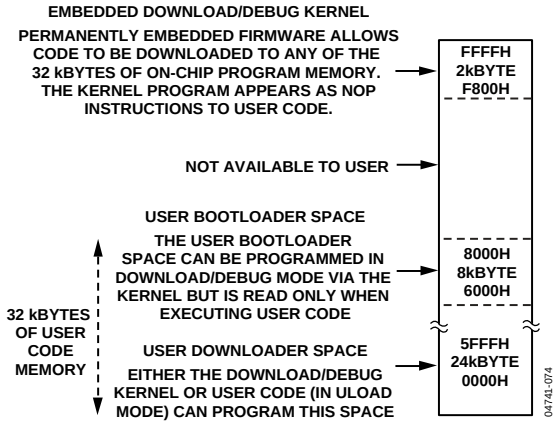

Figure 31. Flash/EE Program Memory Map in ULOAD Mode (32-kbyte Part)

ULOAD mode is not available on the 8-kbyte Flash/EE program memory parts.

Flash/EE Program Memory Security

The ADuC845/ADuC847/ADuC848 facilitate three modes of Flash/EE program memory security: the lock, secure, and serial safe modes. These modes can be independently activated, restricting access to the internal code space. They can be enabled as part of serial download protocol, as described in the AN-1074 Application Note, or via parallel programming.

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in parallel mode and reading the memory via a MOVC command from external memory are still allowed. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Secure Mode

This mode locks the code memory, disabling parallel programming of the program memory. Reading/verifying the memory in parallel mode and reading the internal memory via a MOVC command from external memory are also disabled. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the device into serial download mode, that is, RESET asserted (pulled high) and de-asserted (pulled low) with $\overline{\text{PSEN}}$ low, the device interprets the serial download reset as a normal reset only. It therefore does not enter serial download mode, but executes only a normal reset sequence. Serial safe mode can be disabled only by initiating an ERASE CODE AND DATA command in parallel programming mode.

ON-CHIP PLL (PLLCON)

The ADuC845/ADuC847/ADuC848 are intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (384) of this to provide a stable 12.582912 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving when maximum core performance is not required. The default core clock is the PLL clock divided by 8 or 1.572864 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The control register for the PLL is called PLLCON and is described as follows.

The 5 V parts can be set to a maximum core frequency of 12.58 MHz (CD2...0 = 000) while at 3 V, the maximum core clock rate is 6.29 MHz (CD2...0 = 001). The CD bits should not be set to 000b on the 3 V parts.

The 3 V parts are limited to a core clock speed of 6.29 MHz (CD = 1).

PLLCON PLL Control Register

SFR Address: D7H
Power-On Default: 53H
Bit Addressable: No

Table 39. PLLCON PLL Control Register

Bit No.	Name	Description
7	OSC_PD	Oscillator Power-Down Bit. If low, the 32 kHz crystal oscillator continues running in power-down mode. If high, the 32.768 kHz oscillator is powered down. When this bit is low, the seconds counter continues to count in power-down mode and can interrupt the CPU to exit power-down. The oscillator is always enabled in normal mode.
6	LOCK	PLL Lock Bit. This is a read-only bit. Set automatically at power-on to indicate that the PLL loop is correctly tracking the crystal clock. After power-down, this bit can be polled to wait for the PLL to lock. Cleared automatically at power-on to indicate that the PLL is not correctly tracking the crystal clock. This might be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output can be 12.58 MHz ± 20%. After the device wakes up from power-down, user code can poll this bit to wait for the PLL to lock. If LOCK = 0, the PLL is not locked.
5	–––	Not Implemented. Write Don't Care.
4	LTEA	EA Status. Read-only bit. Reading this bit returns the state of the external $\overline{EA}$ pin latched at reset or power-on.
3	FINT	Fast Interrupt Response Bit. Set by the user to enable the response to any interrupt to be executed at the fastest core clock frequency. Cleared by the user to disable the fast interrupt response feature. This function must not be used on 3 V parts.
2, 1, 0	CD2, CD1, CD0	CPU (Core Clock) Divider Bits. This number determines the frequency at which the core operates. CD2 CD1 CD0 Core Clock Frequency (MHz) 0 0 0 12.582912. Not a valid selection on 3 V parts. 0 0 1 6.291456 (Maximum core clock rate allowed on the 3 V parts) 0 1 0 3.145728 0 1 1 1.572864 (Default core frequency) 1 0 0 0.786432 1 0 1 0.393216 1 1 0 0.196608 1 1 1 0.098304 On 3 V parts (ADuC84xBCPxx-3 or ADuC84xBSxx-3), the CD settings can be only CD = 1; CD = 0 is not a valid selection. If CD = 0 is selected on a 3 V part by writing to PLLCON, the instruction is ignored, and the previous CD value is retained. The Fast Interrupt bit (FINT) must not be used on 3 V parts since it automatically sets the CD bits to 0, which is not a valid setting.

I²C SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 support a fully licensed I²C serial interface. The I²C interface is implemented as a full hardware slave and software master. SDATA (Pin 27 on the MQFP package and Pin 29 on the LFCSP package) is the data I/O pin. SCLK (Pin 26 on the MQFP package and Pin 28 on the LFCSP package) is the serial interface clock for the SPI interface. The I²C interface on the devices is fully independent of all other pin/function multiplexing. The I²C interface incorporated on the ADuC845/ADuC847/ADuC848 also includes a second address register (I2CADD1) at SFR Address F2H with a default power-on value of 7FH. The I²C interface is always available to the user and is not multiplexed with any other I/O functionality on the chip. This means that the I²C and SPI interfaces can be used at the same time.

Note that when using the I²C and SPI interfaces simultaneously, they both use the same interrupt routine (Vector Address 3BH). When an interrupt occurs from one of these, it is necessary to interrogate each interface to see which one has triggered the ISR request.

The four SFRs that are used to control the I²C interface are described next.

I2CCON—I²C Control Register

SFR Address: E8H
Power-On Default: 00H
Bit Addressable: Yes

Table 40. I2CCON SFR Bit Designations

Bit No.	Name	Description
7	MDO	I²C Software Master Data Output Bit (master mode only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SDATA pin if the data output enable bit (MDE) is set.
6	MDE	I²C Software Output Enable Bit (master mode only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable the SDATA pin as an input (Rx).
5	MCO	I²C Software Master Clock Output Bit (master mode only). This bit is used to implement the SCLK for a master I²C transmitter in software. Data written to this bit is output on the SCLK pin.
4	MDI	I²C Software Master Data Input Bit (master mode only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on an SCLK transition if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (slave mode only). Set by the user to reset the I²C interface. Cleared by the user code for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (slave mode only). Set by the MicroConverter if the I²C interface is transmitting. Cleared by the MicroConverter if the I²C interface is receiving.
0	I2CI	I²C Interrupt Bit (slave mode only). Set by the MicroConverter after a byte has been transmitted or received. Cleared by the MicroConverter when the user code reads the I2CDAT SFR. I2CI should not be cleared by user code.

USING THE SPI INTERFACE

Depending on the configuration of the bits in the SPICON SFR shown in Table 41, the SPI interface transmits or receives data in a number of possible modes. Figure 46 shows all possible ADuC845/ADuC847/ADuC848 SPI configurations and the timing relationships and synchronization among the signals involved. Also shown in this figure is the SPI interrupt bit (ISPI) and how it is triggered at the end of each byte-wide communication.

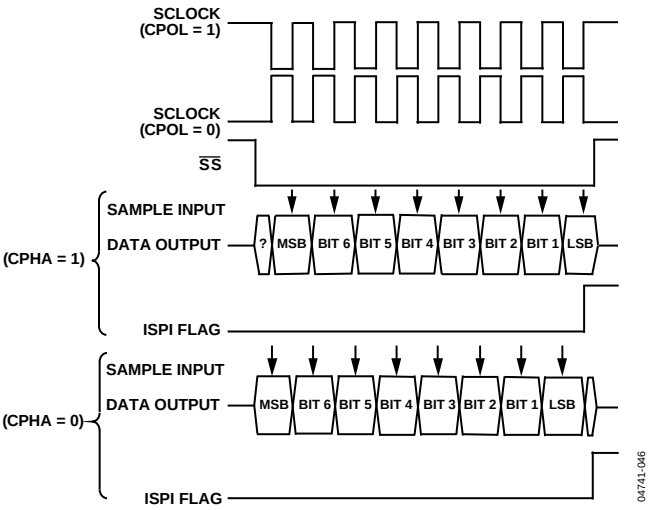

Figure 46. SPI Timing, All Modes

SPI Interface—Master Mode

In master mode, the SCLOCK pin is always an output and generates a burst of eight clocks whenever user code writes to the SPIDAT register. The SCLOCK bit rate is determined by SPR0 and SPR1 in SPICON. Also note that the $\overline{SS}$ pin is not used in master mode. If the devices need to assert the $\overline{SS}$ pin on an external slave device, use a port digital output pin.

In master mode, a byte transmission or reception is initiated by a byte write to SPIDAT. The hardware automatically generates eight clock periods via the SCLOCK pin, and the data is transmitted via MOSI. With each SCLOCK period, a data bit is also sampled via MISO. After eight clocks, the transmitted byte is completely transmitted (via MOSI), and the input byte (if required) is waiting in the input shift register (after being received via MISO). The ISPI flag is set automatically, and an interrupt occurs if enabled. The value in the input shift register is latched into SPIDAT.

SPI Interface—Slave Mode

In slave mode, the SCLOCK is an input. The $\overline{SS}$ pin must also be driven low externally during the byte communication. Transmission is also initiated by a write to SPIDAT. In slave mode, a data bit is transmitted via MISO, and a data bit is received via MOSI through each input SCLOCK period. After eight clocks, the transmitted byte is completely transmitted, and the input byte is waiting in the input shift register. The ISPI flag is set automatically, and an interrupt occurs, if enabled. The value in the shift register is latched into SPIDAT only when the transmission/reception of a byte has been completed. The end of transmission occurs after the eighth clock has been received if CPHA = 1, or when $\overline{SS}$ returns high if CPHA = 0.

POWER SUPPLY MONITOR

The power supply monitor, once enabled, monitors the DV_{DD} and AV_{DD} supplies on the devices. It indicates when any of the supply pins drop below one of four user-selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the power supply monitor function, AV_{DD} must be equal to or greater than 2.63 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor interrupts the core by using the PSMI bit in the PSMCON SFR. This bit is not cleared until the failing power supply returns above the trip point for at least 250 ms.

The monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution does not resume until a safe supply level is well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

The 5 V part has an internal POR trip level of 4.63 V, which means that there are no usable DV_{DD} PSM trip levels on the 5 V part. The 3 V part has a POR trip level of 2.63 V following a reset and initialization sequence, allowing all relevant PSM trip points to be used.

PSMCON—Power Supply Monitor Control Register

SFR Address: DFH
Power-On Default: DEH
Bit Addressable: No

Table 43. PSMCON SFR Bit Designations

Bit No.	Name	Description
7	CMPD	DV_{DD} Comparator Bit. This read-only bit directly reflects the state of the DV_{DD} comparator. Read 1 indicates that the DV_{DD} supply is above its selected trip point. Read 0 indicates that the DV_{DD} supply is below its selected trip point.
6	CMPA	AV_{DD} Comparator Bit. This read-only bit directly reflects the state of the AV_{DD} comparator. Read 1 indicates that the AV_{DD} supply is above its selected trip point. Read 0 indicates that the AV_{DD} supply is below its selected trip point.
5	PSMI	Power Supply Monitor Interrupt Bit. Set high by the MicroConverter if either CMPA or CMPD is low, indicating low analog or digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD and/or CMPA returns (and remains) high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user. However, if either comparator output is low, it is not possible for the user to clear PSMI.
4, 3	TPD1, TPD0	DV_{DD} Trip Point Selection Bits. A 5 V part has no valid PSM trip points. If the DV_{DD} supply falls below the 4.63 V point, the device resets (POR). For a 3 V part, all relevant PSM trip points are valid. The 3 V POR trip point is 2.63 V (fixed). These bits select the DV_{DD} trip point voltage as follows: TPD1 TPD0 Selected DV_{DD} Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
2, 1	TPA1, TPA0	AV_{DD} Trip Point Selection Bits. These bits select the AV_{DD} trip point voltage as follows: TPA1 TPA0 Selected AV_{DD} Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
0	PSMEN	Power Supply Monitor Enable Bit. Set to 1 by the user to enable the power supply monitor circuit. Cleared to 0 by the user to disable the power supply monitor circuit.

Timer 3 Generated Baud Rates

The high integer dividers in a UART block mean that high speed baud rates are not always possible. Also, generating baud rates requires the exclusive use of a timer, rendering it unusable for other applications when the UART is required. To address this problem, the ADuC845/ADuC847/ADuC848 have a dedicated baud rate timer (Timer 3) specifically for generating highly accurate baud rates. Timer 3 can be used instead of Timer 1 or Timer 2 for generating very accurate high speed UART baud rates including 115200 and 230400. Timer 3 also allows a much wider range of baud rates to be obtained. In fact, every desired bit rate from 12 bps to 393216 bps can be generated to within an error of ±0.8%. Timer 3 also frees up the other three timers, allowing them to be used for different applications. A block diagram of Timer 3 is shown in Figure 61.

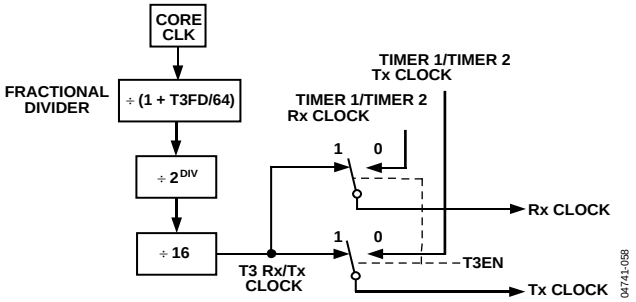

Figure 61. Timer 3, UART Baud Rate

Two SFRs (T3CON and T3FD) are used to control Timer 3. T3CON is the baud rate control SFR, allowing Timer 3 to be used to set up the UART baud rate, and to set up the binary divider (DIV).

The appropriate value to write to the DIV2-1-0 bits can be calculated using the following formula where f_{CORE} is defined in PLLCON SFR. Note that the DIV value must be rounded down.

$$DIV = \frac{\log\left(\frac{Core\ Clock\ Frequency}{16 \times Baud\ Rate}\right)}{\log(2)}$$

T3FD is the fractional divider ratio required to achieve the required baud rate. The appropriate value for T3FD can be calculated with the following formula:

$$T3FD = \frac{2 \times Core\ Clock\ Frequency}{2^{DIV-1} \times Baud\ Rate} - 64$$

Note that T3FD should be rounded to the nearest integer. Once the values for DIV and T3FD are calculated, the actual baud rate can be calculated with the following formula:

$$Actual\ Baud\ Rate = \frac{2 \times Core\ Clock\ Frequency}{2^{DIV-1} \times (T3FD + 64)}$$

For example, to get a baud rate of 9600 while operating at a core clock frequency of 1.5725 MHz, that is, CD = 3,

$$DIV = \log(1572500/(16 \times 9600))/\log 2 = 3.35 = 3$$

Note that the DIV result is rounded down.

$$T3FD = (2 \times 1572500)/(2^{3-1} \times 9600) - 64 = 18 = 12H$$

Therefore, the actual baud rate is 9588 bps, which gives an error of 0.12%.

The T3CON and T3FD registers are used to control Timer 3.

T3CON – Timer 3 Control Register

SFR Address: 9EH
Power-On Default: 00H
Bit Addressable: No

Table 57. Common Baud Rates Using Timer 3 with a 12.58 MHz PLL Clock

Ideal Baud	CD	DIV	T3CON	T3FD	% Error
230400	0	1	81H	2DH	0.18
115200	0	2	82H	2DH	0.18
115200	1	1	81H	2DH	0.18
57600	0	3	83H	2DH	0.18
57600	1	2	82H	2DH	0.18
57600	2	1	81H	2DH	0.18
38400	0	4	84H	12H	0.12
38400	1	3	83H	12H	0.12
38400	2	2	82H	12H	0.12
38400	3	1	81H	12H	0.12
19200	0	5	85H	12H	0.12
19200	1	4	84H	12H	0.12
19200	2	3	83H	12H	0.12
19200	3	2	82H	12H	0.12
19200	4	1	81H	12H	0.12
9600	0	6	86H	12H	0.12
9600	1	5	85H	12H	0.12
9600	2	4	84H	12H	0.12
9600	3	3	83H	12H	0.12
9600	4	2	82H	12H	0.12
9600	5	1	81H	12H	0.12

INTERRUPT SYSTEM

The ADuC845/ADuC847/ADuC848 provide nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE Interrupt Enable Register
IP Interrupt Priority Register
IEIP2 Secondary Interrupt Enable Register

IE—Interrupt Enable Register

SFR Address: A8H
Power-On Default: 00H
Bit Addressable: Yes

Table 58. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	Set by the user to enable External Interrupt 1 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 1 ($\overline{INT0}$).
1	ET0	Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	Set by the user to enable External Interrupt 0 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 0 ($\overline{INT0}$).

IP—Interrupt Priority Register

SFR Address: B8H
Power-On Default: 00H
Bit Addressable: Yes

Table 59. IP SFR Bit Designations

Bit No.	Name	Description
7	-----	Not Implemented. Write Don't Care.
6	PADC	ADC Interrupt Priority (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	PX1	$\overline{INT0}$ (External Interrupt 1) priority (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	PX0	$\overline{INT0}$ (External Interrupt 0) Priority (1 = High; 0 = Low).

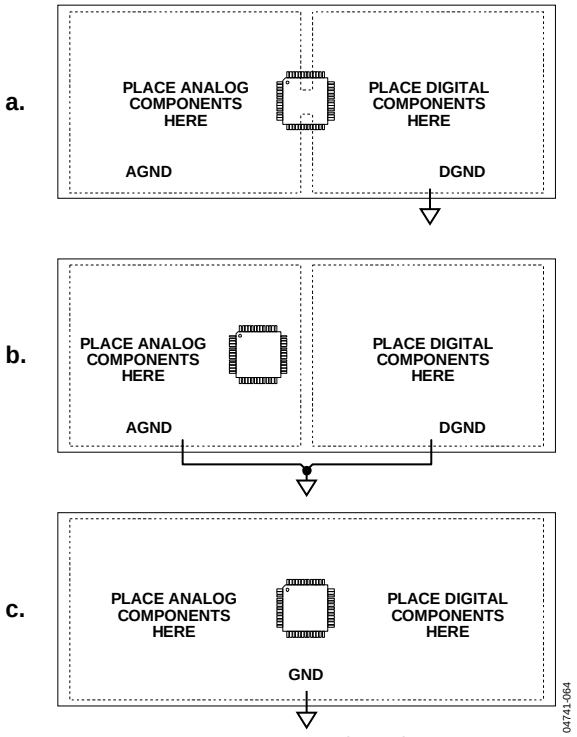

Figure 68. System Grounding Schemes

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the digital inputs of the ADuC845/ADuC847/ADuC848 add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the device. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the device and affecting the accuracy of ADC conversions.

When using the LFCSP package, it is recommended that the paddle underneath the chip be soldered to the board to provide maximum mechanical stability. However, it is recommended that this paddle not be grounded but left floating. All results and specifications contained in this data sheet are taken or recorded with the paddle floating.

System Self-Identification

In some hardware designs, it may be advantageous for the software to be able to identify the host MicroConverter.

The CHIPID SFR is a read-only register located at SFR address C2H. The upper nibble of this SFR designates the MicroConverter within the Σ-Δ ADC family. User software can read this SFR to identify the host MicroConverter and therefore execute slightly different code if required. The CHIPID SFR reads as follows for the Σ-Δ ADC family of MicroConverter products. Note that the ADuC845/ADuC847/ADuC848 are treated as one device as far as the CHIPID is concerned.

Table 63. CHIPID Values for Σ-Δ MicroConverter Products

Device	CHIPID
ADuC816	1xH
ADuC824	0xH
ADuC836	3xH
ADuC834	2xH
ADuC845/ADuC847/ADuC848	AxH

Clock Oscillator

As described earlier, the core clock frequency for the ADuC845/ADuC847/ADuC848 is generated from an on-chip PLL that locks onto a multiple (384 times) of 32.768 kHz. The latter is generated from an internal clock oscillator. To use the internal clock oscillator, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2 as shown in Figure 69.

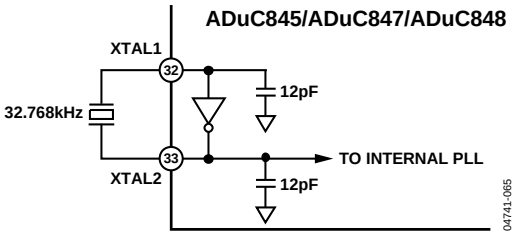

Figure 69. Crystal Connectivity to ADuC845/ADuC847/ADuC848

As shown in the typical external crystal connection diagram in Figure 69, two internal 12 pF capacitors are provided on-chip. These are connected internally, directly to the XTAL1 and XTAL2 pins. The total input capacitance at both pins is detailed in the Specifications table. Note that the total capacitance required for a particular crystal must be in accordance with the crystal manufacturer. However, in most cases, no additional external capacitance is required above that already supplied on-chip.

OTHER HARDWARE CONSIDERATIONS

In-Circuit Serial Download Access

Nearly all ADuC845/ADuC847/ADuC848 designs can take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the UART of the devices, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is shown in Figure 70 with a simple ADM3202-based circuit. If users would rather not include an RS-232 chip on the target board, refer to the uC006 Application Note, *A 4-Wire UART-to-PC Interface*, for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the device.

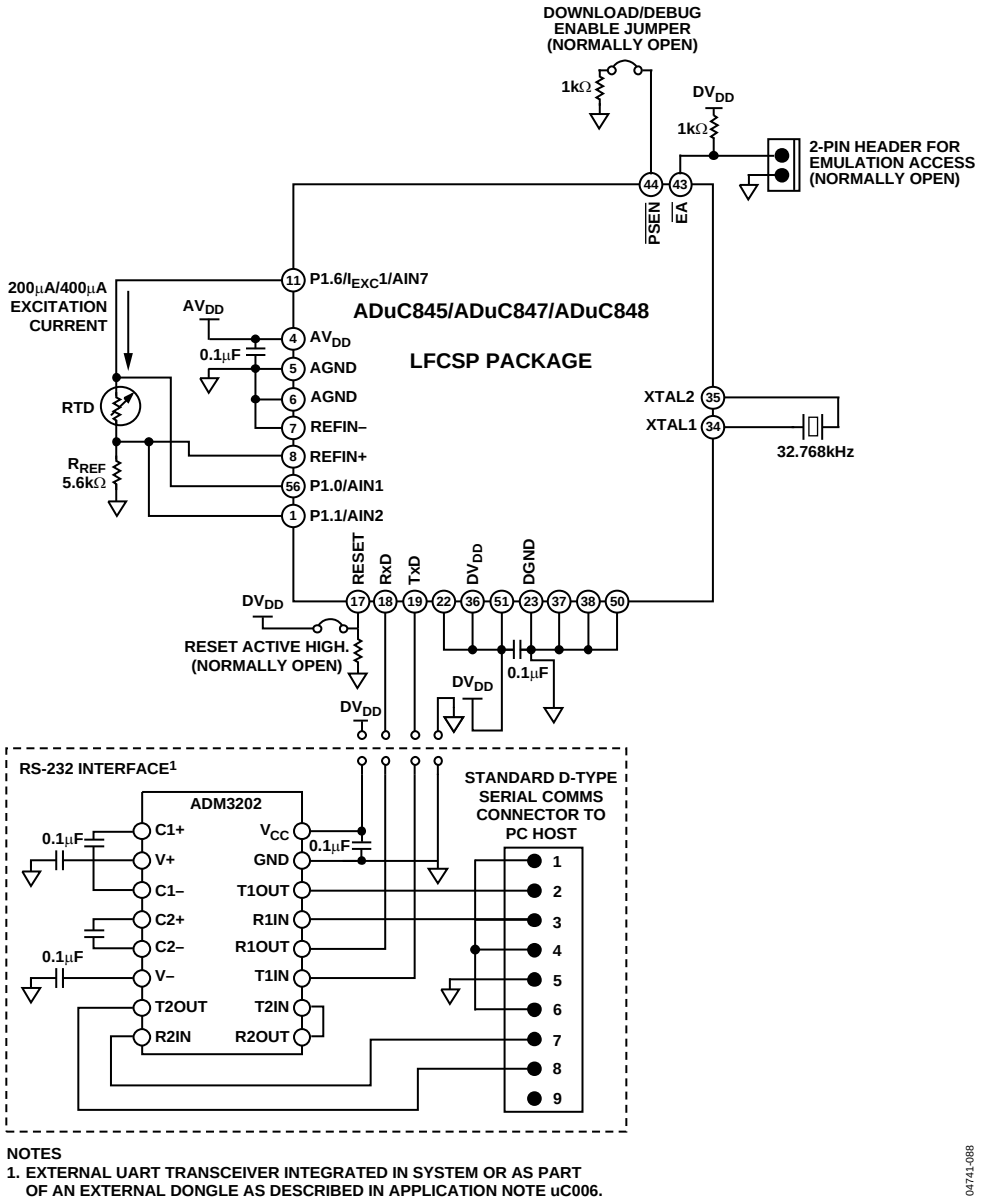

Figure 70. UART Connectivity in Typical System

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 70. To get the devices into download mode, connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it is ready to receive a new program serially. With the jumper removed, the device powers on in normal mode (and runs the program) whenever power is cycled or RESET is toggled. Note that $\overline{\text{PSEN}}$ is normally an output and that it is sampled as an input only on the falling edge of RESET, that is, at power-on or upon an external manual reset. Note also that if any external circuitry unintentionally pulls $\overline{\text{PSEN}}$ low during power-on or reset events, it may cause the chip to enter download mode and fail to begin user code execution. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself or the method of download entry in use during a reset or power-cycle condition.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described previously. In fact, both serial download and serial port debug modes are essentially one mode of operation used in two different ways.

The serial port debugger is fully contained on the device, unlike ROM monitor type debuggers, and, therefore, no external memory is needed to enable in-system debug sessions.

TIMING SPECIFICATIONS

AC inputs during testing are driven at DV_{DD} – 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements are made at V_{IH} min for Logic 1 and V_{IL} max for Logic 0 as shown in Figure 72.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 72.

C_{LOAD} for all outputs = 80 pF, unless otherwise noted.

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 64. CLOCK INPUT (External Clock Driven XTAL1) Parameter

		32.768 kHz External Crystal			
		Min	Typ	Max	Unit
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		6.26		µs
t_{CKH}	XTAL1 Width High		6.26		µs
t_{CKR}	XTAL1 Rise Time		9		ns
t_{CKF}	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	Core Clock Frequency[1]	0.098	1.57	12.58	MHz
t_{CORE}	Core Clock Period[2]		0.636		µs
t_{CYC}	Machine Cycle Time[3]	10.2	0.636	0.08	µs

[1] ADuC845/ADuC847/ADuC848 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 12.58 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[2] This number is measured at the default Core_Clk operating frequency of 1.57 MHz.
[3] ADuC845/ADuC847/ADuC848 machine cycle time is nominally defined as 1/Core_Clk.

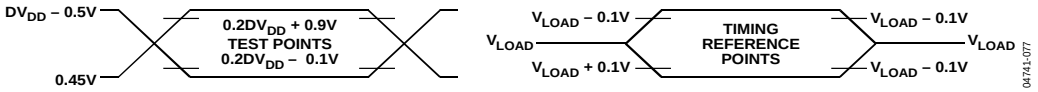

Figure 72. Timing Waveform Characteristics

Table 66. EXTERNAL DATA MEMORY WRITE CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{WLWH}	$\overline{WR}$ Pulse Width	65		130		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	65		135		ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low		130		260	ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	60		120		ns
t_{QVWH}	Data Setup Before $\overline{WR}$	120		250		ns
t_{WHQX}	Data and Address Hold After $\overline{WR}$	380		755		ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		125		ns

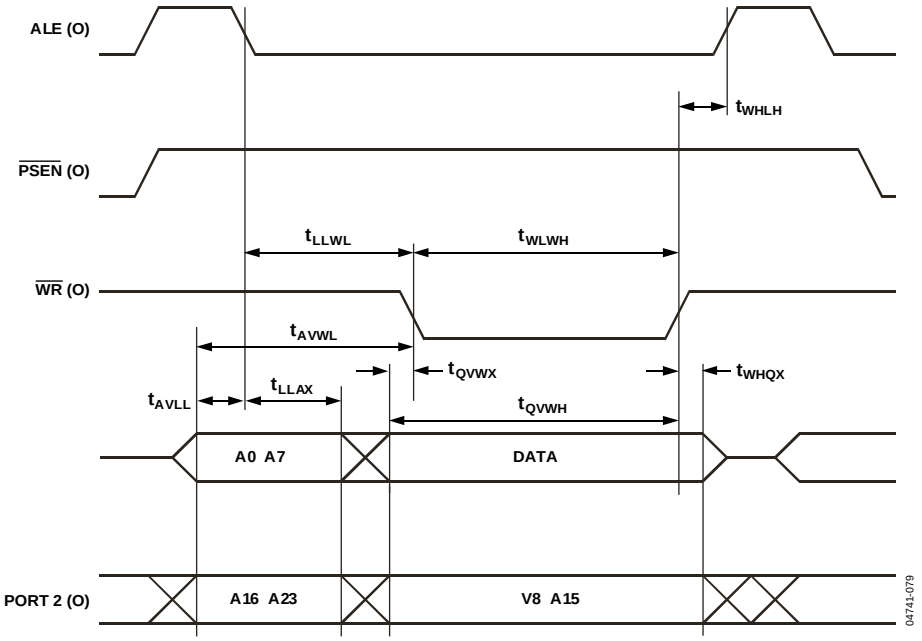

Figure 74. External Data Memory Write Cycle

Table 67. I²C-COMPATIBLE INTERFACE TIMING Parameter

Parameter		Min	Max	Unit
t_L	SCLCK Low Pulse Width	1.3		µs
t_H	SCLCK High Pulse Width	0.6		µs
t_{SHD}	Start Condition Hold Time	0.6		µs
t_{DSU}	Data Setup Time	100		µs
t_{DHD}	Data Hold Time		0.9	µs
t_{RSU}	Setup Time for Repeated Start	0.6		µs
t_{PSU}	Stop Condition Setup Time	0.6		µs
t_{BUF}	Bus Free Time Between a Stop Condition and a Start Condition	1.3		µs
t_R	Rise Time of Both SCLCK and SDATA		300	ns
t_F	Fall Time of Both SCLCK and SDATA		300	ns
t_{SUP}[1]	Pulse Width of Spike Suppressed		50	ns

[1] Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.