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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc845bsz62-5-rl

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSDUCER BURNOUT CURRENT SOURCES					
AIN+ Current		−100		nA	AIN+ is the selected positive input (AIN4 or AIN6 only) to the primary ADC
AIN− Current		100		nA	AIN− is the selected negative input (AIN5 or AIN7 only) to the primary ADC
Initial Tolerance at 25°C		±10		%	
Drift		0.03		%/°C	
EXCITATION CURRENT SOURCES					
Output Current		200		µA	Available from each current source
Initial Tolerance at 25°C		±10		%	
Drift		200		ppm/°C	
Initial Current Matching at 25°C		±1		%	Matching between both current sources
Drift Matching		20		ppm/°C	
Line Regulation (AV_{DD})		1		µA/V	AV_{DD} = 5 V ± 5%
Load Regulation		0.1		µA/V	
Output Compliance[2]	AGND		AV_{DD} − 0.6	V	
POWER SUPPLY MONITOR (PSM)					
AV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
AV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
DV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
DV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)					
Logic Inputs, XTAL1 Only[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	3.5			V	DV_{DD} = 5 V
	2.5			V	DV_{DD} = 3 V
XTAL1 Input Capacitance		18		pF	
XTAL2 Output Capacitance		18		pF	
LOGIC INPUTS					
All Inputs Except SCLOCK, RESET, and XTAL1[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	2.0			V	
SCLOCK and RESET Only (Schmidt Triggered Inputs)[2]					
V_{T+}	1.3		3.0	V	DV_{DD} = 5 V
	0.95		2.5	V	DV_{DD} = 3 V
V_{T-}	0.8		1.4	V	DV_{DD} = 5 V
	0.4		1.1	V	DV_{DD} = 3 V
$V_{T+} - V_{T-}$	0.3		0.85	V	DV_{DD} = 5 V or 3 V
Input Currents					
Port 0, P1.0 to P1.7, $\overline{EA}$			±10	µA	V_{IN} = 0 V or V_{DD}
RESET			±10	µA	V_{IN} = 0 V, DV_{DD} = 5 V
	35		105	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V, internal pull-down
Port 2, Port 3			±10	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V
	−180		−660	µA	V_{IN} = 2 V, DV_{DD} = 5 V
	−20		−75	µA	V_{IN} = 0.45 V, DV_{DD} = 5 V
Input Capacitance		10		pF	All digital inputs

FUNCTIONAL DESCRIPTION

8051 INSTRUCTION SET

Table 4. Optimized Single-Cycle 8051 Instruction Set

Mnemonic	Description	Bytes	Cycles[1]
Arithmetic			
A A,Rn	Add register to A	1	1
ADD A,@Ri	Add indirect memory to A	1	2
ADD A,dir	Add direct byte to A	2	2
ADD A,#data	Add immediate to A	2	2
ADDC A,Rn	Add register to A with carry	1	1
ADDC A,@Ri	Add indirect memory to A with carry	1	2
ADDC A,dir	Add direct byte to A with carry	2	2
ADD A,#data	Add immediate to A with carry	2	2
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2
SUBB A,dir	Subtract direct from A with borrow	2	2
SUBB A,#data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC @Ri	Increment indirect memory	1	2
INC dir	Increment direct byte	2	2
INC DPTR	Increment data pointer	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC @Ri	Decrement indirect memory	1	2
DEC dir	Decrement direct byte	2	2
MUL AB	Multiply A by B	1	4
DIV AB	Divide A by B	1	9
DA A	Decimal adjust A	1	2
Logic			
ANL A,Rn	AND register to A	1	1
ANL A,@Ri	AND indirect memory to A	1	2
ANL A,dir	AND direct byte to A	2	2
ANL A,#data	AND immediate to A	2	2
ANL dir,A	AND A to direct byte	2	2
ANL dir,#data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to A	1	1
ORL A,@Ri	OR indirect memory to A	1	2
ORL A,dir	OR direct byte to A	2	2
ORL A,#data	OR immediate to A	2	2
ORL dir,A	OR A to direct byte	2	2
ORL dir,#data	OR immediate data to direct byte	3	3
XRL A,Rn	Exclusive-OR register to A	1	1
XRL A,@Ri	Exclusive-OR indirect memory to A	2	2
XRL A,#data	Exclusive-OR immediate to A	2	2
XRL dir,A	Exclusive-OR A to direct byte	2	2
XRL A,dir	Exclusive-OR indirect memory to A	2	2
XRL dir,#data	Exclusive-OR immediate data to direct	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1

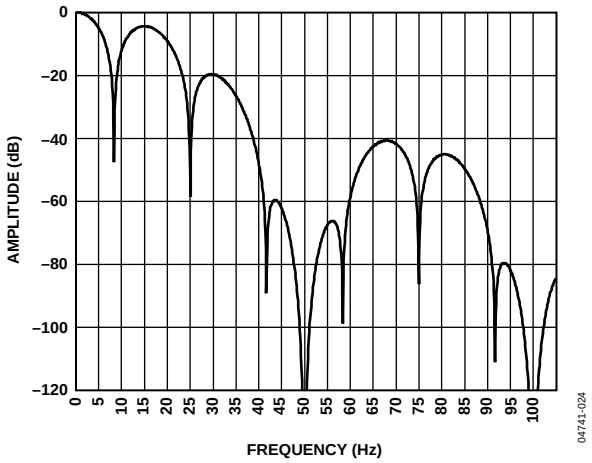

Figure 24. Chop On, Fadc = 16.6 Hz, SF = 52H

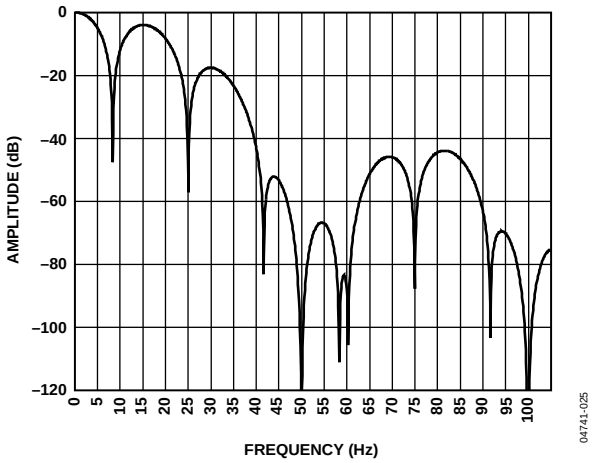

Figure 25. Chop On, Fadc = 16.6 Hz, SF = 52H, REJ60 Enabled

ADCSTAT (ADC STATUS REGISTER)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including REFIN± reference detect and conversion overflow/underflow flags.

SFR Address: D8H
Power-On Default: 00H
Bit Addressable: Yes

Table 23. ADCSTAT SFR Bit Designation

Bit No.	Name	Description
7	RDY0	Ready Bit for the Primary ADC. Set by hardware on completion of conversion or calibration. Cleared directly by the user, or indirectly by a write to the mode bits, to start calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary (ADuC845 only) ADC. Same definition as RDY0 referred to the auxiliary ADC. Valid on the ADuC845 only.
5	CAL	Calibration Status Bit. Set by hardware on completion of calibration. Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration. Note that calibration with the temperature sensor selected (auxiliary ADC on the ADuC845 only) fails to complete.
4	NOXREF	No External Reference Bit (only active if primary or auxiliary (ADuC845 only) ADC is active). Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When set, conversion results are clamped to all 1s. Only detects invalid REFIN±, does not check REFIN2±. Cleared to indicate valid V_{REF}.
3	ERR0	Primary ADC Error Bit. Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC. Valid on the ADuC845 only.
1	–––	Not Implemented. Write Don't Care.
0	–––	Not Implemented. Write Don't Care.

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is shown in Figure 33.

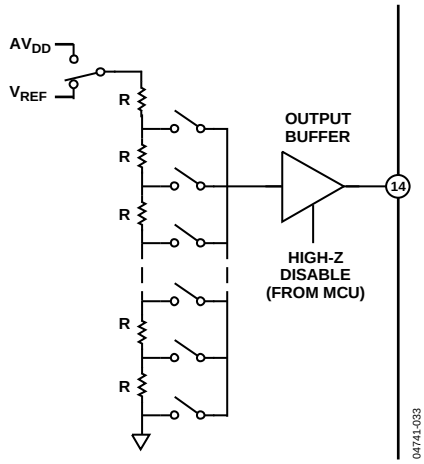

Figure 33. Resistor String DAC Functional Equivalent

Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity. As shown in Figure 33, the reference source for the DAC is user-selectable in software. It can be either AV_{DD} or V_{REF}. In 0 V-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF} (2.5 V). The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that, unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 48 in 0 V-to-V_{REF} mode; Codes 0 to 100; and Codes 3950 to 4095 in 0 V-to-V_{DD} mode.

Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier; a general representation of its effects (neglecting offset and gain error) is shown in Figure 34. The dotted line indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier.

Note that Figure 34 represents a transfer function in 0-to-V_{DD} mode only. In 0 V-to-V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line to the end, showing no signs of the high-end endpoint linearity error.

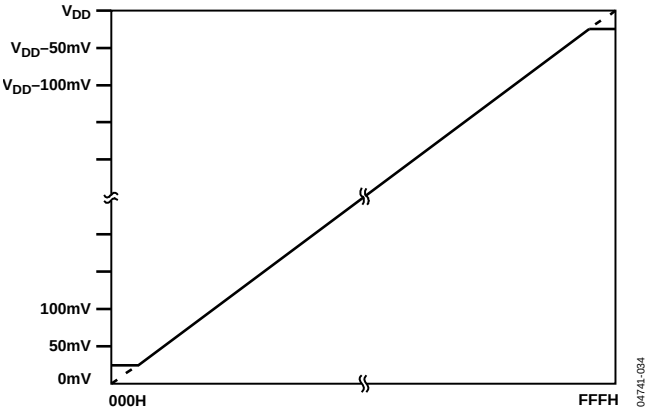

Figure 34. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities shown in Figure 34 become worse as a function of output loading. Most data sheet specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom, respectively, of Figure 34 become larger. With larger current demands, this can significantly limit output voltage swing. Figure 35 and Figure 36 illustrate this behavior. Note that the upper trace in each of these figures is valid only for an output range selection of 0 V to AV_{DD}. In 0 V-to-V_{REF} mode, DAC loading does not cause high-side voltage nonlinearities while the reference voltage remains below the upper trace in the corresponding figure. For example, if AV_{DD} = 3 V and V_{REF} = 2.5 V, the high-side voltage is not affected by loads of less than 5 mA. But around 7 mA, the upper curve in Figure 36 drops below 2.5 V (V_{REF}), indicating that at these higher currents, the output is not capable of reaching V_{REF}.

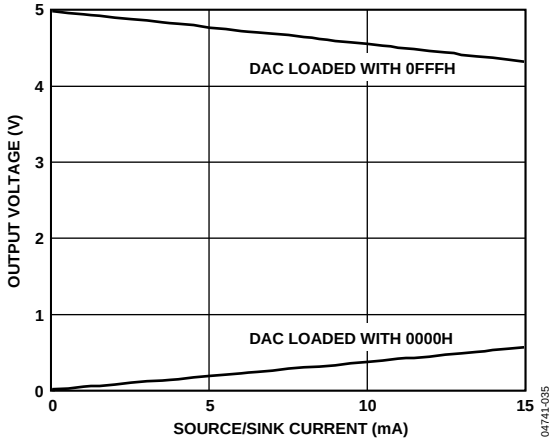

Figure 35. Source and Sink Current Capability with $V_{REF} = AV_{DD} = 5$ V

PWMCON PWM Control SFR

SFR Address: AEH
Power-On Default: 00H
Bit Addressable: No

Table 34. PWMCON PWM Control SFR

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6, 5, 4	PWM2, PWM1, PWM0	PMW Mode Selection. PWM2 PWM1 PWM0 0 0 0 Mode 0: PWM disabled. 0 0 1 Mode 1: Single 16-bit output with programmable pulse and cycle time. 0 1 0 Mode 2: Twin 8-bit outputs. 0 1 1 Mode 3: Twin 16-bit outputs. 1 0 0 Mode 4: Dual 16-bit pulse density outputs. 1 0 1 Mode 5: Dual 8-bit outputs. 1 1 0 Mode 6: Dual 16-bit pulse density RZ outputs. 1 1 1 Mode 7: PWM counter reset with outputs not used.
3, 2	PWS1, PWS0	PWM Clock Source Divider. PWS1 PWS0 0 0 Selected clock. 0 1 Selected clock divided by 4. 1 0 Selected clock divided by 16. 1 1 Selected clock divided by 64.
1, 0	PWC1, PWC0	PWM Clock Source Selection. PWC1 PWC0 0 0 F_{XTAL}/15 (2.184 kHz). 0 1 F_{XTAL} (32.768 kHz). 1 0 External input on P2.7. 1 1 F_{VCO} (12.58 MHz).

PWM Pulse Width High Byte (PWM0H)

SFR Address: B2H
Power-On Default: 00H
Bit Addressable: No

Table 35. PWM0H: PWM Pulse Width High Byte

PWM0H.7	PWM0H.6	PWM0H.5	PWM0H.4	PWM0H.3	PWM0H.2	PWM0H.1	PWM0H.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Pulse Width Low Byte (PWM0L)

SFR Address: B1H
Power-On Default: 00H
Bit Addressable: No

The outputs of the PWM at P2.5 and P2.6 are shown in Figure 40. As can be seen, the output of PWM0 (P2.5) goes low when the PWM counter equals PWM0L. The output of PWM1 (P2.6) goes high when the PWM counter equals PWM1H and goes low again when the PWM counter equals PWM0H. Setting PWM1H to 0 ensures that both PWM outputs start simultaneously.

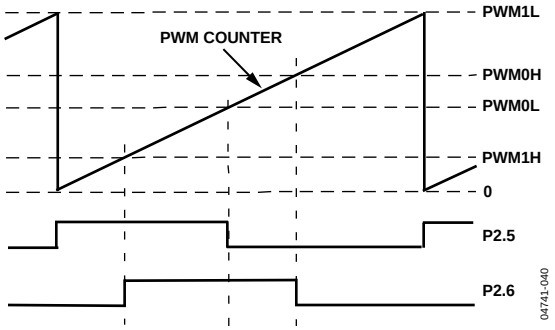

Figure 40. PWM Mode 2

Mode 3 (Twin 16-Bit PWM)

In Mode 3, the PWM counter is fixed to count from 0 to 65536, giving a fixed 16-bit PWM. Operating from the 12.58 MHz core clock results in a PWM output rate of 192 Hz. The duty cycle of the PWM outputs at P2.5 and P2.6 are independently programmable.

As shown in Figure 41, while the PWM counter is less than PWM0H/L, the output of PWM0 (P2.5) is high. Once the PWM counter equals PWM0H/L, PWM0 (P2.5) goes low and remains low until the PWM counter rolls over.

Similarly, while the PWM counter is less than PWM1H/L, the output of PWM1 (P2.6) is high. Once the PWM counter equals PWM1H/L, PWM1 (P2.6) goes low and remains low until the PWM counter rolls over.

In this mode, both PWM outputs are synchronized, that is, once the PWM counter rolls over to 0, both PWM0 (P2.5) and PWM1 (P2.6) go high.

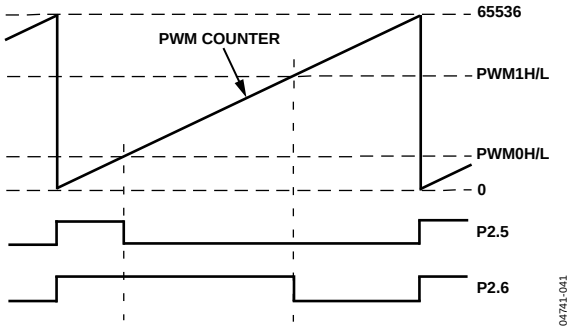

Figure 41. PWM Mode 3

Mode 4 (Dual NRZ 16-Bit Σ-Δ DAC)

Mode 4 provides a high speed PWM output similar to that of a Σ-Δ DAC. Typically, this mode is used with the PWM clock equal to 12.58 MHz.

In this mode, P2.5 and P2.6 are updated every PWM clock (80 ns in the case of 12.58 MHz). Over any 65536 cycles (16-bit PWM), PWM0 (P2.5) is high for PWM0H/L cycles and low for (65536 – PWM0H/L) cycles. Similarly, PWM1 (P2.6) is high for PWM1H/L cycles and low for (65536 – PWM1H/L) cycles.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three clocks and high for one clock (each clock is approximately 80 ns). Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale, by having a high cycle followed by only two low cycles.

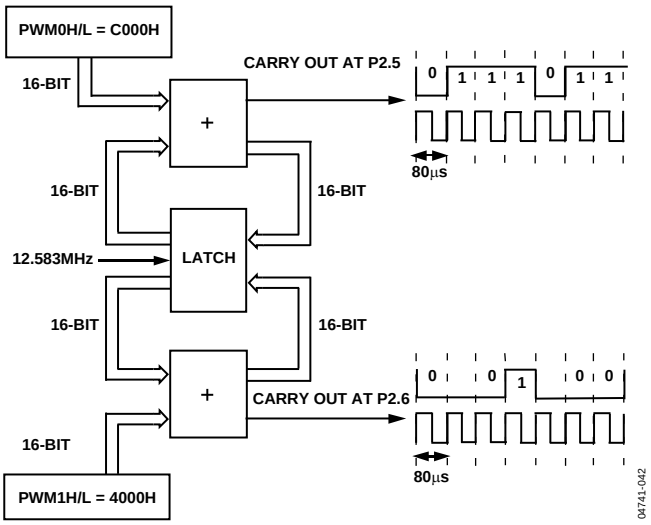

Figure 42. PWM Mode 4

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

I²C SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 support a fully licensed I²C serial interface. The I²C interface is implemented as a full hardware slave and software master. SDATA (Pin 27 on the MQFP package and Pin 29 on the LFCSP package) is the data I/O pin. SCLK (Pin 26 on the MQFP package and Pin 28 on the LFCSP package) is the serial interface clock for the SPI interface. The I²C interface on the devices is fully independent of all other pin/function multiplexing. The I²C interface incorporated on the ADuC845/ADuC847/ADuC848 also includes a second address register (I2CADD1) at SFR Address F2H with a default power-on value of 7FH. The I²C interface is always available to the user and is not multiplexed with any other I/O functionality on the chip. This means that the I²C and SPI interfaces can be used at the same time.

Note that when using the I²C and SPI interfaces simultaneously, they both use the same interrupt routine (Vector Address 3BH). When an interrupt occurs from one of these, it is necessary to interrogate each interface to see which one has triggered the ISR request.

The four SFRs that are used to control the I²C interface are described next.

I2CCON—I²C Control Register

SFR Address: E8H
Power-On Default: 00H
Bit Addressable: Yes

Table 40. I2CCON SFR Bit Designations

Bit No.	Name	Description
7	MDO	I²C Software Master Data Output Bit (master mode only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SDATA pin if the data output enable bit (MDE) is set.
6	MDE	I²C Software Output Enable Bit (master mode only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable the SDATA pin as an input (Rx).
5	MCO	I²C Software Master Clock Output Bit (master mode only). This bit is used to implement the SCLK for a master I²C transmitter in software. Data written to this bit is output on the SCLK pin.
4	MDI	I²C Software Master Data Input Bit (master mode only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on an SCLK transition if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (slave mode only). Set by the user to reset the I²C interface. Cleared by the user code for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (slave mode only). Set by the MicroConverter if the I²C interface is transmitting. Cleared by the MicroConverter if the I²C interface is receiving.
0	I2CI	I²C Interrupt Bit (slave mode only). Set by the MicroConverter after a byte has been transmitted or received. Cleared by the MicroConverter when the user code reads the I2CDAT SFR. I2CI should not be cleared by user code.

SPICON—SPI Control Register

SFR Address: F8H
Power-On Default: 05H
Bit Addressable: Yes

Table 41. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user code to enable SPI functionality. Cleared by user code to enable standard Port 2 functionality.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user code to enable master mode operation (SCLOCK is an output). Cleared by user code to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Bit. Set by user code to enable SCLOCK idle high. Cleared by user code to enable SCLOCK idle low.
2	CPHA[1]	Clock Phase Select Bit. Set by user code if the leading SCLOCK edge is to transmit data. Cleared by user code if the trailing SCLOCK edge is to transmit data.
1, 0	SPR1, SPR0	SPI Bit-Rate Bits. SPR1 SPR0 Selected Bit Rate 0 0 $f_{core}/2$ 0 1 $f_{core}/4$ 1 0 $f_{core}/8$ 1 1 $f_{core}/16$

[1] The CPOL and CPHA bits should both contain the same values for master and slave devices.

Note that both SPI and I²C use the same ISR (Vector Address 3BH); therefore, when using SPI and I²C simultaneously, it is necessary to check the interfaces following an interrupt to determine which one caused the interrupt.

SPIDAT: SPI Data Register

SFR Address: 7FH
Power-On Default: 00H
Bit Addressable: No

INTVAL—User Timer Interval Select Register

Function:	User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled.
SFR Address:	A6H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 255 decimal

HTHSEC—Hundredths of Seconds Time Register

Function:	This register is incremented in 1/128-second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address:	A2H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 127 decimal

SEC—Seconds Time Register

Function:	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address:	A3H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

MIN—Minutes Time Register

Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59 before rolling over to increment the HOUR time register.
SFR Address:	A4H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

HOUR—Hours Time Register

Function:	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. The HOUR SFR counts from 0 to 23 before rolling over to 0.
SFR Address:	A5H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 23 decimal

To enable the TIC as a real-time clock, the HOUR, MIN, SEC, and HTHSEC registers can be loaded with the current time. Once the TCEN bit is high, the TIC starts. To use the TIC as a time interval counter, select the count interval—hundredths of seconds, seconds, minutes, and hours via the ITS0 and ITS1 bits in the TIMECON SFR. Load the count required into the INTVAL SFR.

Note that INTVAL is only an 8-bit register, so user software must take into account any intervals longer than are possible with 8 bits. Therefore, to count an interval of 20 seconds, use the following procedure:

```
MOV TIMECON, #0D0H ;Enable 24Hour mode, count seconds, Clear TCEN.
MOV INTVAL,  #14H  ;Load INTVAL with required count interval...in this case 14H = 20
MOV TIMECON, #0D3H ;Start TIC counting and enable the 8bit INTVAL counter.
```

Timer/Counter 0 and 1 Operating Modes

This section describes the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 52 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

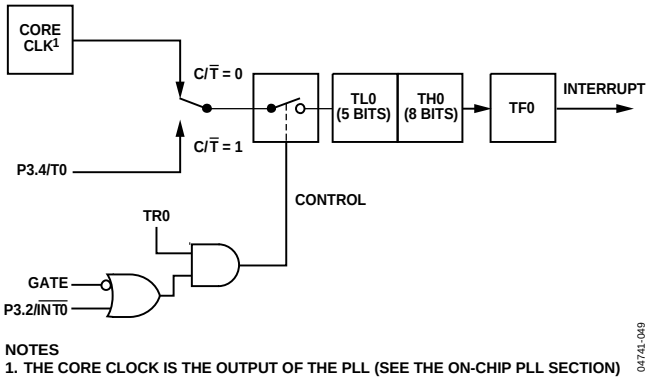

Figure 52. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 53.

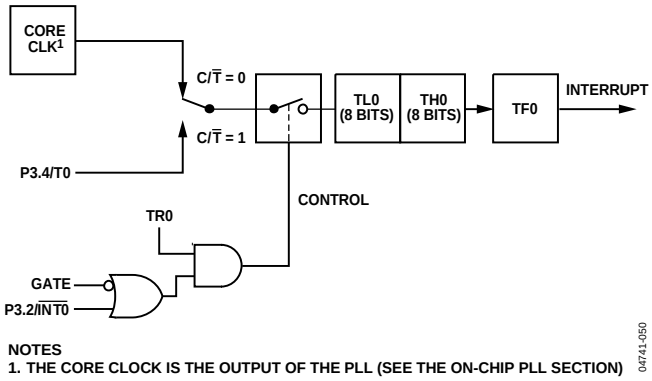

Figure 53. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload as shown in Figure 54. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

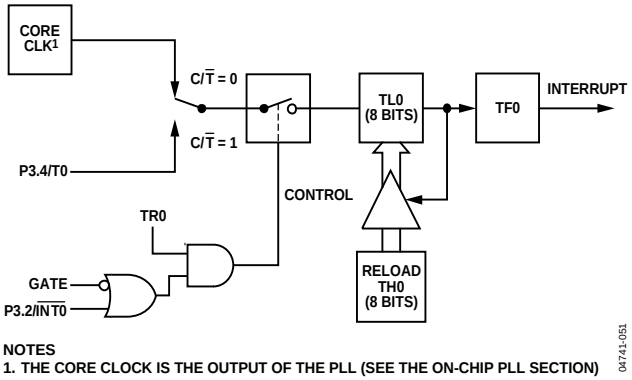

Figure 54. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 55. TL0 uses the Timer 0 Control Bits C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 then controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

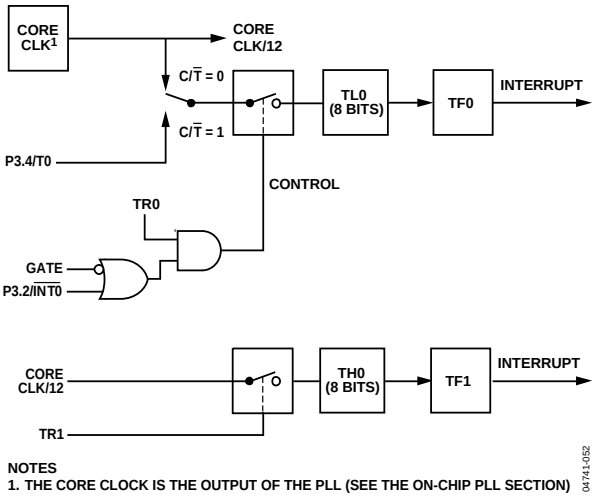

Figure 55. Timer/Counter 0, Mode 3

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART Serial Port Baud Rate Generation

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(\frac{CoreClockFrequency}{12}\right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Core\ Clock\ Frequency$$

Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or in both (one for transmit and the other for receive).

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{CoreClockFrequency}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{1}{16} \times Timer\ 2\ Overflow\ Rate$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 60.

In this case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{Core\ \ Clock\ \ Frequency}{(16 \times [65536\ - (RCAP\ 2H\ :RCAP\ 2L)])}$$

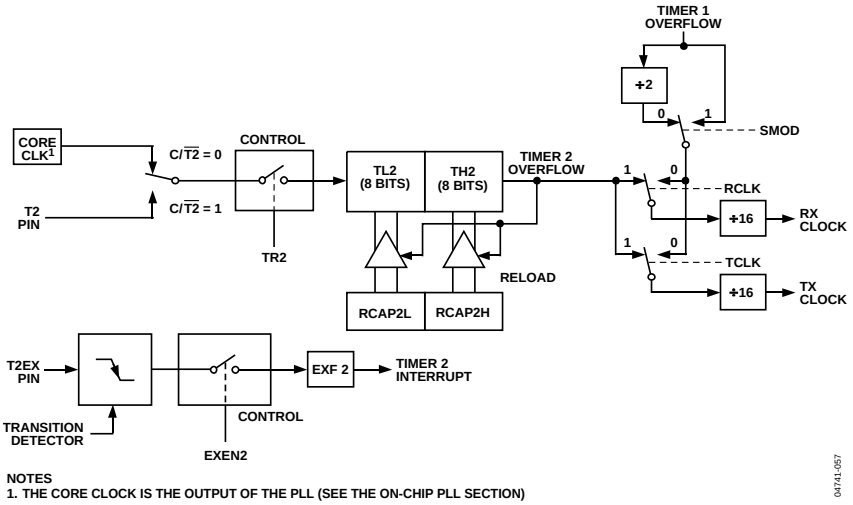

Figure 60. Timer 2, UART Baud Rates

Table 57. Common Baud Rates Using Timer 3 with a 12.58 MHz PLL Clock

Ideal Baud	CD	DIV	T3CON	T3FD	% Error
230400	0	1	81H	2DH	0.18
115200	0	2	82H	2DH	0.18
115200	1	1	81H	2DH	0.18
57600	0	3	83H	2DH	0.18
57600	1	2	82H	2DH	0.18
57600	2	1	81H	2DH	0.18
38400	0	4	84H	12H	0.12
38400	1	3	83H	12H	0.12
38400	2	2	82H	12H	0.12
38400	3	1	81H	12H	0.12
19200	0	5	85H	12H	0.12
19200	1	4	84H	12H	0.12
19200	2	3	83H	12H	0.12
19200	3	2	82H	12H	0.12
19200	4	1	81H	12H	0.12
9600	0	6	86H	12H	0.12
9600	1	5	85H	12H	0.12
9600	2	4	84H	12H	0.12
9600	3	3	83H	12H	0.12
9600	4	2	82H	12H	0.12
9600	5	1	81H	12H	0.12

INTERRUPT SYSTEM

The ADuC845/ADuC847/ADuC848 provide nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE Interrupt Enable Register
IP Interrupt Priority Register
IEIP2 Secondary Interrupt Enable Register

IE—Interrupt Enable Register

SFR Address: A8H
Power-On Default: 00H
Bit Addressable: Yes

Table 58. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	Set by the user to enable External Interrupt 1 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 1 ($\overline{INT0}$).
1	ET0	Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	Set by the user to enable External Interrupt 0 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 0 ($\overline{INT0}$).

IP—Interrupt Priority Register

SFR Address: B8H
Power-On Default: 00H
Bit Addressable: Yes

Table 59. IP SFR Bit Designations

Bit No.	Name	Description
7	-----	Not Implemented. Write Don't Care.
6	PADC	ADC Interrupt Priority (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	PX1	$\overline{INT0}$ (External Interrupt 1) priority (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	PX0	$\overline{INT0}$ (External Interrupt 0) Priority (1 = High; 0 = Low).

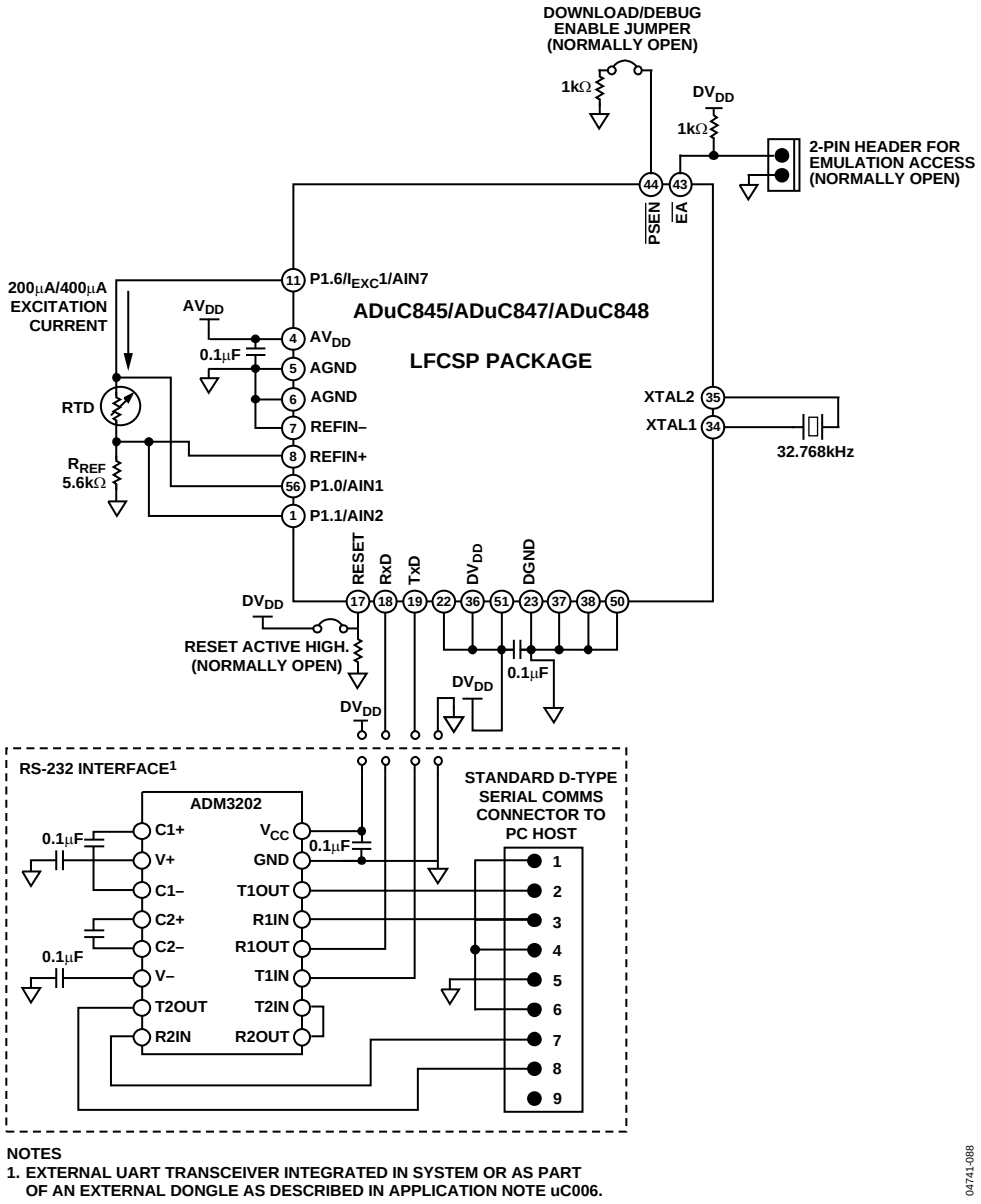

Figure 70. UART Connectivity in Typical System

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 70. To get the devices into download mode, connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it is ready to receive a new program serially. With the jumper removed, the device powers on in normal mode (and runs the program) whenever power is cycled or RESET is toggled. Note that $\overline{\text{PSEN}}$ is normally an output and that it is sampled as an input only on the falling edge of RESET, that is, at power-on or upon an external manual reset. Note also that if any external circuitry unintentionally pulls $\overline{\text{PSEN}}$ low during power-on or reset events, it may cause the chip to enter download mode and fail to begin user code execution. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself or the method of download entry in use during a reset or power-cycle condition.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described previously. In fact, both serial download and serial port debug modes are essentially one mode of operation used in two different ways.

The serial port debugger is fully contained on the device, unlike ROM monitor type debuggers, and, therefore, no external memory is needed to enable in-system debug sessions.

Table 65. EXTERNAL DATA MEMORY READ CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{RLRH}	$\overline{RD}$ Pulse Width	60		125		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	145		290		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		48		100	ns
t_{RHDX}	Data and Address Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		150		625	ns
t_{LLDV}	ALE Low to Valid Data In		170		350	ns
t_{AVDV}	Address to Valid Data In		230		470	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	130		255		ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		15		35	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		120		ns

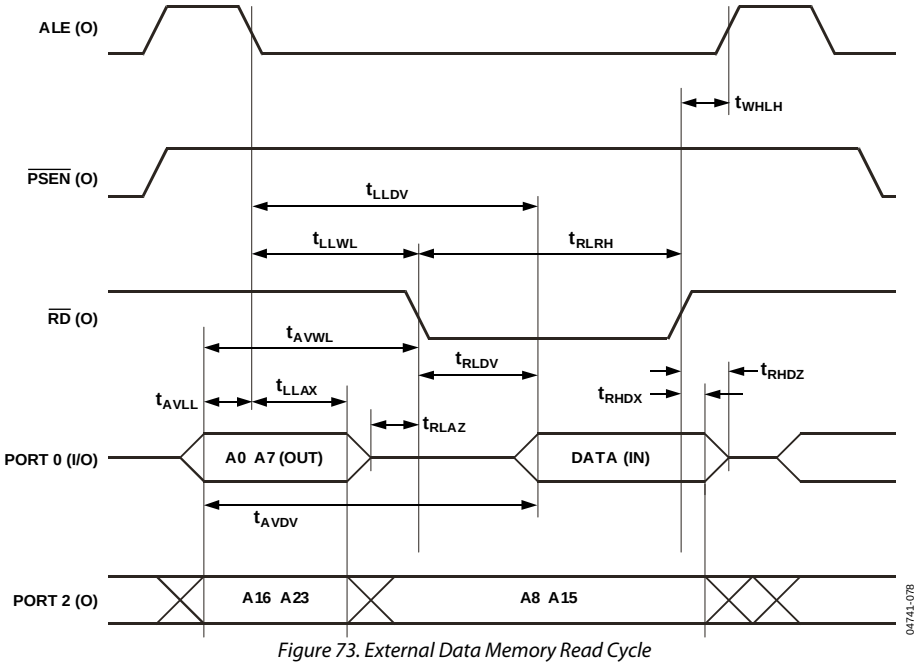

Figure 73. External Data Memory Read Cycle

Table 68. SPI MASTER MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		635		ns
t_{SH}	SCLOCK High Pulse Width[1]		635		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 1.57 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

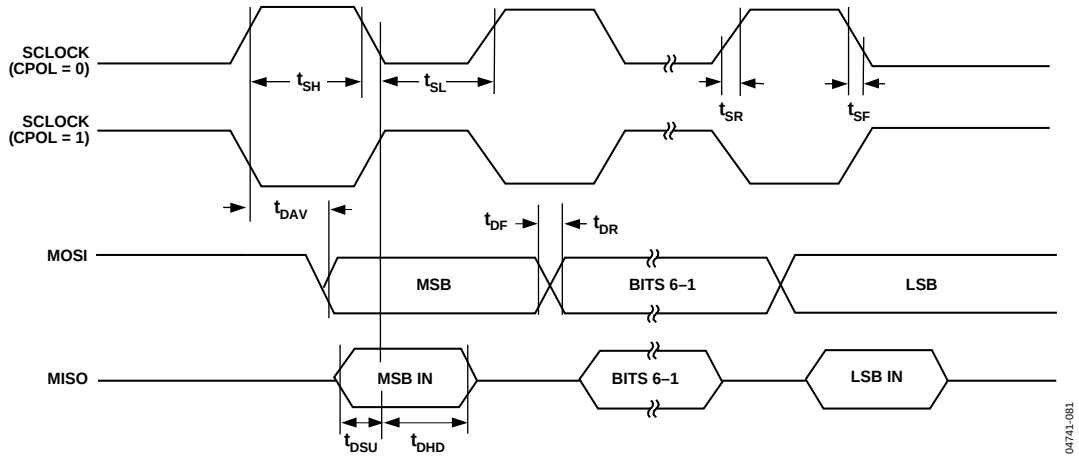

Figure 76. SPI Master Mode Timing (CHPA = 1)

Table 72. UART TIMING (SHIFT REGISTER MODE) Parameter

		12.58 MHz Core_Clk			Variable Core_Clk			
		Min	Typ	Max	Min	Typ	Max	Unit
TXLXL	Serial Port Clock Cycle Time		954			$12t_{core}$		ns
TQVXH	Output Data Setup to Clock	662						ns
TDVXH	Input Data Setup to Clock	292						ns
TXHDX	Input Data Hold After Clock	0						ns
TXHQX	Output Data Hold After Clock	22						ns

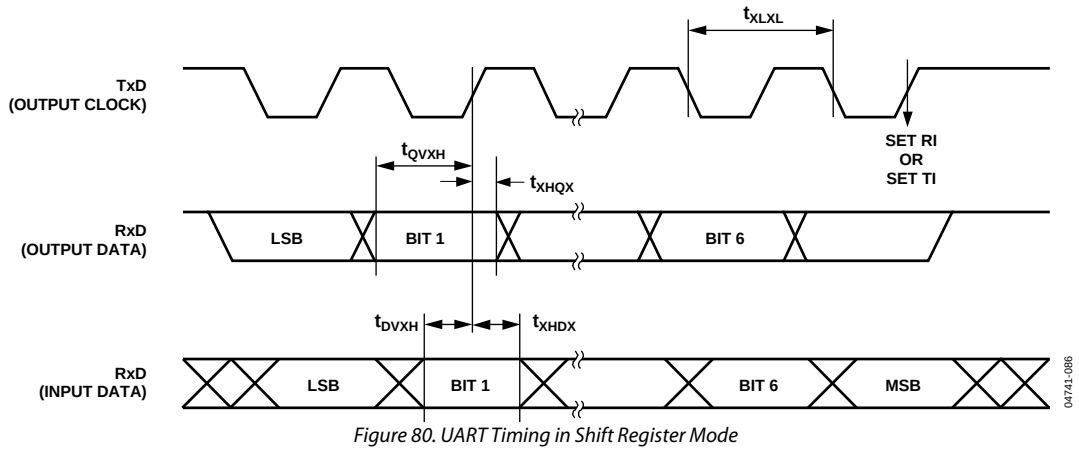

Figure 80. UART Timing in Shift Register Mode

NOTES