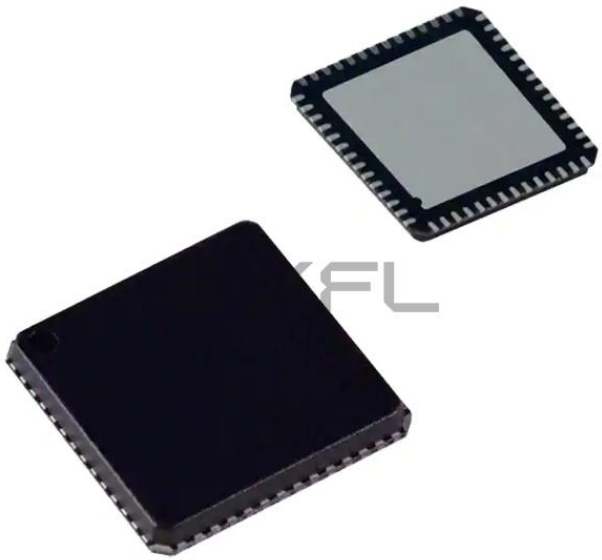

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc847bcpz62-5

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (ALL DIGITAL OUTPUTS EXCEPT XTAL2)					
V_{OH}, Output High Voltage[2]	2.4			V	DV_{DD} = 5 V, I_{SOURCE} = 80 µA
	2.4			V	DV_{DD} = 3 V, I_{SOURCE} = 20 µA
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 8 mA, SCLOCK, SDATA
			0.4	V	I_{SINK} = 1.6 mA on P0, P1, P2
Floating State Leakage Current[2]			±10	µA	
Floating State Output Capacitance		10		pF	
START-UP TIME					
At Power-On		600		ms	
After Ext RESET in Normal Mode		3		ms	
After WDT RESET in Normal Mode		2		ms	Controlled via WDCON SFR
From Power-Down Mode					
Oscillator Running					PLLCON.7 = 0
Wake-Up with $\overline{INT0}$ Interrupt		20		µs	
Wake-Up with SPI Interrupt		20		µs	
Wake-Up with TIC Interrupt		20		µs	
Oscillator Powered Down					PLLCON.7 = 1
Wake-Up with $\overline{INT0}$ Interrupt		30		µs	
Wake-Up with SPI Interrupt		30		µs	
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS					
Endurance[9]	100,000			Cycles	
Data Retention[10]	100			Years	
POWER REQUIREMENTS					
Power Supply Voltages					
AV_{DD} 3 V Nominal	2.7		3.6	V	
AV_{DD} 5 V Nominal	4.75		5.25	V	
DV_{DD} 3 V Nominal	2.7		3.6	V	
DV_{DD} 5 V Nominal	4.75		5.25	V	
5 V Power Consumption					4.75 V < DV_{DD} < 5.25 V, AV_{DD} = 5.25 V
Normal Mode[11, 12]					
DV_{DD} Current			10	mA	Core clock = 1.57 MHz
		25	31	mA	Core clock = 12.58 MHz
AV_{DD} Current			180	µA	
Power-Down Mode[11, 12]					
DV_{DD} Current		40	53	µA	T_{MAX} = 85°C; OSC on; TIC on
		50		µA	T_{MAX} = 125°C; OSC on; TIC on
		20	33	µA	T_{MAX} = 85°C; OSC off
		30		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off
Typical Additional Peripheral Currents (AI_{DD} and DI_{DD})					5 V V_{DD}, CD = 3
Primary ADC		1		mA	
Auxiliary ADC (ADuC845 Only)		0.5		mA	
Power Supply Monitor		30		µA	
DAC		60		µA	DACH/L = 000H
Dual Excitation Current Sources		200		µA	200 µA each. Can be combined to give 400 µA on a single output.
ALE Off		−20		µA	PCON.4 = 1 (see Table 6)
WDT		10		µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PWM					
–Fxtal		3		µA	
–Fvco		0.5		mA	
TIC		1		µA	
3 V Power Consumption					2.7 V < DV_{DD} < 3.6 V, AV_{DD} = 3.6 V
Normal Mode[11, 12]					
DV_{DD} Current			4.8	mA	Core clock = 1.57 MHz
		9	11	mA	Core clock = 6.29 MHz (CD = 1)
AV_{DD} Current			180	µA	ADC not enabled
Power-Down Mode[11, 12]					
DV_{DD} Current		20	26	µA	T_{MAX} = 85°C; OSC on; TIC on
		29		µA	T_{MAX} = 125°C; OSC on; TIC on
		14	20	µA	T_{MAX} = 85°C; OSC off
		21		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off

[1] Temperature range is for ADuC845BS; for the ADuC847BS and ADuC848BS (MQFP package), the range is –40°C to +125°C. Temperature range for ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) is –40°C to +85°C.
[2] These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[3] System zero-scale calibration can remove this error.
[4] Gain error drift is a span drift. To calculate full-scale error drift, add the offset error drift to the gain error drift times the full-scale input.
[5] In general terms, the bipolar input voltage range to the primary ADC is given by the ADC range = ±(V_{REF} 2^{RN})/1.25, where: V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected. RN = decimal equivalent of RN2, RN1, RN0. For example, if V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0, respectively, then the ADC range = ±1.28 V. In unipolar mode, the effective range is 0 V to 1.28 V in this example.
[6] 1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0/XREF1 or AXREF bits in ADC0CON2 and ADC1CON, respectively. (AXREF is available only on the ADuC845.)
[7] In bipolar mode, the auxiliary ADC can be driven only to a minimum of AGND – 30 mV as indicated by the auxiliary ADC absolute AIN voltage limits. The bipolar range is still –V_{REF} to +V_{REF}.
[8] DAC linearity and ac specifications are calculated using a reduced code range of 48 to 4095, 0 V to V_{REF}, reduced code range of 100 to 3950, 0 V to V_{DD}.
[9] Endurance is qualified to 100 kcycle per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 kcycles.
[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.
[11] Power supply current consumption is measured in normal mode following the power-on sequence, and in power-down modes under the following conditions: Normal mode: reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, core executing internal software loop. Power-down mode: reset = 0.4 V, all P0 pins and P1.2 to P1.7 pins = 0.4 V. All other digital I/O pins are open circuit, core Clk changed via CD bits in PLLCON, PCON.1 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[12] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

General Notes about Specifications

- DAC gain error is a measure of the span error of the DAC.
- The ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) have been qualified and tested with the base of the LFCSP package floating. The base of the LFCSP package should be soldered to the board, but left floating electrically, to ensure good mechanical stability.
- Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

ADC CIRCUIT INFORMATION

The ADuC845 incorporates two 10-channel (8-channel on the MQFP package) 24-bit Σ-Δ ADCs, while the ADuC847 and ADuC848 each incorporate a single 10-channel (8-channel on the MQFP package) 24-bit and 16-bit Σ-Δ ADC.

Each device also includes an on-chip programmable gain amplifier and configurable buffering (neither is available on the auxiliary ADC on the ADuC845). The devices also incorporate digital filtering intended for measuring wide dynamic range and low frequency signals such as those in weigh-scale, strain-gage, pressure transducer, or temperature measurement applications.

The ADuC845/ADuC847/ADuC848 can be configured as four or five (MQFP/LFCSP package) fully-differential input channels or as eight or ten (MQFP/LFCSP package) pseudo differential input channels referenced to AINCOM. The ADC on each device (primary only on the ADuC845) can be fully buffered internally, and can be programmed for one of eight input ranges from ±20 mV to ±2.56 V (V_{REF} × 1.024). Buffering the input channel means that the device can handle significant source impedances on the selected analog input and that RC filtering (for noise rejection or RFI reduction) can be placed on the analog inputs. If the ADC is used with internal buffering disabled (ADC0CON1.7 = 1, ADC0CON1.6 = 0), these unbuffered inputs provide a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the inputs can cause dc gain errors, depending on the output impedance of the source that is driving the ADC inputs.

Table 8 and Table 9 show the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 16-bit and 20-bit levels, respectively, is introduced. When used with internal buffering enabled, it is recommended that a capacitor (10 nF to 100 nF) be placed on the input to the ADC (usually as part of an antialiasing filter) to aid in noise performance.

The input channels are intended to convert signals directly from sensors without the need for external signal conditioning. With internal buffering disabled (relevant bits set/cleared in ADC0CON1), external buffering might be required.

When the internal buffer is enabled, it might be necessary to offset the negative input channel by +100 mV and to offset the positive channel by −100 mV if the reference range is AV_{DD}. This accounts for the restricted common-mode input range in the buffer. Some circuits, for example, bridge circuits, are inherently suitable to use without having to offset where the output voltage is balanced around $V_{REF}/2$ and is not sufficiently large to encroach on the supply rails. Internal buffering is not available on the auxiliary ADC (ADuC845 only). The auxiliary ADC (ADuC845 only) is fixed at a gain range of ±2.50 V.

The ADCs use a Σ-Δ conversion technique to realize up to 24 bits on the ADuC845 and the ADuC847, and up to 16 bits on the ADuC848 of no missing codes performance (20 Hz update rate, chop enabled). The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A $sinc^3$ programmable low-pass filter (see Table 28) is then used to decimate the modulator output data stream to give a valid data conversion result at programmable output rates. The signal chain has two modes of operation, chop enabled and chop disabled. The $\overline{CHOP}$ bit in the ADCMODE register enables or disables the chopping scheme.

Table 8. Maximum Resistance for No 16-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	111.3 kΩ	27.8 kΩ	16.7 kΩ	4.5 kΩ	2.58 kΩ	700 Ω
2	53.7 kΩ	13.5 kΩ	8.1 kΩ	2.2 kΩ	1.26 kΩ	360 Ω
4	25.4 kΩ	6.4 kΩ	3.9 kΩ	1.0 kΩ	600 Ω	170 Ω
8–128	10.7 kΩ	2.9 kΩ	1.7 kΩ	480 Ω	270 Ω	75 Ω

Table 9. Maximum Resistance for No 20-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	84.9 kΩ	21.1 kΩ	12.5 kΩ	3.2 kΩ	1.77 kΩ	440 Ω
2	42.0 kΩ	10.4 kΩ	6.1 kΩ	1.6 kΩ	880 Ω	220 Ω
4	20.5 kΩ	5.0 kΩ	2.9 kΩ	790 Ω	430 Ω	110 Ω
8–128	8.8 kΩ	2.3 k Ω	1.3 k Ω	370 Ω	195 Ω	50 Ω

ADC Noise Performance with Chop Disabled ($\overline{CHOP}$ = 1)

Table 14 through Table 17 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. Note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution. Typically, the performance of the ADC with chop disabled shows a 0.5 LSB degradation over the performance with chop enabled.

Table 14. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
68	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 15. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	17	17	17.5	18
82	49.95	13	14	15	16	16.5	17.5	18	18
255	16.06	13.5	14.5	15.5	16.5	17.5	18.5	18.5	19

Table 16. ADuC848 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
69	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 17. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320mV	±640mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	16	16	16	16
82	49.95	13	14	15	16	16	16	16	16
255	16.06	13.5	14.5	15.5	16	16	16	16	16

ADCSTAT (ADC STATUS REGISTER)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including REFIN± reference detect and conversion overflow/underflow flags.

SFR Address: D8H
Power-On Default: 00H
Bit Addressable: Yes

Table 23. ADCSTAT SFR Bit Designation

Bit No.	Name	Description
7	RDY0	Ready Bit for the Primary ADC. Set by hardware on completion of conversion or calibration. Cleared directly by the user, or indirectly by a write to the mode bits, to start calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary (ADuC845 only) ADC. Same definition as RDY0 referred to the auxiliary ADC. Valid on the ADuC845 only.
5	CAL	Calibration Status Bit. Set by hardware on completion of calibration. Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration. Note that calibration with the temperature sensor selected (auxiliary ADC on the ADuC845 only) fails to complete.
4	NOXREF	No External Reference Bit (only active if primary or auxiliary (ADuC845 only) ADC is active). Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When set, conversion results are clamped to all 1s. Only detects invalid REFIN±, does not check REFIN2±. Cleared to indicate valid V_{REF}.
3	ERR0	Primary ADC Error Bit. Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC. Valid on the ADuC845 only.
1	–––	Not Implemented. Write Don't Care.
0	–––	Not Implemented. Write Don't Care.

ADCMODE (ADC MODE REGISTER)

Used to control the operational mode of both ADCs.

SFR Address: D1H
Power-On Default: 08H
Bit Addressable: No

Table 24. ADCMODE SFR Bit Designations

Bit No.	Name	Description
7	---	Not Implemented. Write Don't Care.
6	REJ60	Automatic 60 Hz Notch Select Bit. Setting this bit places a notch in the frequency response at 60 Hz, allowing simultaneous 50 Hz and 60 Hz rejection at an SF word of 82 decimal. This 60 Hz notch can be set only if SF ≥68 decimal, that is, the regular filter notch must be ≤60 Hz. This second notch is placed at 60 Hz only if the device clock is at 32.768 kHz.
5	ADC0EN	Primary ADC Enable. Set by the user to enable the primary ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the primary ADC into power-down mode.
4	ADC1EN (ADuC845 only)	Auxiliary (ADuC845 only) ADC Enable. Set by the user to enable the auxiliary (ADuC845 only) ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the auxiliary (ADuC845 only) ADC in power-down mode.
3	$\overline{\text{CHOP}}$	Chop Mode Disable. Set by the user to disable chop mode on both the primary and auxiliary (ADuC845 only) ADC allowing a three times higher ADC data throughput. SF values as low as 3 are allowed with this bit set, giving up to 1.3 kHz ADC update rates. Cleared by the user to enable chop mode on both the primary and auxiliary (ADuC845 only) ADC.
2, 1, 0	MD2, MD1, MD0	Primary and Auxiliary (ADuC845 only) ADC Mode Bits. These bits select the operational mode of the enabled ADC as follows: MD2 MD1 MD0 0 0 0 ADC Power-Down Mode (Power-On Default). 0 0 1 Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided. 0 1 0 Single Conversion Mode. In single conversion mode, a single conversion is performed on the enabled ADC. Upon completion of a conversion, the ADC data registers (ADC0H/M/L and/or ADC1H/M/L (ADuC845 only)) are updated. The relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000. Note that ADC0L is not available on the ADuC848. 0 1 1 Continuous Conversion. In continuous conversion mode, the ADC data registers are regularly updated at the selected update rate (see the Sinc Filter SFR Bit Designations in Table 28). 1 0 0 Internal Zero-Scale Calibration. Internal short automatically connected to the enabled ADC input(s). 1 0 1 Internal Full-Scale Calibration. Internal or external REFIN± or REFIN2± V_{REF} (as determined by XREF bits in ADC0CON2 and/or AXREF (ADuC845 only) in ADC1CON (ADuC845 only) is automatically connected to the enabled ADC input(s) for this calibration. 1 1 0 System Zero-Scale Calibration. User should connect system zero-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers. 1 1 1 System Full-Scale Calibration. User should connect system full-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers.

ICON (EXCITATION CURRENT SOURCES CONTROL REGISTER)

The ICON register is used to configure the current sources and the burnout detection source.

SFR Address: D5H
Power-On Default: 00H
Bit Addressable: No

Table 30. Excitation Current Source SFR Bit Designations

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	ICON.6	Burnout Current Enable Bit. When set, this bit enables the sensor burnout current sources on primary ADC channels AIN5/AIN6 or AIN7/AIN8. Not available on any other ADC input pins or on the auxiliary ADC (ADuC845 only).
5	ICON.5	Not Implemented. Write Don't Care.
4	ICON.4	Not Implemented. Write Don't Care.
3	ICON.3	IEXC2 Pin Select. 0 selects AIN8, 1 selects AIN7
2	ICON.2	IEXC1 Pin Select. 0 selects AIN7, 1 selects AIN8
1	ICON.1	IEXC2 Enable Bit (0 = disable).
0	ICON.0	IEXC1 Enable Bit (0 = disable).

A write to the ICON register has an immediate effect but does not reset the ADCs. Therefore, if a current source is changed while an ADC is already converting, the user must wait until the third or fourth output at least (depending on the status of the chop mode) to see a fully settled new output.

Both IEXC1 and IEXC2 can be configured to operate on the same output pin thereby increasing the current source capability to 400 μA.

ON-CHIP PLL (PLLCON)

The ADuC845/ADuC847/ADuC848 are intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (384) of this to provide a stable 12.582912 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving when maximum core performance is not required. The default core clock is the PLL clock divided by 8 or 1.572864 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The control register for the PLL is called PLLCON and is described as follows.

The 5 V parts can be set to a maximum core frequency of 12.58 MHz (CD2...0 = 000) while at 3 V, the maximum core clock rate is 6.29 MHz (CD2...0 = 001). The CD bits should not be set to 000b on the 3 V parts.

The 3 V parts are limited to a core clock speed of 6.29 MHz (CD = 1).

PLLCON PLL Control Register

SFR Address: D7H
Power-On Default: 53H
Bit Addressable: No

Table 39. PLLCON PLL Control Register

Bit No.	Name	Description
7	OSC_PD	Oscillator Power-Down Bit. If low, the 32 kHz crystal oscillator continues running in power-down mode. If high, the 32.768 kHz oscillator is powered down. When this bit is low, the seconds counter continues to count in power-down mode and can interrupt the CPU to exit power-down. The oscillator is always enabled in normal mode.
6	LOCK	PLL Lock Bit. This is a read-only bit. Set automatically at power-on to indicate that the PLL loop is correctly tracking the crystal clock. After power-down, this bit can be polled to wait for the PLL to lock. Cleared automatically at power-on to indicate that the PLL is not correctly tracking the crystal clock. This might be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output can be 12.58 MHz ± 20%. After the device wakes up from power-down, user code can poll this bit to wait for the PLL to lock. If LOCK = 0, the PLL is not locked.
5	–––	Not Implemented. Write Don't Care.
4	LTEA	EA Status. Read-only bit. Reading this bit returns the state of the external $\overline{EA}$ pin latched at reset or power-on.
3	FINT	Fast Interrupt Response Bit. Set by the user to enable the response to any interrupt to be executed at the fastest core clock frequency. Cleared by the user to disable the fast interrupt response feature. This function must not be used on 3 V parts.
2, 1, 0	CD2, CD1, CD0	CPU (Core Clock) Divider Bits. This number determines the frequency at which the core operates. CD2 CD1 CD0 Core Clock Frequency (MHz) 0 0 0 12.582912. Not a valid selection on 3 V parts. 0 0 1 6.291456 (Maximum core clock rate allowed on the 3 V parts) 0 1 0 3.145728 0 1 1 1.572864 (Default core frequency) 1 0 0 0.786432 1 0 1 0.393216 1 1 0 0.196608 1 1 1 0.098304 On 3 V parts (ADuC84xBCPxx-3 or ADuC84xBSxx-3), the CD settings can be only CD = 1; CD = 0 is not a valid selection. If CD = 0 is selected on a 3 V part by writing to PLLCON, the instruction is ignored, and the previous CD value is retained. The Fast Interrupt bit (FINT) must not be used on 3 V parts since it automatically sets the CD bits to 0, which is not a valid setting.

I²C SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 support a fully licensed I²C serial interface. The I²C interface is implemented as a full hardware slave and software master. SDATA (Pin 27 on the MQFP package and Pin 29 on the LFCSP package) is the data I/O pin. SCLK (Pin 26 on the MQFP package and Pin 28 on the LFCSP package) is the serial interface clock for the SPI interface. The I²C interface on the devices is fully independent of all other pin/function multiplexing. The I²C interface incorporated on the ADuC845/ADuC847/ADuC848 also includes a second address register (I2CADD1) at SFR Address F2H with a default power-on value of 7FH. The I²C interface is always available to the user and is not multiplexed with any other I/O functionality on the chip. This means that the I²C and SPI interfaces can be used at the same time.

Note that when using the I²C and SPI interfaces simultaneously, they both use the same interrupt routine (Vector Address 3BH). When an interrupt occurs from one of these, it is necessary to interrogate each interface to see which one has triggered the ISR request.

The four SFRs that are used to control the I²C interface are described next.

I2CCON—I²C Control Register

SFR Address: E8H
Power-On Default: 00H
Bit Addressable: Yes

Table 40. I2CCON SFR Bit Designations

Bit No.	Name	Description
7	MDO	I²C Software Master Data Output Bit (master mode only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SDATA pin if the data output enable bit (MDE) is set.
6	MDE	I²C Software Output Enable Bit (master mode only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable the SDATA pin as an input (Rx).
5	MCO	I²C Software Master Clock Output Bit (master mode only). This bit is used to implement the SCLK for a master I²C transmitter in software. Data written to this bit is output on the SCLK pin.
4	MDI	I²C Software Master Data Input Bit (master mode only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on an SCLK transition if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (slave mode only). Set by the user to reset the I²C interface. Cleared by the user code for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (slave mode only). Set by the MicroConverter if the I²C interface is transmitting. Cleared by the MicroConverter if the I²C interface is receiving.
0	I2CI	I²C Interrupt Bit (slave mode only). Set by the MicroConverter after a byte has been transmitted or received. Cleared by the MicroConverter when the user code reads the I2CDAT SFR. I2CI should not be cleared by user code.

SPICON—SPI Control Register

SFR Address: F8H
Power-On Default: 05H
Bit Addressable: Yes

Table 41. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user code to enable SPI functionality. Cleared by user code to enable standard Port 2 functionality.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user code to enable master mode operation (SCLOCK is an output). Cleared by user code to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Bit. Set by user code to enable SCLOCK idle high. Cleared by user code to enable SCLOCK idle low.
2	CPHA[1]	Clock Phase Select Bit. Set by user code if the leading SCLOCK edge is to transmit data. Cleared by user code if the trailing SCLOCK edge is to transmit data.
1, 0	SPR1, SPR0	SPI Bit-Rate Bits. SPR1 SPR0 Selected Bit Rate 0 0 $f_{core}/2$ 0 1 $f_{core}/4$ 1 0 $f_{core}/8$ 1 1 $f_{core}/16$

[1] The CPOL and CPHA bits should both contain the same values for master and slave devices.

Note that both SPI and I²C use the same ISR (Vector Address 3BH); therefore, when using SPI and I²C simultaneously, it is necessary to check the interfaces following an interrupt to determine which one caused the interrupt.

SPIDAT: SPI Data Register

SFR Address: 7FH
Power-On Default: 00H
Bit Addressable: No

INTVAL—User Timer Interval Select Register

Function:	User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled.
SFR Address:	A6H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 255 decimal

HTHSEC—Hundredths of Seconds Time Register

Function:	This register is incremented in 1/128-second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address:	A2H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 127 decimal

SEC—Seconds Time Register

Function:	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address:	A3H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

MIN—Minutes Time Register

Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59 before rolling over to increment the HOUR time register.
SFR Address:	A4H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

HOUR—Hours Time Register

Function:	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. The HOUR SFR counts from 0 to 23 before rolling over to 0.
SFR Address:	A5H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 23 decimal

To enable the TIC as a real-time clock, the HOUR, MIN, SEC, and HTHSEC registers can be loaded with the current time. Once the TCEN bit is high, the TIC starts. To use the TIC as a time interval counter, select the count interval—hundredths of seconds, seconds, minutes, and hours via the ITS0 and ITS1 bits in the TIMECON SFR. Load the count required into the INTVAL SFR.

Note that INTVAL is only an 8-bit register, so user software must take into account any intervals longer than are possible with 8 bits. Therefore, to count an interval of 20 seconds, use the following procedure:

```
MOV TIMECON, #0D0H ;Enable 24Hour mode, count seconds, Clear TCEN.
MOV INTVAL,  #14H  ;Load INTVAL with required count interval...in this case 14H = 20
MOV TIMECON, #0D3H ;Start TIC counting and enable the 8bit INTVAL counter.
```

Timer/Counter 0 and 1 Operating Modes

This section describes the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 52 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

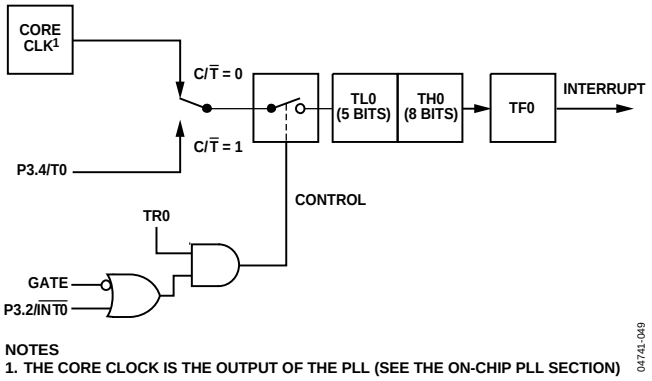

Figure 52. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 53.

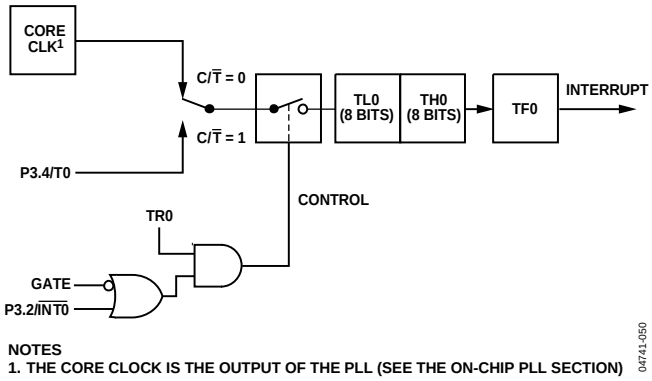

Figure 53. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload as shown in Figure 54. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

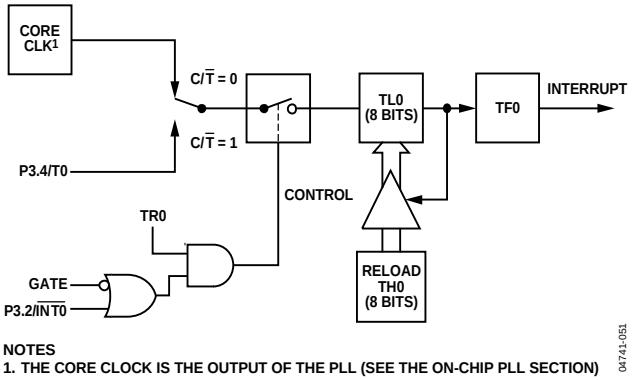

Figure 54. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 55. TL0 uses the Timer 0 Control Bits C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 then controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

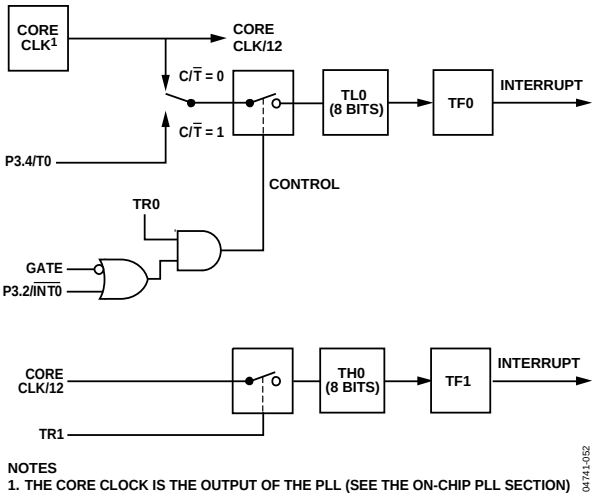

Figure 55. Timer/Counter 0, Mode 3

Mode 0 (8-Bit Shift Register Mode)

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The 8 bits are transmitted with the least significant bit (LSB) first.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line, and the clock pulses are output from the TxD line as shown in Figure 58.

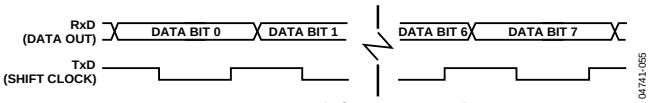

Figure 58. 8-Bit Shift Register Mode

Mode 1 (8-Bit UART, Variable Baud Rate)

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (0) and followed by a stop bit (1). Therefore, 10 bits are transmitted on TxD or are received on RxD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The write to SBUF signal also loads a 1 (stop bit) into the 9th bit position of the transmit shift register. The data is output bit-by-bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 59.

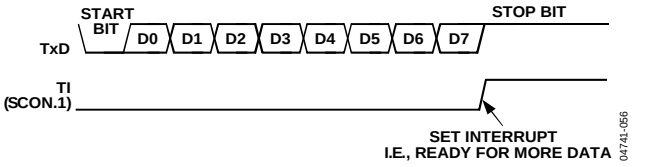

Figure 59. 8-Bit Variable Baud Rate

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming that a valid start bit is detected, character reception continues. The start bit is skipped and the 8 data bits are clocked into the serial port shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th bit (stop bit) is clocked into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is *not* met, the received frame is irretrievably lost, and RI is not set.

Mode 2 (9-Bit UART with Fixed Baud Rate)

Mode 2 is selected by setting SM0 and clearing SM1. In this mode, the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at Core_Clk/64 by default, although by setting the SMOD bit in PCON, the frequency can be doubled to Core_Clk/32. Eleven bits are transmitted or received: a start bit (0), 8 data bits, a programmable 9th bit, and a stop bit (1). The 9th bit is most often used as a parity bit, although it can be used for anything, including a ninth data bit if required.

To transmit, the 8 data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated, the 8 data bits (from SBUF) are loaded into the transmit shift register (LSB first). The contents of TB8 are loaded into the 9th bit position of the transmit shift register. The transmission starts at the next valid baud rate clock. The TI flag is set as soon as the stop bit appears on TxD.

Reception for Mode 2 is similar to that of Mode 1. The 8 data bytes are input at RxD (LSB first) and loaded onto the receive shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th data bit is latched into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

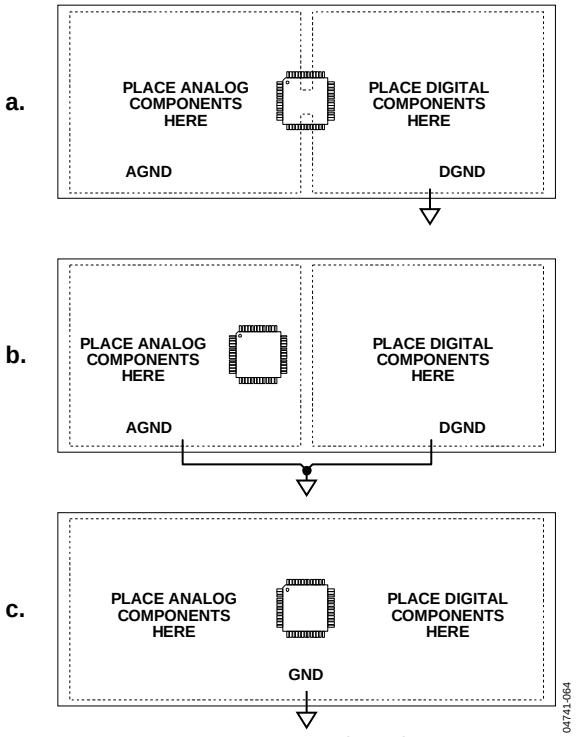

Figure 68. System Grounding Schemes

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the digital inputs of the ADuC845/ADuC847/ADuC848 add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the device. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the device and affecting the accuracy of ADC conversions.

When using the LFCSP package, it is recommended that the paddle underneath the chip be soldered to the board to provide maximum mechanical stability. However, it is recommended that this paddle not be grounded but left floating. All results and specifications contained in this data sheet are taken or recorded with the paddle floating.

System Self-Identification

In some hardware designs, it may be advantageous for the software to be able to identify the host MicroConverter.

The CHIPID SFR is a read-only register located at SFR address C2H. The upper nibble of this SFR designates the MicroConverter within the Σ-Δ ADC family. User software can read this SFR to identify the host MicroConverter and therefore execute slightly different code if required. The CHIPID SFR reads as follows for the Σ-Δ ADC family of MicroConverter products. Note that the ADuC845/ADuC847/ADuC848 are treated as one device as far as the CHIPID is concerned.

Table 63. CHIPID Values for Σ-Δ MicroConverter Products

Device	CHIPID
ADuC816	1xH
ADuC824	0xH
ADuC836	3xH
ADuC834	2xH
ADuC845/ADuC847/ADuC848	AxH

Clock Oscillator

As described earlier, the core clock frequency for the ADuC845/ADuC847/ADuC848 is generated from an on-chip PLL that locks onto a multiple (384 times) of 32.768 kHz. The latter is generated from an internal clock oscillator. To use the internal clock oscillator, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2 as shown in Figure 69.

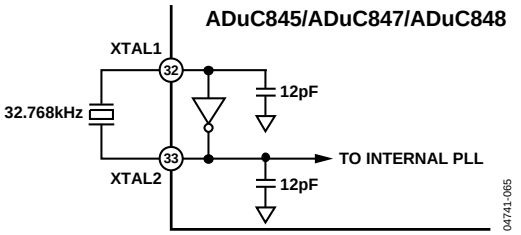

Figure 69. Crystal Connectivity to ADuC845/ADuC847/ADuC848

As shown in the typical external crystal connection diagram in Figure 69, two internal 12 pF capacitors are provided on-chip. These are connected internally, directly to the XTAL1 and XTAL2 pins. The total input capacitance at both pins is detailed in the Specifications table. Note that the total capacitance required for a particular crystal must be in accordance with the crystal manufacturer. However, in most cases, no additional external capacitance is required above that already supplied on-chip.

OTHER HARDWARE CONSIDERATIONS

In-Circuit Serial Download Access

Nearly all ADuC845/ADuC847/ADuC848 designs can take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the UART of the devices, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is shown in Figure 70 with a simple ADM3202-based circuit. If users would rather not include an RS-232 chip on the target board, refer to the uC006 Application Note, *A 4-Wire UART-to-PC Interface*, for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the device.

QuickStart DEVELOPMENT SYSTEM

The QuickStart Development System is an entry-level, low cost development tool suite supporting the ADuC8xx MicroConverter product family. The system consists of the following PC-based (Windows®-compatible) hardware and software development tools:

Hardware:	Evaluation board and serial port programming cable.
Software:	Serial download software.
Miscellaneous:	CD-ROM documentation and prototype evaluation board.

A brief description of some of the software tools and components in the QuickStart system follows.

Download—In-Circuit Serial Downloader

The serial downloader is a Windows application that allows the user to serially download an assembled program (Intel® hexa-decimal format file) to the on-chip program flash memory via the serial COM port on a standard PC. The AN-1074 Application Note details this serial download protocol.

ASPIRE—IDE

The ASPIRE® integrated development environment is a Windows application that allows the user to compile, edit, and debug code in the same environment. The ASPIRE software allows users to debug code execution on silicon using the MicroConverter UART serial port. The debugger provides access to all on-chip peripherals during a typical debug session as well as single-step, animate (automatic single stepping), and break-point code execution control.

Note that the ASPIRE IDE is also included as part of the QuickStart-PLUS system. As part of the QuickStart-PLUS system the ASPIRE IDE also supports mixed level and C source debugging. This is not available in the QuickStart system where the program is limited to assembly only.

QuickStart-PLUS DEVELOPMENT SYSTEM

The QuickStart-PLUS development system offers users enhanced nonintrusive debug and emulation tools. The system consists of the following PC-based (Windows-compatible) hardware and software development tools:

Hardware:	Prototype Board, Accutron NonIntrusive Single-Pin Emulator.
Software:	ASPIRE Integrated Development Environment. Features full C and Assembly emulation using the Accutron single-pin emulator.
Miscellaneous:	CD-ROM documentation.

Table 65. EXTERNAL DATA MEMORY READ CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{RLRH}	$\overline{RD}$ Pulse Width	60		125		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	145		290		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		48		100	ns
t_{RHDX}	Data and Address Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		150		625	ns
t_{LLDV}	ALE Low to Valid Data In		170		350	ns
t_{AVDV}	Address to Valid Data In		230		470	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	130		255		ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		15		35	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		120		ns

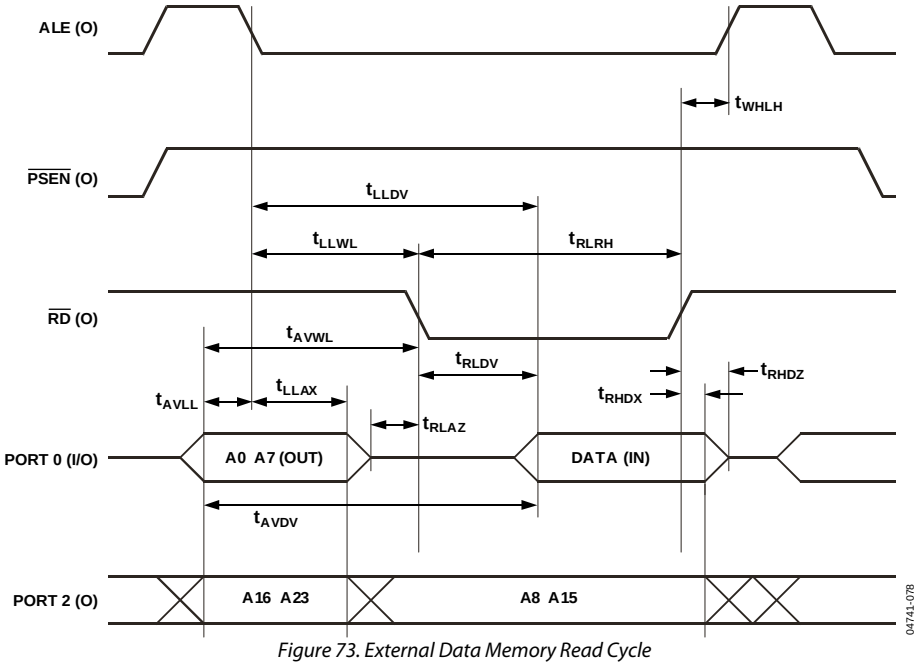

Figure 73. External Data Memory Read Cycle

Table 70. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

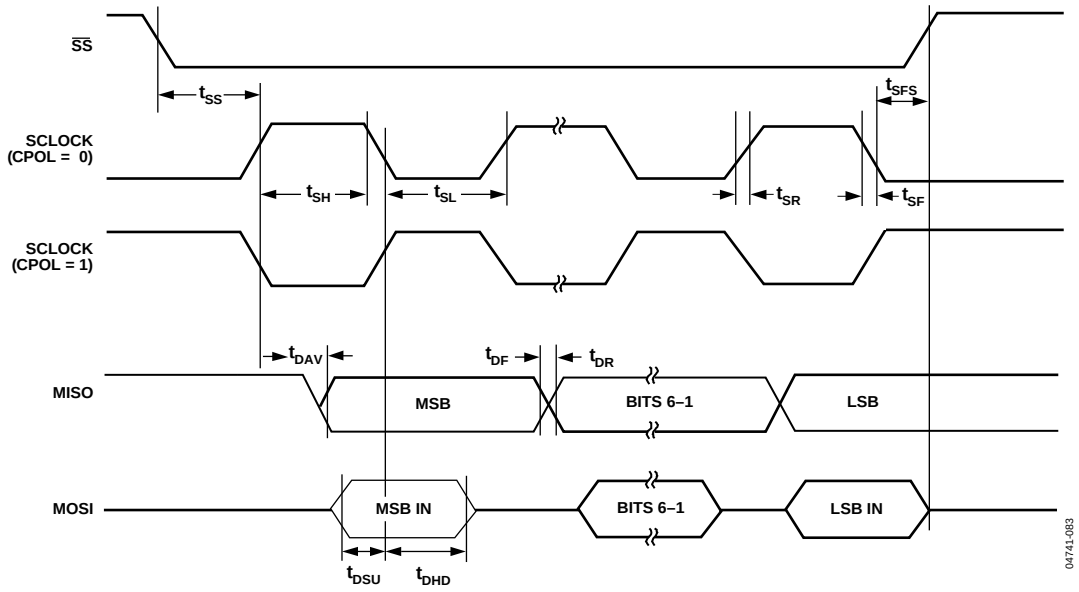

Figure 78. SPI Slave Mode Timing (CHPA = 1)

NOTES