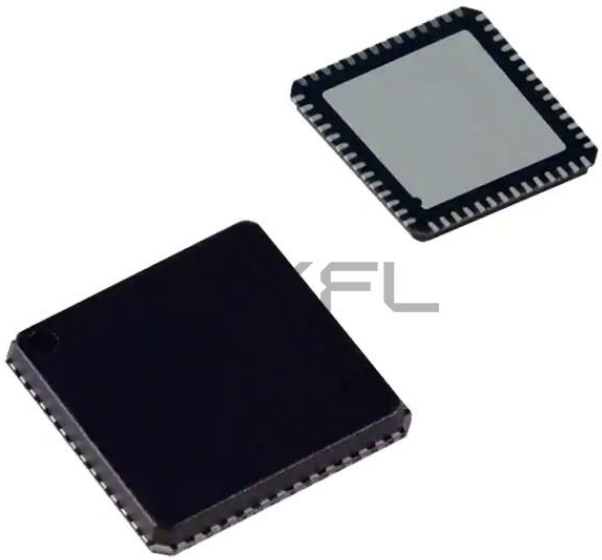

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc847bcpz8-3

REVISION HISTORY

5/2016—Rev. C to Rev. D

Changed uC004 to AN-1074 ..... Throughout
Updated Outline Dimensions 108
Changes to Ordering Guide 109

12/2012—Rev. B to Rev. C

Changes to Figure 3 and Table 3 11
Changes to Burnout Current Sources Section 32
Change to ADCMODE (ADC Mode Register) Section 42
Changes to Mode 4 (Dual NRZ 16-Bit Σ-Δ DAC) Section 58
Change to Hardware Slave Mode Section 63
Updated Outline Dimensions 104
Changes to Ordering Guide 105

2/2005—Rev. A to Rev. B

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Changes to the Excitation Currents Section 36
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Added 5 V Part Section 88
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6/2004—Rev. 0 to Rev. A

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Added SPIDAT: SPI Data Register Section 65
Changes to Table 42 67
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Changes to Timer/Counter 0 and 1 Data Registers Section 76
Changes to Table 54 80
Added the SBUF—UART Serial Port Data Register Section 80
Addition to the Timer 3 Generated Baud Rates Section 83
Added Table 57 and Renumbered Subsequent Tables 84
Changes to Table 61 86

4/2004—Revision 0: Initial Version

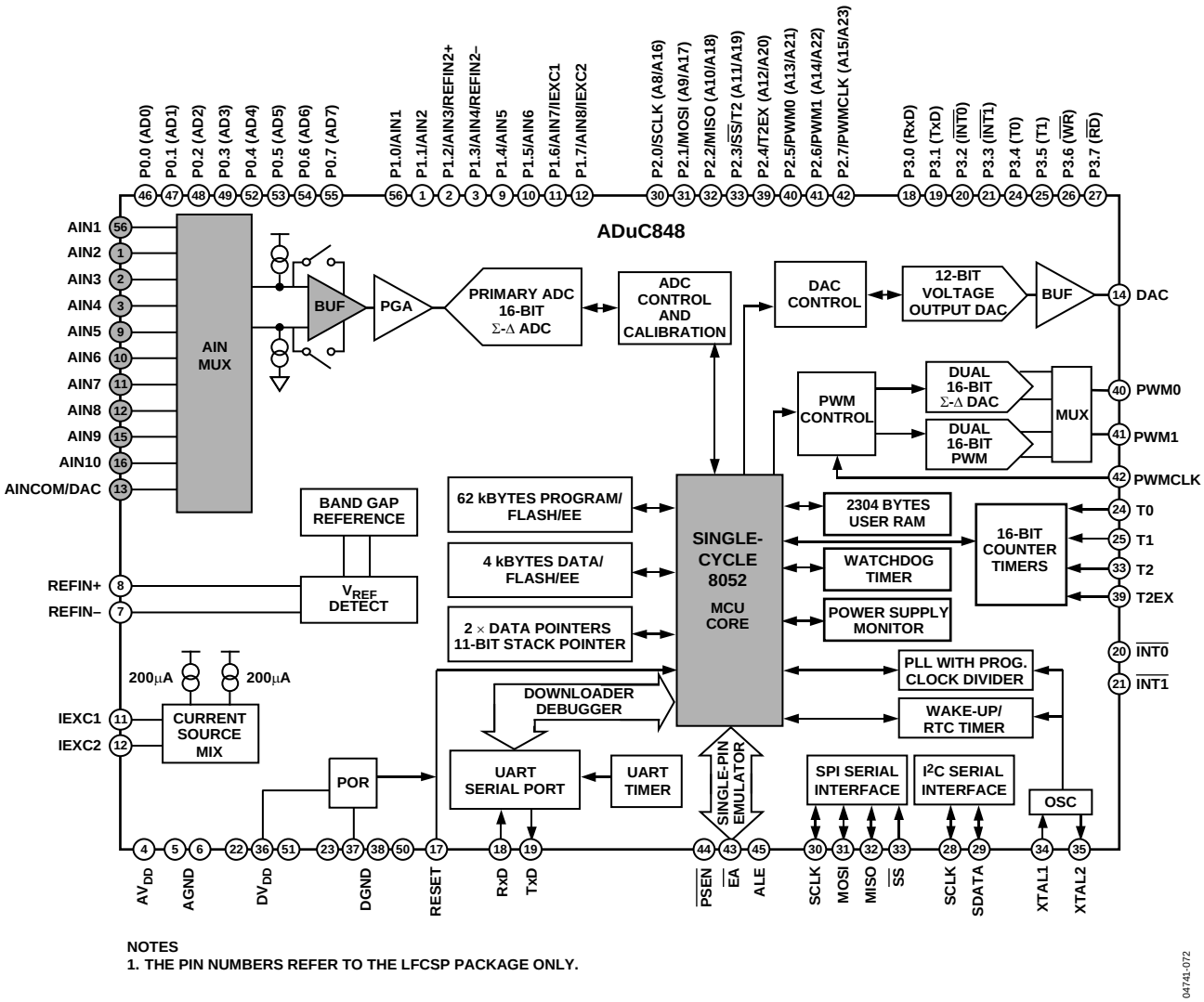

Figure 6. Detailed Block Diagram of the ADuC848

8052 INSTRUCTION SET

Table 4 documents the number of clock cycles required for each instruction. Most instructions are executed in one or two clock cycles resulting in 12.58 MIPs peak performance when operating at PLLCON = 00H.

TIMER OPERATION

Timers on a standard 8052 increment by one with each machine cycle. On the ADuC845, ADuC847, and ADuC848, one machine cycle is equal to one clock cycle; therefore, the timers increment at the same rate as the core clock.

ALE

On the ADuC834, the output on the ALE pin is a clock at 1/6th of the core operating frequency. On the ADuC845, ADuC847, and ADuC848, the ALE pin operates as follows. For a single machine cycle instruction, ALE is high for the entire machine cycle. For a two or more machine cycle instruction, ALE is high for the first machine cycle and then low for the remainder of the machine cycles.

EXTERNAL MEMORY ACCESS

The ADuC845, ADuC847, and ADuC848 do not support external program memory access, but the devices can access up to 16 MB (24 address bits) of external data memory. When accessing external RAM, the EWAIT register might need to be programmed to give extra machine cycles to MOVX commands to allow differing external RAM access speeds.

SPECIAL FUNCTION REGISTERS (SFRs)

The SFR space is mapped into the upper 128 bytes of internal data memory space and accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC845/ADuC847/ADuC848 via the SFR area is shown in Figure 11.

All registers except the program counter (PC) and the four general-purpose register banks reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

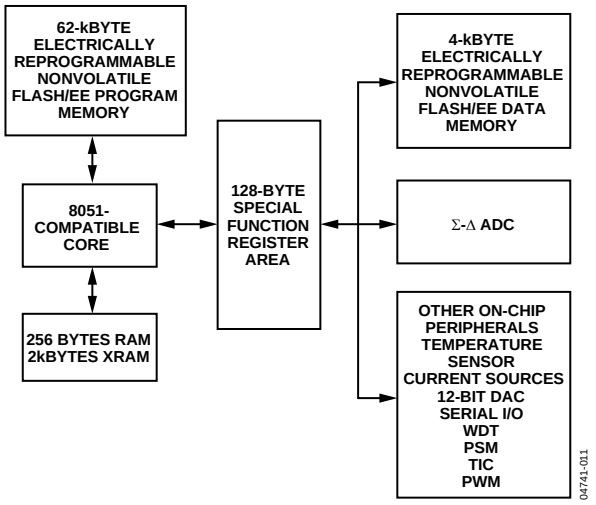

Figure 11. Programming Model

Accumulator SFR (ACC)

ACC is the accumulator register, which is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions usually refer to the accumulator as A.

B SFR (B)

The B register is used with the accumulator for multiplication and division operations. For other instructions, it can be treated as a general-purpose scratch pad register.

Data Pointer (DPTR)

The data pointer is made up of three 8-bit registers: DPP (page byte), DPH (high byte), and DPL (low byte). These provide memory addresses for internal code and data memory access. The DPTR can be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL).

The ADuC845/ADuC847/ADuC848 support dual data pointers. See the Dual Data Pointers section.

Stack Pointer (SP and SPH)

The SP SFR is the stack pointer, which is used to hold an internal RAM address called the *top of the stack*. The SP register is incremented before data is stored during PUSH and CALL executions. Although the stack can reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

As mentioned earlier, the devices offer an extended 11-bit stack pointer. The three extra bits needed to make up the 11-bit stack pointer are the three LSBs of the SPH byte located at B7H. To enable the SPH SFR, the EXSP (CFG84x.7) bit must be set; otherwise, the SPH SFR can be neither written to nor read from.

Program Status Word (PSW)

The PSW SFR contains several bits that reflect the current status of the CPU as listed in Table 5.

SFR Address: D0H
Power-On Default: 00H
Bit Addressable: Yes

Table 5. PSW SFR Bit Designations

Bit No.	Name	Description
7	CY	Carry Flag.
6	AC	Auxiliary Carry Flag.
5	F0	General-Purpose Flag.
4, 3	RS1, RS0	Register Bank Select Bits.
		RS1 RS0 Selected Bank
		0 0 0
		0 1 1
		1 0 2
		1 1 3
2	OV	Overflow Flag.
1	F1	General-Purpose Flag.
0	P	Parity Bit.

Signal Chain Overview with Chop Disabled ($\overline{CHOP}$ = 1)

With $\overline{CHOP}$ = 1, chop is disabled and the available output rates vary from 16.06 Hz to 1.365 kHz. The range of applicable SF words is from 3 to 255. When switching between channels with chop disabled, the channel throughput rate is higher than when chop is enabled. The drawback with chop disabled is that the drift performance is degraded and offset calibration is required following a gain range change or significant temperature change. A block diagram of the ADC input channel with chop disabled is shown in Figure 15.

The signal chain includes a multiplex or buffer, PGA, Σ-Δ modulator, and digital filter. The modulator bit stream is applied to a Sinc^3 filter. Programming the Sinc^3 decimation factor is restricted to an 8-bit register SF; the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) is therefore

$$f_{ADC} = \frac{1}{8 \times SF} \times f_{MOD}$$

where:
f_{ADC} is the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register, valid range is from 3 to 255.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The settling time to a step input is governed by the digital filter. A synchronized step change requires a settling time of three times the programmed update rate; a channel change can be treated as a synchronized step change. This is one conversion longer than the case for chop enabled. However, because the ADC throughput is three times faster with chop disabled than it is with chop enabled, the actual time to a settled ADC output is significantly less also. This means that following a synchronized step change, the ADC requires three conversions (note: data is not output following a synchronized ADC change until data has settled) before the result accurately reflects the new input voltage.

$$t_{SETTLE} = \frac{3}{f_{ADC}} = 3 \times t_{ADC}$$

An unsynchronized step change requires four conversions to accurately reflect the new analog input at its output. Note that with an unsynchronized change the ADC continues to output data and so the user must take unsettled outputs into account. Again, this is one conversion longer than with chop enabled, but because the ADC throughput with chop disabled is faster than with chop enabled, the actual time taken to obtain a settled ADC output is less.

The allowable range for SF is 3 to 255 with a default of 69 (45H). The corresponding conversion rates, rms, and peak-to-peak noise performances are shown in Table 14, Table 15, Table 16, and Table 17. Note that the conversion time increases by 0.244 ms for each increment in SF.

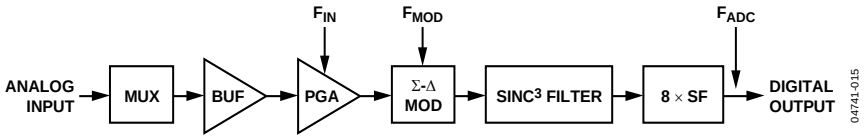

Figure 15. Block Diagram of ADC Input Channel with Chop Disabled

ADC Noise Performance with Chop Disabled ($\overline{CHOP}$ = 1)

Table 14 through Table 17 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. Note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution. Typically, the performance of the ADC with chop disabled shows a 0.5 LSB degradation over the performance with chop enabled.

Table 14. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
68	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 15. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	17	17	17.5	18
82	49.95	13	14	15	16	16.5	17.5	18	18
255	16.06	13.5	14.5	15.5	16.5	17.5	18.5	18.5	19

Table 16. ADuC848 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
69	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 17. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320mV	±640mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	16	16	16	16
82	49.95	13	14	15	16	16	16	16	16
255	16.06	13.5	14.5	15.5	16	16	16	16	16

(see Table 30). These burnout current sources are also available only with buffering enabled via the BUF0/BUF1 bits in the ADC0CON1 SFR. Once the burnout currents are turned on, a current flows in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. When the resulting voltage measured is full scale, the transducer has gone open circuit. When the voltage measured is 0 V, this indicates that the transducer has gone short circuit. The current sources work over the normal absolute input voltage range specifications.

REFERENCE DETECT CIRCUIT

The main and auxiliary (ADuC845 only) ADCs can be configured to allow the use of the internal band gap reference or an external reference that is applied to the REFIN± pins by means of the XREF0/1 bit in the Control Registers AD0CON2 and AD1CON (ADuC845 only). A reference detection circuit is provided to detect whether a valid voltage is applied to the REFIN± pins. This feature arose in connection with strain-gage sensors in weigh scales where the reference and signal are provided via a cable from the remote sensor. It is desirable to detect whether the cable is disconnected. If either of the pins is floating or if the applied voltage is below a specified threshold, a flag (NOXREF) is set in the ADC status register (ADCSTAT), conversion results are clamped, and calibration registers are not updated if a calibration is in progress.

Note that the reference detect does not look at REFIN2± pins.

If, during either an offset or gain calibration, the NOEXREF bit becomes active, indicating an incorrect V_{REF}, updating the relevant calibration register is inhibited to avoid loading incorrect data into these registers, and the appropriate bits in ADCSTAT (ERR0 or ERR1) are set. If the user needs to verify that a valid reference is in place every time a calibration is performed, the status of the ERR0 and ERR1 bits should be checked at the end of every calibration cycle.

SINC FILTER REGISTER (SF)

The number entered into the SF register sets the decimation factor of the Sinc^3 filter for the ADC. See Table 28 and Table 29.

The range of operation of the SF word depends on whether ADC chop is on or off. With chop disabled, the minimum SF word is 3 and the maximum is 255. This gives an ADC throughput rate from 16.06 Hz to 1.365 kHz. With chop enabled, the minimum SF word is 13 (all values lower than 13 are clamped to 13) and the maximum is 255. This gives an ADC throughput rate of 5.4 Hz to 105 Hz. See the f_{ADC} equation in the ADC description preceding section.

An additional feature of the Sinc^3 filter is a second notch filter positioned in the frequency response at 60 Hz. This gives simultaneous 60 Hz rejection to whatever notch is defined by the SF filter. This 60 Hz filter is enabled via the REJ60 bit in the ADCMODE register (ADCMODE.6). The notch is valid only for SF words ≥ 68; otherwise, ADC errors occur, and, the notch is best used with an SF word of 82d giving simultaneous 50 Hz and 60 Hz rejection. This function is useful only with an ADC clock (modulator rate) of 32.768 kHz. During calibration, the current (user-written) value of the SF register is used.

Σ-Δ MODULATOR

A Σ-Δ ADC usually consists of two main blocks, an analog modulator, and a digital filter. For the ADuC845/ADuC847/ADuC848, the analog modulator consists of a difference amplifier, an integrator block, a comparator, and a feedback DAC as shown in Figure 16.

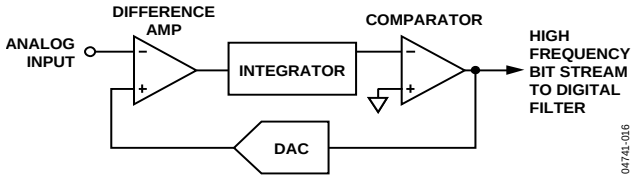

Figure 16. Σ-Δ Modulator Simplified Block Diagram

In operation, the analog signal is fed to the difference amplifier along with the output from the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output from the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data-word by using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (that results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency.

DIGITAL FILTER

The output of the ∑-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the device.

The ADuC845/ADuC847/ADuC848 filter is a low-pass, Sinc^3 or $[(SINx)/x]^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc filter) SFR as listed in Table 28 and Table 29.

Figure 22, Figure 23, Figure 24, and Figure 25 show the frequency response of the ADC, yielding an overall output rate of 16.6 Hz with chop enabled and 50 Hz with chop disabled. Also detailed in these plots is the effect of the fixed 60 Hz drop-in notch filter

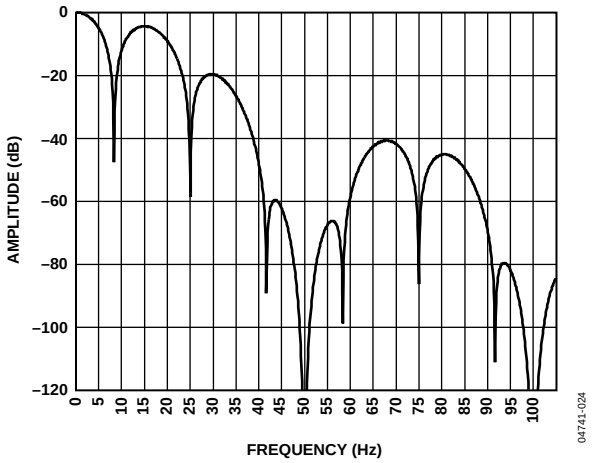

Figure 24. Chop On, Fadc = 16.6 Hz, SF = 52H

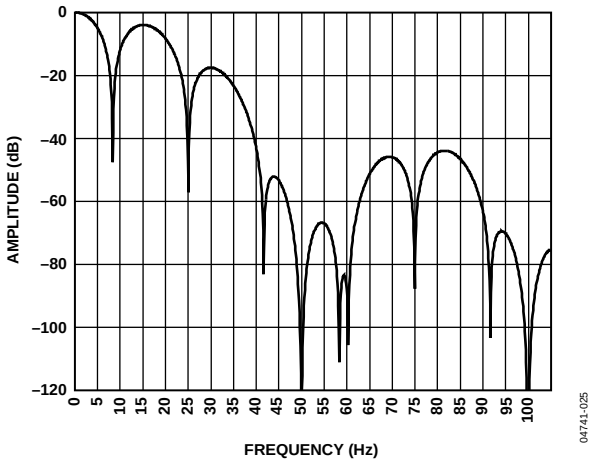

Figure 25. Chop On, Fadc = 16.6 Hz, SF = 52H, REJ60 Enabled

SF (ADC SINC FILTER CONTROL REGISTER)

The SF register is used to configure the decimation factor for the ADC, and therefore, has a direct influence on the ADC throughput rate.

SFR Address: D4H
Power-On Default: 45H
Bit Addressable: No

Table 28. Sinc Filter SFR Bit Designations

SF.7	SF.6	SF.5	SF.4	SF.3	SF.2	SF.1	SF.0
0	1	0	0	0	1	0	1

The bits in this register set the decimation factor of the ADC. This has a direct bearing on the throughput rate of the ADC along with the chop setting. The equations used to determine the ADC throughput rate are

$$Fadc\ (Chop\ On) = \frac{1}{3 \times 8 \times SFword} \times 32.768\ \text{kHz}$$

where *SFword* is in decimal.

$$Fadc\ (Chop\ Off) = \frac{1}{8 \times SFword} \times 32.768\ \text{kHz}$$

where *SFword* is in decimal.

Table 29. SF SFR Bit Examples

Chop Enabled (ADCMODE.3 = 0)

SF (Decimal)	SF (Hexadecimal)	Fadc (Hz)	Tadc (ms)	Tsettle (ms)
13[1]	0D	105.3	9.52	19.04
69	45	19.79	50.53	101.1
82	52	16.65	60.06	120.1
255	FF	5.35	186.77	373.54

Chop Disabled (ADCMODE.3 = 1)

SF (Decimal)	SF (Hexadecimal)	Fadc (Hz)	Tadc (ms)	Tsettle (ms)
3	03	1365.3	0.73	2.2
69	45	59.36	16.84	50.52
82	52	49.95	20.02	60.06
255	FF	16.06	62.25	186.8

[1] With chop enabled, if an SF word smaller than 13 is written to this SF register, the filter automatically defaults to 13.

During ADC calibration, the user-programmed value of SF word is used. The SF word does not default to the maximum setting (255) as it did on previous MicroConverter® products. However, for optimum calibration results, it is recommended that the maximum SF word be set.

USER DOWNLOAD MODE (ULOAD)

Figure 28 shows that it is possible to use the 62 kbytes of Flash/EE program memory available to the user as one single block of memory. In this mode, all the Flash/EE memory is read-only to user code.

However, most of the Flash/EE program memory can also be written to during run time simply by entering ULOAD mode. In ULOAD mode, the lower 56 kbytes of program memory can be erased and reprogrammed by the user software as shown in Figure 30. ULOAD mode can be used to upgrade the code in the field via any user-defined download protocol. By configuring the SPI port on the ADuC845/ADuC847/ADuC848 as a slave, it is possible to completely reprogram the 56 kbytes of Flash/EE program memory in under 5 s (see the AN-1074 Application Note).

Alternatively, ULOAD mode can be used to save data to the 56 kbytes of Flash/EE memory. This can be extremely useful in data logging applications where the devices can provide up to 60 kbytes of data memory on-chip (4 kbytes of dedicated Flash/EE data memory also exist).

The upper 6 kbytes of the 62 kbytes of Flash/EE program memory (8 kbytes on the 32-kbyte parts) are programmable only via serial download or parallel programming. This means that this space appears as read-only to user code; therefore, it cannot be accidentally erased or reprogrammed by erroneous code execution, making it very suitable to use the 6 kbytes as a bootloader. A bootload enable option exists in the Windows® serial downloader (WSD) to "Always RUN from E000H after Reset." If using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset.

Programming the Flash/EE program memory via ULOAD mode is described in the Flash/EE Memory Control SFR section of ECON and also in the AN-1074 Application Note.

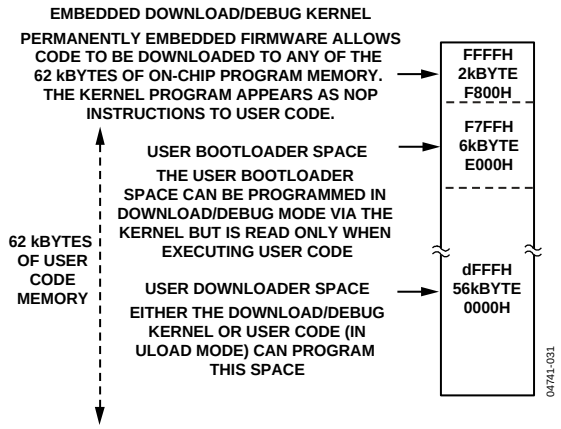

Figure 30. Flash/EE Program Memory Map in ULOAD Mode (62-kbyte Part)

The 32-kbyte memory parts have the user bootload space starting at 6000H. The memory mapping is shown in Figure 31.

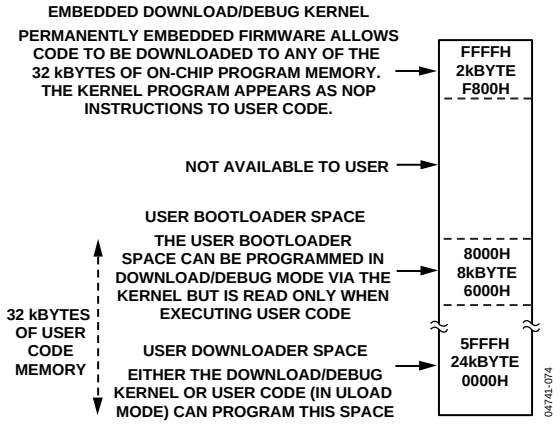

Figure 31. Flash/EE Program Memory Map in ULOAD Mode (32-kbyte Part)

ULOAD mode is not available on the 8-kbyte Flash/EE program memory parts.

Flash/EE Program Memory Security

The ADuC845/ADuC847/ADuC848 facilitate three modes of Flash/EE program memory security: the lock, secure, and serial safe modes. These modes can be independently activated, restricting access to the internal code space. They can be enabled as part of serial download protocol, as described in the AN-1074 Application Note, or via parallel programming.

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in parallel mode and reading the memory via a MOVC command from external memory are still allowed. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Secure Mode

This mode locks the code memory, disabling parallel programming of the program memory. Reading/verifying the memory in parallel mode and reading the internal memory via a MOVC command from external memory are also disabled. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the device into serial download mode, that is, RESET asserted (pulled high) and de-asserted (pulled low) with $\overline{\text{PSEN}}$ low, the device interprets the serial download reset as a normal reset only. It therefore does not enter serial download mode, but executes only a normal reset sequence. Serial safe mode can be disabled only by initiating an ERASE CODE AND DATA command in parallel programming mode.

I²C SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 support a fully licensed I²C serial interface. The I²C interface is implemented as a full hardware slave and software master. SDATA (Pin 27 on the MQFP package and Pin 29 on the LFCSP package) is the data I/O pin. SCLK (Pin 26 on the MQFP package and Pin 28 on the LFCSP package) is the serial interface clock for the SPI interface. The I²C interface on the devices is fully independent of all other pin/function multiplexing. The I²C interface incorporated on the ADuC845/ADuC847/ADuC848 also includes a second address register (I2CADD1) at SFR Address F2H with a default power-on value of 7FH. The I²C interface is always available to the user and is not multiplexed with any other I/O functionality on the chip. This means that the I²C and SPI interfaces can be used at the same time.

Note that when using the I²C and SPI interfaces simultaneously, they both use the same interrupt routine (Vector Address 3BH). When an interrupt occurs from one of these, it is necessary to interrogate each interface to see which one has triggered the ISR request.

The four SFRs that are used to control the I²C interface are described next.

I2CCON—I²C Control Register

SFR Address: E8H
Power-On Default: 00H
Bit Addressable: Yes

Table 40. I2CCON SFR Bit Designations

Bit No.	Name	Description
7	MDO	I²C Software Master Data Output Bit (master mode only). This data bit is used to implement a master I²C transmitter interface in software. Data written to this bit is output on the SDATA pin if the data output enable bit (MDE) is set.
6	MDE	I²C Software Output Enable Bit (master mode only). Set by the user to enable the SDATA pin as an output (Tx). Cleared by the user to enable the SDATA pin as an input (Rx).
5	MCO	I²C Software Master Clock Output Bit (master mode only). This bit is used to implement the SCLK for a master I²C transmitter in software. Data written to this bit is output on the SCLK pin.
4	MDI	I²C Software Master Data Input Bit (master mode only). This data bit is used to implement a master I²C receiver interface in software. Data on the SDATA pin is latched into this bit on an SCLK transition if the data output enable (MDE) bit is 0.
3	I2CM	I²C Master/Slave Mode Bit. Set by the user to enable I²C software master mode. Cleared by the user to enable I²C hardware slave mode.
2	I2CRS	I²C Reset Bit (slave mode only). Set by the user to reset the I²C interface. Cleared by the user code for normal I²C operation.
1	I2CTX	I²C Direction Transfer Bit (slave mode only). Set by the MicroConverter if the I²C interface is transmitting. Cleared by the MicroConverter if the I²C interface is receiving.
0	I2CI	I²C Interrupt Bit (slave mode only). Set by the MicroConverter after a byte has been transmitted or received. Cleared by the MicroConverter when the user code reads the I2CDAT SFR. I2CI should not be cleared by user code.

WATCHDOG TIMER

The watchdog timer generates a device reset or interrupt within a reasonable amount of time if the ADuC845/ADuC847/ADuC848 enters an erroneous state, possibly due to a programming error or electrical noise. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the WDE bit within a predetermined amount of time (see the PRE3…0 bits in Table 44). The watchdog timer is clocked from the 32 kHz external crystal connected between the XTAL1 and XTAL2 pins. The WDCOM SFR can be written only by user software if the double write sequence described in WDWR is initiated on every write access to the WDCON SFR.

WDCON—Watchdog Control Register

SFR Address: C0H
Power-On Default: 10H
Bit Addressable: Yes

Table 44. WDCON SFR Bit Designations

Bit No.	Name	Description
7, 6, 5, 4	PRE3, PRE2, PRE1, PRE0	Watchdog Timer Prescale Bits. The watchdog timeout period is given by the equation $t_{WD} = (2^{PRE} \times (2^9/ f_{XTAL}))$ $(0 \le PRE \le 7; f_{XTAL} = 32.768\ kHz)$

PRE3	PRE2	PRE1	PRE0	Timeout Period (ms)	Action
0	0	0	0	15.6	Reset or interrupt
0	0	0	1	31.2	Reset or interrupt
0	0	1	0	62.5	Reset or interrupt
0	0	1	1	125	Reset or interrupt
0	1	0	0	250	Reset or interrupt
0	1	0	1	500	Reset or interrupt
0	1	1	0	1000	Reset or interrupt
0	1	1	1	2000	Reset or interrupt
1	0	0	0	0.0	Immediate reset
PRE3–PRE0 > 1000b					Reserved. Not a valid selection.

3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period expires. This interrupt is not disabled by the CLR EA instruction, and it is also a fixed, high priority interrupt. If the watchdog timer is not being used to monitor the system, it can be used alternatively as a timer. The prescaler is used to set the timeout period in which an interrupt is generated.
2	WDS	Watchdog Status Bit. Set by the watchdog controller to indicate that a watchdog timeout has occurred. Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit. Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog timer generates a reset or interrupt, depending on WDIR. Cleared under the following conditions: user writes 0; watchdog reset (WDIR = 0); hardware reset; PSM interrupt.

0	WDWR	Watchdog Write Enable Bit.
		Writing data to the WDCON SFR involves a double instruction sequence. Global interrupts must first be disabled. The WDWR bit is set with the very next instruction, a write to the WDCON SFR. For example:
		`CLR EA ;Disable Interrupts while configuring to WDT`
		`SETB WDWR ;Allow Write to WDCON`
		`MOV WDCON, #72H ;Enable WDT for 2.0s timeout`
		`SETB EA ;Enable Interrupts again (if required)`

TIMECON—TIC Control Register

SFR Address: A1H
Power-On Default: 00H
Bit Addressable: No

Table 45. TIMECON SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	TFH	Twenty-Four Hour Select Bit. Set by the user to enable the hour counter to count from 0 to 23. Cleared by the user to enable the hour counter to count from 0 to 255.
5, 4	ITS1, ITS0	Interval Timebase Selection Bits. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	ST1	Single Time Interval Bit. Set by the user to generate a single interval timeout. If set, a timeout clears the TIEN bit. Cleared by the user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by user software.
1	TIEN	Time Interval Enable Bit. Set by the user to enable the 8-bit time interval counter. Cleared by the user to disable the interval counter.
0	TCEN	Time Clock Enable Bit. Set by the user to enable the time clock to the time interval counters. Cleared by the user to disable the clock to the time interval counters and reset the time interval SFRs to the last value written to them by the user. The time registers (HTHSEC, SEC, MIN, and HOUR) can be written while TCEN is low.

8052-COMPATIBLE ON-CHIP PERIPHERALS

This section gives a brief overview of the various secondary peripheral circuits that are available to the user on-chip. These features are mostly 8052-compatible (with a few additional features) and are controlled via standard 8052 SFR bit definitions.

Parallel I/O

The ADuC845/ADuC847/ADuC848 use four input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some are capable of external memory operations, while others are multiplexed with alternate functions for the peripheral functions available on-chip. In general, when a peripheral is enabled, that pin cannot be used as a general-purpose I/O pin.

Port 0

Port 0 is an 8-bit open-drain bidirectional I/O port that is directly controlled via the Port 0 SFR (80H). Port 0 is also the multiplexed low-order address and data bus during accesses to external data memory.

Figure 48 shows a typical bit latch and I/O buffer for a Port 0 pin. The bit latch (one bit in the SFRof the port) is represented as a Type D flip-flop, which clocks in a value from the internal bus in response to a write to latch signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a read latch signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a read pin signal from the CPU. Some instructions that read a port activate the read latch signal, and others activate the read pin signal. See the Read-Modify-Write Instructions section for details.

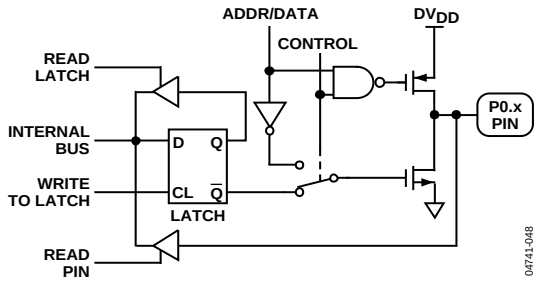

Figure 48. Port 0 Bit Latch and I/O Buffer

As shown in Figure 48, the output drivers of Port 0 pins are switchable to an internal ADDR and ADDR/DATA bus by an internal control signal for use in external memory accesses. During external memory accesses, the P0 SFR has 1s written to it; therefore, all its bit latches become 1. When accessing external memory, the control signal in Figure 48 goes high, enabling push-pull operation of the output pin from the internal address or data bus (ADDR/DATA line). Therefore, no external pull-ups are required on Port 0 for it to access external memory.

In general-purpose I/O port mode, Port 0 pins that have 1s written to them via the Port 0 SFR are configured as open-drain and, therefore, float. In this state, Port 0 pins can be used as high impedance inputs. This is represented in Figure 48 by the NAND gate whose output remains high as long as the control signal is low, thereby disabling the top FET. External pull-up resistors are, therefore, required when Port 0 pins are used as general-purpose outputs. Port 0 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 1.6 mA.

Port 1

Port 1 is also an 8-bit port directly controlled via the P1 SFR (90H). Port 1 digital output capability is not supported on this device. Port 1 pins can be configured as digital inputs or analog inputs. By (power-on) default, these pins are configured as analog inputs, that is, 1 is written to the corresponding Port 1 register bit. To configure any of these pins as digital inputs, the user should write a 0 to these port bits to configure the corresponding pin as a high impedance digital input. These pins also have various secondary functions aside from their analog input capability, as described in Table 46.

Table 46. Port 1 Alternate Functions

Pin No.	Alternate Function
P1.2	REFIN2+ (second reference input, postive)
P1.3	REFIN2− (second reference input, negative)
P1.6	IEXC1 (200 µA excitation current source)
P1.7	IEXC2 (200 µA excitation current source)

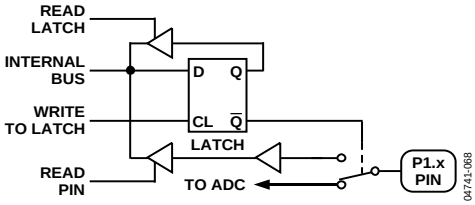

Figure 49. Port 1 Bit Latch and I/O Buffer

Port 2

Port 2 is a bidirectional port with internal pull-up resistors directly controlled via the P2 SFR. Port 2 also emits the middle- and high-order address bytes during accesses to the 24-bit external data memory space.

In general-purpose I/O port mode, Port 2 pins that have 1s written to them are pulled high by the internal pull-ups as shown in Figure 50 and, in that state, can be used as inputs. As inputs, Port 2 pins pulled externally low source current because of the internal pull-up resistors. Port 2 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 1.6 mA.

TCON—Timer/Counter 0 and 1 Control Register

SFR Address: 88H
Power-On Default: 00H
Bit Addressable: Yes

Table 51. TCON SFR Bit Designations

Bit No.	Name	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the program counter (PC) vectors to the interrupt service routine.
6	TR1	Timer 1 Run Control Bit. Set by the user to turn on Timer/Counter 1. Cleared by the user to turn off Timer/Counter 1.
5	TF0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	TR0	Timer 0 Run Control Bit. Set by the user to turn on Timer/Counter 0. Cleared by the user to turn off Timer/Counter 0.
3	IE1[1]	External Interrupt 1 ($\overline{INT1}$) Flag. Set by hardware by a falling edge or by a zero level applied to the external interrupt pin, $\overline{INT1}$, depending on the state of Bit IT1. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
2	IT1[1]	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.
1	IE0[1]	External Interrupt 0 ($\overline{INT0}$) Flag. Set by hardware by a falling edge or by a zero level being applied to the external interrupt pin, $\overline{INT0}$, depending on the statue of Bit IT0. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
0	IT0[1]	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.

[1] These bits are not used to control Timer/Counters 0 and 1, but are used instead to control and monitor the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Timer/Counter 0 and 1 Data Registers

Each timer consists of two 8-bit registers. These can be used as independent registers or combined into a single 16-bit register, depending on the timers' mode configuration.

TH0 and TL0—Timer 0 high and low bytes.
SFR Address: 8CH and 8AH, respectively.
Power-On Default: 00H and 00H, respectively.

TH1 and TL1—Timer 1 high and low bytes.
SFR Address: 8DH and 8BH, respectively.
Power-On Default: 00H and 00H, respectively.

Table 57. Common Baud Rates Using Timer 3 with a 12.58 MHz PLL Clock

Ideal Baud	CD	DIV	T3CON	T3FD	% Error
230400	0	1	81H	2DH	0.18
115200	0	2	82H	2DH	0.18
115200	1	1	81H	2DH	0.18
57600	0	3	83H	2DH	0.18
57600	1	2	82H	2DH	0.18
57600	2	1	81H	2DH	0.18
38400	0	4	84H	12H	0.12
38400	1	3	83H	12H	0.12
38400	2	2	82H	12H	0.12
38400	3	1	81H	12H	0.12
19200	0	5	85H	12H	0.12
19200	1	4	84H	12H	0.12
19200	2	3	83H	12H	0.12
19200	3	2	82H	12H	0.12
19200	4	1	81H	12H	0.12
9600	0	6	86H	12H	0.12
9600	1	5	85H	12H	0.12
9600	2	4	84H	12H	0.12
9600	3	3	83H	12H	0.12
9600	4	2	82H	12H	0.12
9600	5	1	81H	12H	0.12

as op amps and voltage reference) can be powered from the AV_{DD} supply line as well.

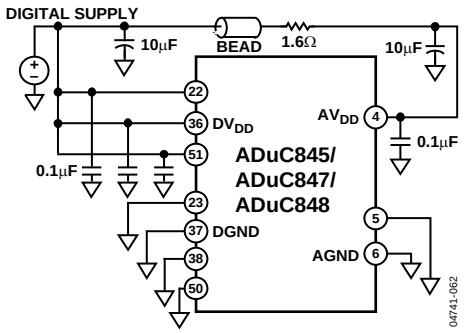

Figure 65. External Single-Supply Connections (56-Lead LFCSP Pin Numbering)

Notice that in both Figure 64 and Figure 65 a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local decoupling capacitors (0.1 µF) are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are closer than the 10 µF capacitors to each V_{DD} pin with lead lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that, at all times, the analog and digital ground pins on the device must be referenced to the same system ground reference point. It is recommended that the LFCSP paddle be soldered to ensure mechanical stability but be floated with respect to system V_{DD}s or grounds.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC845/ADuC847/ADuC848.

3 V Part

For DV_{DD} below 2.63 V, the internal POR holds the device in reset. As DV_{DD} rises above 2.63 V, an internal timer times out for typically 128 ms before the device is released from reset. The user must ensure that the power supply has at least reached a stable 2.7 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 66 illustrates the operation of the internal POR.

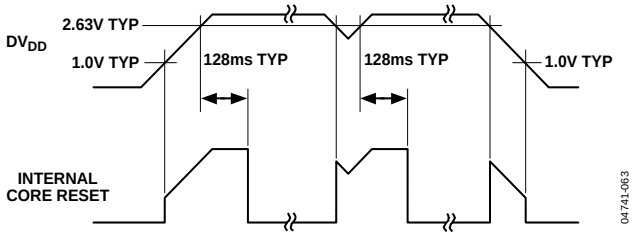

Figure 66. 3 V Part POR operation

5 V Part

For DV_{DD} below 4.5 V, the internal POR holds the device in reset. As DV_{DD} rises above 4.5 V, an internal timer times out for approximately 128 ms before the device is released from reset. The user must ensure that the power supply has reached a stable 4.75 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 67 illustrates this operation.

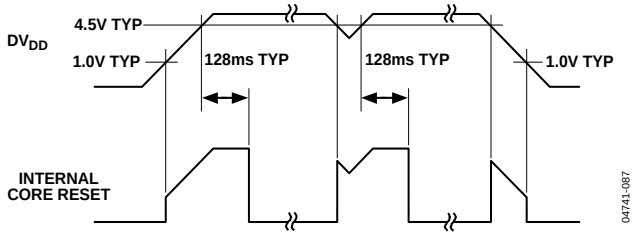

Figure 67. 5 V Part POR Operation

POWER CONSUMPTION

The DV_{DD} power supply current consumption is specified in normal and power-down modes. The AV_{DD} power supply current is specified with the analog peripherals disabled. The normal mode power consumption represents the current drawn from DV_{DD} by the digital core. The other on-chip peripherals (such as the watchdog timer and power supply monitor) consume negligible current and are therefore included with the normal operating current. The user must add any currents sourced by the parallel and serial I/O pins, and those sourced by the DAC to determine the total current needed at the ADuC845/ADuC847/ADuC848 DV_{DD} and AV_{DD} supply pins. Also, current drawn from the DV_{DD} supply increases by approximately 5 mA during Flash/EE erase and program cycles.

POWER-SAVING MODES

Setting the power-down mode bit, PCON.1, in the PCON SFR described in Table 6, allows the chip to be switched from normal mode into full power-down mode.

In power-down mode, both the PLL and the clock to the core are stopped. The on-chip oscillator can be halted or can continue to oscillate, depending on the state of the oscillator power-down bit (OSC_PD) in the PLLCON SFR. The TIC, driven directly from the oscillator, can also be enabled during power-down. However, all other on-chip peripherals are shut down. Port pins retain their logic levels in this mode, but the DAC output goes to a high impedance state (three-state) while ALE and $\overline{PSEN}$ outputs are held low. There are five ways to terminate power-down mode:

- **Asserting the RESET Pin**
  Returns to normal mode. All registers are set to their reset default value and program execution starts at the reset vector once the RESET pin is de-asserted.

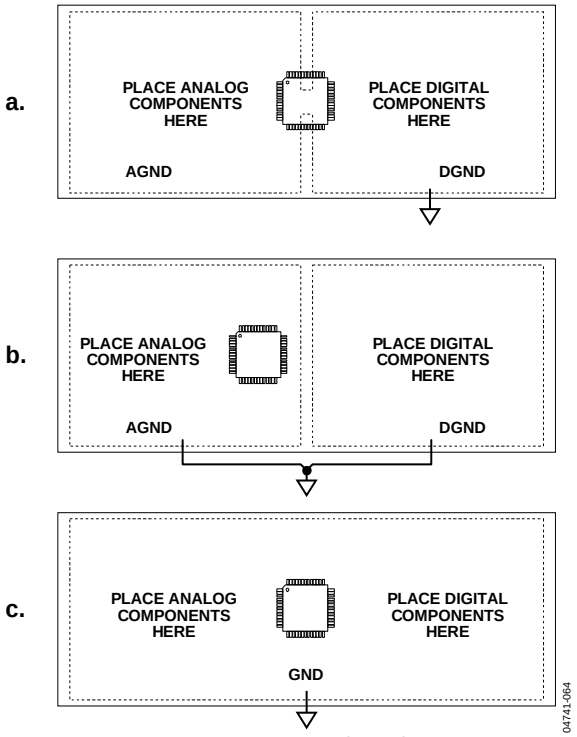

Figure 68. System Grounding Schemes

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the digital inputs of the ADuC845/ADuC847/ADuC848 add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the device. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the device and affecting the accuracy of ADC conversions.

When using the LFCSP package, it is recommended that the paddle underneath the chip be soldered to the board to provide maximum mechanical stability. However, it is recommended that this paddle not be grounded but left floating. All results and specifications contained in this data sheet are taken or recorded with the paddle floating.

System Self-Identification

In some hardware designs, it may be advantageous for the software to be able to identify the host MicroConverter.

The CHIPID SFR is a read-only register located at SFR address C2H. The upper nibble of this SFR designates the MicroConverter within the Σ-Δ ADC family. User software can read this SFR to identify the host MicroConverter and therefore execute slightly different code if required. The CHIPID SFR reads as follows for the Σ-Δ ADC family of MicroConverter products. Note that the ADuC845/ADuC847/ADuC848 are treated as one device as far as the CHIPID is concerned.

Table 63. CHIPID Values for Σ-Δ MicroConverter Products

Device	CHIPID
ADuC816	1xH
ADuC824	0xH
ADuC836	3xH
ADuC834	2xH
ADuC845/ADuC847/ADuC848	AxH

Clock Oscillator

As described earlier, the core clock frequency for the ADuC845/ADuC847/ADuC848 is generated from an on-chip PLL that locks onto a multiple (384 times) of 32.768 kHz. The latter is generated from an internal clock oscillator. To use the internal clock oscillator, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2 as shown in Figure 69.

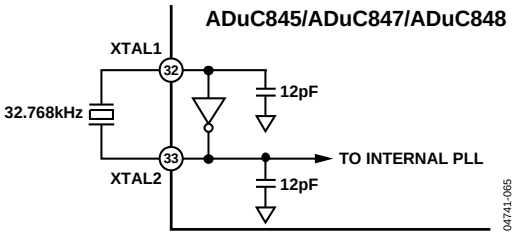

Figure 69. Crystal Connectivity to ADuC845/ADuC847/ADuC848

As shown in the typical external crystal connection diagram in Figure 69, two internal 12 pF capacitors are provided on-chip. These are connected internally, directly to the XTAL1 and XTAL2 pins. The total input capacitance at both pins is detailed in the Specifications table. Note that the total capacitance required for a particular crystal must be in accordance with the crystal manufacturer. However, in most cases, no additional external capacitance is required above that already supplied on-chip.

OTHER HARDWARE CONSIDERATIONS

In-Circuit Serial Download Access

Nearly all ADuC845/ADuC847/ADuC848 designs can take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the UART of the devices, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is shown in Figure 70 with a simple ADM3202-based circuit. If users would rather not include an RS-232 chip on the target board, refer to the uC006 Application Note, *A 4-Wire UART-to-PC Interface*, for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the device.

TIMING SPECIFICATIONS

AC inputs during testing are driven at DV_{DD} – 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements are made at V_{IH} min for Logic 1 and V_{IL} max for Logic 0 as shown in Figure 72.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 72.

C_{LOAD} for all outputs = 80 pF, unless otherwise noted.

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 64. CLOCK INPUT (External Clock Driven XTAL1) Parameter

		32.768 kHz External Crystal			
		Min	Typ	Max	Unit
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		6.26		µs
t_{CKH}	XTAL1 Width High		6.26		µs
t_{CKR}	XTAL1 Rise Time		9		ns
t_{CKF}	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	Core Clock Frequency[1]	0.098	1.57	12.58	MHz
t_{CORE}	Core Clock Period[2]		0.636		µs
t_{CYC}	Machine Cycle Time[3]	10.2	0.636	0.08	µs

[1] ADuC845/ADuC847/ADuC848 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 12.58 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[2] This number is measured at the default Core_Clk operating frequency of 1.57 MHz.
[3] ADuC845/ADuC847/ADuC848 machine cycle time is nominally defined as 1/Core_Clk.

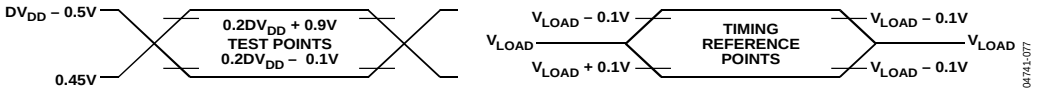

Figure 72. Timing Waveform Characteristics

Table 70. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

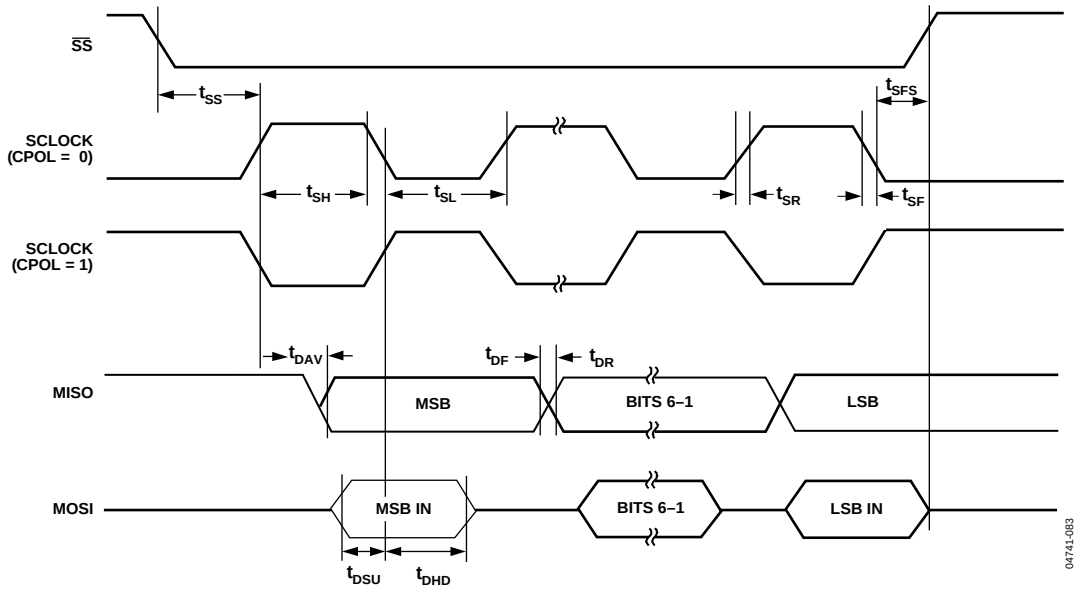

Figure 78. SPI Slave Mode Timing (CHPA = 1)

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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