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Details

Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc847bcpz8-5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Data Sheet

ADuC845/ADuC847/ADuC848

Parameter	Min	Тур	Max	Unit	Test Conditions/Comments
Normal Mode Rejection 50 Hz/60 Hz ²					
On AIN	75			dB	50 Hz/60 Hz \pm 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on
	67			dB	50 Hz/60 Hz \pm 1 Hz, 50 Hz Fadc, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz \pm 1 Hz, 50 Hz Fadc, SF = 52H, chop off
Analog Input Current ²			±1	nA	T _{MAX} = 85°C, buffer on
			±5	nA	T _{MAX} = 125°C, buffer on
Analog Input Current Drift		±5		pA/°C	T _{MAX} = 85°C, buffer on
2 .		±15		pA/°C	T _{MAX} = 125°C, buffer on
Average Input Current		±125		nA/V	±2.56 V range, buffer bypassed
Average Input Current Drift		±2		pA/V/°C	Buffer bypassed
Absolute AIN Voltage Limits ²	AGND +		AV _{DD} –	V	AIN1 AIN10 and AINCOM with buffer enabled
	0.1		0.1		
Absolute AIN Voltage Limits ²	A _{GND} – 0.03		AV _{DD} + 0.03	V	AIN1 AIN10 and AINCOM with buffer bypassed
EXTERNAL REFERENCE INPUTS					
REFIN(+) to REFIN(–) Voltage		2.5		V	REFIN refers to both REFIN and REFIN2
REFIN(+) to REFIN(–) Range ²	1		AVDD	V	REFIN refers to both REFIN and REFIN2
Average Reference Input Current		±1		μA/V	Both ADCs enabled
Average Reference Input Current Drift		±0.1		nA/V/°C	
NOXREF Trigger Voltage	0.3		0.65	V	NOXREF (ADCSTAT.4) bit active if $V_{REF} > 0.3$ V, and inactive if $V_{REF} > 0.65$ V
Common-Mode Rejection					
DC Rejection		125		dB	$AIN = 1 V$, range = $\pm 2.56 V$
50 Hz/60 Hz Rejection ²	90			dB	50 Hz/60 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 82
Normal Mode Rejection 50 Hz/60 Hz ²	75			dB	50 Hz/60 Hz \pm 1 Hz, AIN = 1 V, range = \pm 2.56 V, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, AlN = 1 V, range = ±2.56 V, SF = 52H, chop on
	67			dB	50 Hz/60 Hz \pm 1 Hz, AIN = 1 V, range = \pm 2.56 V, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz \pm 1 Hz, AlN = 1 V, range = \pm 2.56 V, SF = 52H, chop off
AUXILIARY ADC (ADuC845 Only)					
Conversion Rate	5.4		105	Hz	Chop on
	16.06		1365	Hz	Chop off
No Missing Codes ²	24			Bits	≤26.7 Hz update rate, chop enabled
	24			Bits	80.3 Hz update rate, chop disabled
Resolution	See Table	19 and Table 21			
Output Noise	See Table 1	8 and Table 20)		Output noise varies with selected update rates.
Integral Nonlinearity			±15	ppm of FSR	1 LSB ₁₆
Offset Error ³		±3		μV	Chop on
		±0.25		LSB ₁₆	Chop off
Offset Error Drift ²		10		nV/°C	Chop on
		200		nV/°C	Chop off
Full-Scale Error ⁴		±0.5		LSB ₁₆	
Gain Error Drift⁴		±0.5		ppm/°C	
Power Supply Rejection	80			dB	AIN = 1 V, range = ± 2.56 V, chop enabled
		80		dB	AIN = 1 V, range = ± 2.56 V, chop disabled

Signal Chain Overview (Chop Enabled, $\overline{CHOP} = 0$)

With the $\overline{\text{CHOP}}$ bit = 0 (see the ADCMODE SFR bit designations in Table 24), the chopping scheme is enabled. This is the default condition and gives optimum performance in terms of offset errors and drift performance. With chop enabled, the available output rates vary from 5.35 Hz to 105 Hz (SF = 255 and 13, respectively). A typical block diagram of the ADC input channel with chop enabled is shown in Figure 12.

The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency. The output of the Σ - Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band limited, low noise output from the ADCs.

The ADC filter is a low-pass $Sinc^3$ or $(sinx/x)^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the Sinc filter word loaded into the filter (SF) register (see Table 28). The complete signal chain is chopped, resulting in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important. With chop enabled, the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc³ filter, therefore, have a positive offset and a negative offset term included. As a result, a final summing stage is included so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data register. Programming the Sinc³ decimation factor is restricted to an 8-bit register called SF (see Table 28), the actual decimation factor is the register value times 8. Therefore, the decimated output rate from the Sinc³ filter (and the ADC conversion rate) is

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

where:

 f_{ADC} is the ADC conversion rate.

SF is the decimal equivalent of the word loaded to the filter register.

 f_{MOD} is the modulator sampling rate of 32.768 kHz.

The chop rate of the channel is half the output data rate:

$$f_{CHOP} = \frac{1}{2 \times f_{ADC}}$$

As shown in the block diagram (Figure 12), the Sinc³ filter outputs alternately contain $+V_{OS}$ and $-V_{OS}$, where V_{OS} is the respective channel offset.



Figure 12. Block Diagram of the ADC Input Channel with Chop Enabled

Data Sheet

(see Table 30). These burnout current sources are also available only with buffering enabled via the BUF0/BUF1 bits in the ADC0CON1 SFR. Once the burnout currents are turned on, a current flows in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. When the resulting voltage measured is full scale, the transducer has gone open circuit. When the voltage measured is 0 V, this indicates that the transducer has gone short circuit. The current sources work over the normal absolute input voltage range specifications.

REFERENCE DETECT CIRCUIT

The main and auxiliary (ADuC845 only) ADCs can be configured to allow the use of the internal band gap reference or an external reference that is applied to the REFIN \pm pins by means of the XREF0/1 bit in the Control Registers AD0CON2 and AD1CON (ADuC845 only). A reference detection circuit is provided to detect whether a valid voltage is applied to the REFIN \pm pins. This feature arose in connection with strain-gage sensors in weigh scales where the reference and signal are provided via a cable from the remote sensor. It is desirable to detect whether the cable is disconnected. If either of the pins is floating or if the applied voltage is below a specified threshold, a flag (NOXREF) is set in the ADC status register (ADCSTAT), conversion results are clamped, and calibration registers are not updated if a calibration is in progress.

Note that the reference detect does not look at REFIN2± pins.

If, during either an offset or gain calibration, the NOEXREF bit becomes active, indicating an incorrect V_{REF} , updating the relevant calibration register is inhibited to avoid loading incorrect data into these registers, and the appropriate bits in ADCSTAT (ERR0 or ERR1) are set. If the user needs to verify that a valid reference is in place every time a calibration is performed, the status of the ERR0 and ERR1 bits should be checked at the end of every calibration cycle.

SINC FILTER REGISTER (SF)

The number entered into the SF register sets the decimation factor of the Sinc³ filter for the ADC. See Table 28 and Table 29.

The range of operation of the SF word depends on whether ADC chop is on or off. With chop disabled, the minimum SF word is 3 and the maximum is 255. This gives an ADC throughput rate from 16.06 Hz to 1.365 kHz. With chop enabled, the minimum SF word is 13 (all values lower than 13 are clamped to 13) and the maximum is 255. This gives an ADC throughput rate of 5.4 Hz to 105 Hz. See the f_{ADC} equation in the ADC description preceding section.

An additional feature of the Sinc³ filter is a second notch filter positioned in the frequency response at 60 Hz. This gives simultaneous 60 Hz rejection to whatever notch is defined by the SF filter. This 60 Hz filter is enabled via the REJ60 bit in the ADCMODE register (ADCMODE.6). The notch is valid only for SF words \geq 68; otherwise, ADC errors occur, and, the notch is best used with an SF word of 82d giving simultaneous 50 Hz and 60 Hz rejection. This function is useful only with an ADC clock (modulator rate) of 32.768 kHz. During calibration, the current (user-written) value of the SF register is used.

Σ - Δ MODULATOR

A Σ - Δ ADC usually consists of two main blocks, an analog modulator, and a digital filter. For the ADuC845/ADuC847/ ADuC848, the analog modulator consists of a difference amplifier, an integrator block, a comparator, and a feedback DAC as shown in Figure 16.



Figure 16. Σ-Δ Modulator Simplified Block Diagram

In operation, the analog signal is fed to the difference amplifier along with the output from the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output from the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data-word by using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (that results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency.

DIGITAL FILTER

The output of the Σ - Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the device.

The ADuC845/ADuC847/ADuC848 filter is a low-pass, Sinc³ or [(SINx)/x]³ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc filter) SFR as listed in Table 28 and Table 29.

Figure 22, Figure 23, Figure 24, and Figure 25 show the frequency response of the ADC, yielding an overall output rate of 16.6 Hz with chop enabled and 50 Hz with chop disabled. Also detailed in these plots is the effect of the fixed 60 Hz drop-in notch filter

FUNCTIONAL DESCRIPTION

ADC SFR INTERFACE

The ADCs are controlled and configured via a number of SFRs that are mentioned here and described in more detail in the following sections.

Table 22. ADC SFR Interface

Name	Description
ADCSTAT	ADC Status Register. Holds the general status of the primary and auxiliary (ADuC845 only) ADCs.
ADCMODE	ADC Mode Register. Controls the general modes of operation for primary and auxiliary (ADuC845 only) ADCs.
ADC0CON1	Primary ADC Control Register 1. Controls the specific configuration of the primary ADC.
ADC0CON2	Primary ADC Control Register 2. Controls the specific configuration of the primary ADC.
ADC1CON	Auxiliary ADC Control Register. Controls the specific configuration of the auxiliary ADC. ADuC845 only.
SF	Sinc Filter Register. Configures the decimation factor for the Sinc ³ filter and, therefore, the primary and auxiliary (ADuC845 only) ADC update rates.
ICON	Current Source Control Register. Allows user control of the various on-chip current source options.
ADC0L/M/H	Primary ADC 24-bit (16-bit on the ADuC848) conversion result is held in these three 8-bit registers. ADC0L is not available on the ADuC848.
ADC1L/M/H	Auxiliary ADC 24-bit conversion result is held in these two 8-bit registers. ADuC845 only.
OF0L/M/H	Primary ADC 24-bit offset calibration coefficient is held in these three 8-bit registers. OF0L is not available on the ADuC848.
OF1L/H	Auxiliary ADC 16-bit offset calibration coefficient is held in these two 8-bit registers. ADuC845 only.
GN0L/M/H	Primary ADC 24-bit gain calibration coefficient is held in these three 8-bit registers. GN0L is not available on the ADuC848.
GN1L/H	Auxiliary ADC 16-bit gain calibration coefficient is held in these two 8-bit registers. ADuC845 only.

ADCSTAT (ADC STATUS REGISTER)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including REFIN± reference detect and conversion overflow/underflow flags.

SFR Address:	D8H
Power-On Default:	00H
Bit Addressable:	Yes

Bit No.	Name	Description
7	RDY0	Ready Bit for the Primary ADC.
		Set by hardware on completion of conversion or calibration.
		Cleared directly by the user, or indirectly by a write to the mode bits, to start calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary (ADuC845 only) ADC.
		Same definition as RDY0 referred to the auxiliary ADC. Valid on the ADuC845 only.
5	CAL	Calibration Status Bit.
		Set by hardware on completion of calibration.
		Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration.
		Note that calibration with the temperature sensor selected (auxiliary ADC on the ADuC845 only) fails to complete.
4	NOXREF	No External Reference Bit (only active if primary or auxiliary (ADuC845 only) ADC is active).
		Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When set, conversion results are clamped to all 1s. Only detects invalid REFIN±, does not check REFIN2±.
		Cleared to indicate valid V _{REF} .
3	ERRO	Primary ADC Error Bit.
		Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written.
		Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC. Valid on the ADuC845 only.
1		Not Implemented. Write Don't Care.
0		Not Implemented. Write Don't Care.

Table 23. ADCSTAT SFR Bit Designation

NONVOLATILE FLASH/EE MEMORY OVERVIEW

The ADuC845/ADuC847/ADuC848 incorporate Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable code and data memory space.

Like EEPROM, flash memory can be programmed in-system at the byte level, although it must first be erased, in page blocks. Thus, flash memory is often and more correctly referred to as Flash/EE memory.



Figure 26. Flash/EE Memory Development

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. The Flash/EE memory technology allows the user to update program code space incircuit, without needing to replace onetime programmable (OTP) devices at remote operating nodes.

Flash/EE Memory on the ADuC845, ADuC847, ADuC848

The ADuC845/ADuC847/ADuC848 provide two arrays of Flash/EE memory for user applications—up to 62 kbytes of Flash/EE program space and 4 kbytes of Flash/EE data memory space. Also, 8-kbyte and 32-kbyte program memory options are available. All examples and references in this datasheet use the 62-kbyte option; however, similar protocols and procedures are applicable to the 32-kbyte and 8-kbyte options unless otherwise noted, provided that the difference in memory size is taken into account.

The 62 kbytes Flash/EE code space are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed in-circuit, using the serial download mode provided, using conventional third party memory programmers, or via any user-defined protocol in user download (ULOAD) mode.

The 4-kbyte Flash/EE data memory space can be used as a general-purpose, nonvolatile scratchpad area. User access to this area is via a group of seven SFRs. This space can be programmed at a byte level, although it must first be erased in 4-byte pages.

All the following sections use the 62-kbyte program space as an example when referring to program and ULOAD mode. For the 64-kbyte part, the ULOAD area takes up the top 6 kbytes of the program space, that is, from 56 kbytes to 62 kbytes. For the 32-kbyte part, the ULOAD space moves to the top 8 kbytes of the on-chip program memory, that is., from 24 kbytes to 32 kbytes.

No ULOAD mode is available on the 8-kbyte part since the bootload area on the 8-kbyte part is 8 kbytes long, so no usable user program space remains. The kernel still resides in the protected area from 62 kbytes to 64 kbytes.

Flash/EE Memory Reliability

The Flash/EE program and data memory arrays on the ADuC845/ADuC847/ADuC848 are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events:

- 1. Initial page erase sequence
- 2. Read/verify sequence
- 3. Byte program sequence
- 4. Second read/verify sequence

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 00H to FFH until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications table, the ADuC845/ADuC847/ ADuC848 Flash/EE memory endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of – 40°C, +25°C, +85°C, and +125°C. (The LFCSP package is qualified to +85°C only.) The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention is the ability of the Flash/EE memory to retain its programmed data over time. Again, the devices have been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature ($T_1 = 55^{\circ}$ C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_1 as shown in Figure 27.



FLASH/EE PROGRAM MEMORY

The ADuC845/ADuC847/ADuC848 contain a 64-kbyte array of Flash/EE program memory. The lower 62 kbytes of this program memory are available to the user for program storage or as additional NV data memory.

The upper 2 kbytes of this Flash/EE program memory array contain permanently embedded firmware, allowing in-circuit serial download, serial debug, and nonintrusive single-pin emulation. These 2 kbytes of embedded firmware also contain a power-on configuration routine that downloads factory calibrated coefficients to the various calibrated peripherals such as ADC, temperature sensor, current sources, band gap, and references.

These 2 kbytes of embedded firmware are hidden from the user code. Attempts to read this space read 0s; therefore, the embedded firmware appears as NOP instructions to user code.

In normal operating mode (power-on default), the 62 kbytes of user Flash/EE program memory appear as a single block. This block is used to store the user code as shown in Figure 28.



In normal mode, the 62 kbytes of Flash/EE program memory

can be programmed by serial downloading and by parallel programming.

ADuC845/ADuC847/ADuC848

Serial Downloading (In-Circuit Programming)

The ADuC845/ADuC847/ADuC848 facilitate code download via the standard UART serial port. The devices enter serial download mode after a reset or a power cycle if the $\overline{\text{PSEN}}$ pin is pulled low through an external 1 k Ω resistor. Once in serial download mode, the hidden embedded download kernel executes. This allows the user to download code to the full 62 kbytes of Flash/EE program memory while the device is in circuit in its target application hardware.

A PC serial download executable (WSD.EXE) is provided as part of the ADuC845/ADuC847/ADuC848 Quick Start development system. The AN-1074 Application Note fully describes the serial download protocol that is used by the embedded download kernel.

Parallel Programming

The parallel programming mode is fully compatible with conventional third-party flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 29. In this mode, Ports 0 and 2 operate as the external address bus interface, P3 operates as the external data bus interface, and P1.0 operates as the write enable strobe. P1.1, P1.2, P1.3, and P1.4 are used as general configuration ports that configure the device for various program and erase operations during parallel programming.



The command words that are assigned to P1.1, P1.2, P1.3, and P1.4 are described in Table 31.

Table 31	. Flash/EE M	emory Parallel	Programming	Modes
----------	--------------	----------------	-------------	-------

					0 0
	Port 1 Pins				
	P1.4	P1.3	P1.2	P1.1	Programming Mode
-	0	0	0	0	Erase Flash/EE Program, Data, and Security Mode
	1	0	1	0	Program Code Byte
	0	0	1	0	Program Data Byte
	1	0	1	1	Read Code Byte
	0	0	1	1	Read Data Byte
	1	1	0	0	Program Security Modes
	1	1	0	1	Read/Verify Security Modes
	All oth	er code	S		Redundant
	1 0 1 0 1 1 All oth	0 0 0 1 1 ner code	1 1 1 0 0	0 0 1 1 0	Security Mode Program Code Byte Program Data Byte Read Code Byte Read Data Byte Program Security Modes Read/Verify Security Modes Redundant

Example: Programming the Flash/EE Data Memory

A user wants to program F3H into the second byte on Page 03H of the Flash/EE data memory space while preserving the other 3 bytes already in this page. A typical program of the Flash/EE data array involves

- 1. Setting EADRH/L with the page address.
- 2. Writing the data to be programmed to the EDATA1-4.
- 3. Writing the ECON SFR with the appropriate command.

Step 1: Set Up the Page Address

Address registers EADRH and EADRL hold the high byte address and the low byte address of the page to be addressed. The assembly language to set up the address may appear as

MOV EADRH, #0 ;Set Page Address Pointer MOV EADRL, #03H

Step 2: Set Up the EDATA Registers

Write the four values to be written into the page into the four SFRs EDATA1–4. Unfortunately, the user does not know three of them. Thus, the user must read the current page and overwrite the second byte.

MOV ECON, #1 ;Read Page into EDATA1-4 MOV EDATA2, #0F3H ;Overwrite Byte 2

Step 3: Program Page

A byte in the Flash/EE array can be programmed only if it has previously been erased. Specifically, a byte can be programmed only if it already holds the value FFH. Because of the Flash/EE architecture, this erasure must happen at a page level; therefore, a minimum of 4 bytes (1 page) are erased when an erase command is initiated. Once the page is erased, the user can program the 4 bytes in-page and then perform a verification of the data.

MOV	ECON, #5	;ERASE Page
MOV	ECON, #2	;WRITE Page
MOV	ECON, #4	;VERIFY Page
MOV	A, ECON	;Check if ECON = 0 (OK!)

Although the 4 kbytes of Flash/EE data memory are factory preerased, that is, byte locations set to FFH, it is good programming practice to include an ERASEALL routine as part of any configuration/set-up code running on the devices. An ERASEALL command consists of writing 06H to the ECON SFR, which initiates an erase of the 4-kbyte Flash/EE array. This command coded in 8051 assembly language would appear as

MOV ECON, #06H ;ERASE

;ERASE all Command ;2ms duration

FLASH/EE MEMORY TIMING

Typical program and erase times for the devices are as follows:

Normal Mode (Operating on Flash/EE Data Memory)

Command	Bytes Affected	
READPAGE	4 bytes	25 machine cycles
WRITEPAGE	4 bytes	380 µs
VERIFYPAGE	4 bytes	25 machine cycles
ERASEPAGE	4 bytes	2 ms
ERASEALL	4 kbytes	2 ms
READBYTE	1 byte	10 machine cycles
WRITEBYTE	1 byte	200 µs

ULOAD Mode (Operating on Flash/EE Program Memory)

WRITEPAGE	256 bytes	15 ms
ERASEPAGE	64 bytes	2 ms
ERASEALL	56 kbytes	2 ms
WRITEBYTE	1 byte	200 µs

A given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core microcontroller operation is idled until the requested program/read or erase mode is completed. In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two-machine-cycle MOV instruction (to write to the ECON SFR), the next instruction is not executed until the Flash/EE operation is complete. This means that the core cannot respond to interrupt requests until the Flash/EE operation is complete, although the core peripheral functions such as counter/timers continue to count as configured throughout this period.

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For larger loads, the current drive capability may not be sufficient. To increase the source and sink current capability of the DAC, an external buffer should be added as shown in Figure 37.



The internal DAC output buffer also features a high impedance disable function. In the chip's default power-on state, the DAC is disabled and its output is in a high impedance state (or threestate) where it remains inactive until enabled in software. This means that if a zero output is desired during power-on or power-down transient conditions, a pull-down resistor must be added to each DAC output. Assuming that this resistor is in place, the DAC output remains at ground potential whenever the DAC is disabled.

ADuC845/ADuC847/ADuC848

PULSE-WIDTH MODULATOR (PWM)

The ADuC845/ADuC847/ADuC848 has a highly flexible PWM offering programmable resolution and an input clock. The PWM can be configured in six different modes of operation. Two of these modes allow the PWM to be configured as a Σ - Δ DAC with up to 16 bits of resolution. A block diagram of the PWM is shown in Figure 38.



The PWM uses control SFR, PWMCON, and four data SFRs: PWM0H, PWM0L, PWM1H, and PWM1L.

PWMCON (as described in Table 34) controls the different modes of operation of the PWM as well as the PWM clock frequency. PWM0H/L and PWM1H/L are the data registers that determine the duty cycles of the PWM outputs at P2.5 and P2.6.

To use the PWM user software, first write to PWMCON to select the PWM mode of operation and the PWM input clock. Writing to PWMCON also resets the PWM counter. In any of the 16-bit modes of operation (Modes 1, 3, 4, 6), user software should write to the PWM0L or PWM1L SFRs first. This value is written to a hidden SFR. Writing to the PWM0H or PWM1H SFRs updates both the PWMxH and the PWMxL SFRs but does not change the outputs until the end of the PWM cycle in progress. The values written to these 16-bit registers are then used in the next PWM cycle.

SFR Address:	AEH
Power-On Default:	00H
Bit Addressable:	No

Table 34. PWMCON PWM Control SFR

Bit No.	Name	Description				
7		Not Implemented. Write Don't Care.				
6, 5, 4	PWM2, PWM1, PWM0	PMW Mode Selection.				
		PWM2	PWM1	PWM0		
		0	0	0	Mode 0:	PWM disabled.
		0	0	1	Mode 1:	Single 16-bit output with programmable pulse and cycle time.
		0	1	0	Mode 2:	Twin 8-bit outputs.
		0	1	1	Mode 3:	Twin 16-bit outputs.
		1	0	0	Mode 4:	Dual 16-bit pulse density outputs.
		1	0	1	Mode 5:	Dual 8-bit outputs.
		1	1	0	Mode 6:	Dual 16-bit pulse density RZ outputs.
		1	1	1	Mode 7:	PWM counter reset with outputs not used.
3, 2	PWS1, PWS0	PWM CI	ock Sourc	e Divider.		
		PWS1	PWS0			
		0	0	Selected	d clock.	
		0	1	Selected clock divided by 4.		
		1	0	Selected	d clock divid	ded by 16.
		1	1	Selected	d clock divid	ded by 64.
1, 0	PWC1, PWC0	PWM CI	ock Sourc	ce Selection.		
		PWC1	PWC0			
		0	0	Fxtal/15	(2.184 kHz)	
		0	1	F _{XTAL} (32	.768 kHz).	
		1	0	External	input on P	2.7.
		1	1	Fvco (12.	58 MHz).	

PWM Pulse Width High Byte (PWM0H)

SFR Address:	B2H
Power-On Default:	00H
Bit Addressable:	No

Table 35. PWM0H: PWM Pulse Width High Byte

PWM0H.7	PWM0H.6	PWM0H.5	PWM0H.4	PWM0H.3	PWM0H.2	PWM0H.1	PWM0H.0
0	0	0	0	0	0	0	0
R/W							

PWM Pulse Width Low Byte (PWM0L)

SFR Address:	B1H
Power-On Default:	00H
Bit Addressable:	No

ON-CHIP PLL (PLLCON)

The ADuC845/ADuC847/ADuC848 are intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (384) of this to provide a stable 12.582912 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving when maximum core performance is not required. The default core clock is the PLL clock divided by 8 or 1.572864 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The control register for the PLL is called PLLCON and is described as follows.

The 5 V parts can be set to a maximum core frequency of 12.58 MHz (CD2...0 = 000) while at 3 V, the maximum core clock rate is 6.29 MHz (CD2...0 = 001). The CD bits should not be set to 000b on the 3 V parts.

The 3 V parts are limited to a core clock speed of 6.29 MHz (CD = 1).

PLLCON PLL Control Register

SFR Address:	D7H
Power-On Default:	53H
Bit Addressable:	No

Table 39. PLLCON PLL Control Register

Bit No.	Name	Descr	iption		
7	OSC_PD	Oscilla	ntor Power-D	own Bit.	
		If low,	the 32 kHz o	rystal oscillate	or continues running in power-down mode.
		lf high	, the 32.768	kHz oscillator	is powered down.
		When to exit	this bit is lov power-dow	w, the seconds n. The oscillat	s counter continues to count in power-down mode and can interrupt the CPU cor is always enabled in normal mode.
6	LOCK	PLL Lo	ock Bit. This i	s a read-only k	pit.
		Set au down,	tomatically a this bit can	at power-on to be polled to v	o indicate that the PLL loop is correctly tracking the crystal clock. After power- vait for the PLL to lock.
		Cleare might can be the PL	d automatic be due to th 12.58 MHz L to lock. If L	ally at power- ne absence of ± 20%. After t .OCK = 0, the l	on to indicate that the PLL is not correctly tracking the crystal clock. This a crystal clock or an external crystal at power-on. In this mode, the PLL output he device wakes up from power-down, user code can poll this bit to wait for PLL is not locked.
5		Not In	plemented.	Write Don't C	are.
4	LTEA	EA Sta	tus. Read-or	nly bit. Readin	g this bit returns the state of the external $\overline{\text{EA}}$ pin latched at reset or power-on.
3	FINT	Fast Interrupt Response Bit.			
		Set by	the user to	enable the res	ponse to any interrupt to be executed at the fastest core clock frequency.
		Cleared by the user to disable the fast interrupt response feature.			
		This fu	Inction must	t not be used	on 3 V parts.
2, 1, 0	CD2, CD1, CD0	CPU (O	Core Clock) [Divider Bits. Th	is number determines the frequency at which the core operates.
		CD2	CD1	CD0	Core Clock Frequency (MHz)
		0	0	0	12.582912. Not a valid selection on 3 V parts.
		0	0	1	6.291456 (Maximum core clock rate allowed on the 3 V parts)
		0	1	0	3.145728
		0	1	1	1.572864 (Default core frequency)
		1	0	0	0.786432
		1	0	1	0.393216
		1	1	0	0.196608
		1	1	1	0.098304
		On 3 V selecti CD val	/ parts (ADu(ion. If CD = 0 lue is retaine	C84xBCPxx-3 () is selected or ed.	or ADuC84xBSxx-3), the CD settings can be only CD = 1; CD = 0 is not a valid n a 3 V part by writing to PLLCON, the instruction is ignored, and the previous
		The Fa	ist Interrupt valid setting.	bit (FINT) mus	st not be used on 3 V parts since it automatically sets the CD bits to 0, which is

I2CADD-I²C Address Register 1

Function:

SFR Address:

Holds one of the I²C peripheral addresses for the device. It may be overwritten by user code. The uC001 Application Note describes the format of the I²C standard 7-bit address. 9BH

Power-On Default:	55H
Bit Addressable:	No

I2CADD1-I²C Address Register 2

Same as the I2CADD.
F2H
7FH
No

I2CDAT-I²C Data Register

Function:The I2CDAT SFR is written to by user code to transmit data, or read by user code to read data just received by
the I²C interface. Accessing I2CDAT automatically clears any pending I²C interrupt and the I2CI bit in the
I2CCON SFR. User code should access I2CDAT only once per interrupt cycle.SFR Address:9AHPower-On Default:00HBit Addressable:No

The main features of the MicroConverter I²C interface are

- Only two bus lines are required: a serial data line (SDATA) and a serial clock line (SCLOCK).
- An I²C master can communicate with multiple slave devices. Because each slave device has a unique 7-bit address, single master/slave relationships can exist at all times even in a multislave environment.
- The ability to respond to two separate addresses when operating in slave mode.
- On-chip filtering rejects <50 ns spikes on the SDATA and the SCLOCK lines to preserve data integrity.



Software Master Mode

The ADuC845/ADuC847/ADuC848 can be used as an I²C master device by configuring the I²C peripheral in master mode and writing software to output the data bit-by-bit. This is referred to as a software master. Master mode is enabled by setting the I2CM bit in the I2CCON register.

To transmit data on the SDATA line, MDE must be set to enable the output driver on the SDATA pin. If MDE is set, the SDATA pin is pulled high or low depending on whether the MDO bit is set or cleared. MCO controls the SCLOCK pin and is always configured as an output in master mode. In master mode, the SCLOCK pin is pulled high or low depending on the whether MCO is set or cleared.

To receive data, MDE must be cleared to disable the output driver on SDATA. Software must provide the clocks by toggling the MCO bit and reading the SDATA pin via the MDI bit. If MDE is cleared, MDI can be used to read the SDATA pin. The value of the SDATA pin is latched into MDI on a rising edge of SCLOCK. MDI is set if the SDATA pin is high on the last rising edge of SCLOCK. MDI is cleared if the SDATA pin is low on the last rising edge of SCLOCK.

Software must control MDO, MCO, and MDE appropriately to generate the start condition, slave address, acknowledge bits, data bytes, and stop conditions. These functions are described in the uC001 Application Note.

TIME INTERVAL COUNTER (TIC)

A TIC is provided on-chip for counting longer intervals than the standard 8051-compatible timers can count. The TIC is capable of timeout intervals ranging from 1/128 second to 255 hours. Also, this counter is clocked by the external 32.768 kHz crystal rather than by the core clock, and it can remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required. Note that instructions to the TIC SFRs are also clocked at 32.768 kHz, so sufficient time must be allowed in user code for these instructions to execute.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled. If the device is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 45. Note also that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by user software. In effect, this facilitates the implementation of a real-time clock. A basic block diagram of the TIC is shown in Figure 47. Because the TIC is clocked directly from a 32 kHz external crystal on the devices, instructions that access the TIC registers are also clocked at 32 kHz (not at the core frequency). The user must ensure that sufficient time is given for these instructions to execute.





Figure 47. TIC Simplified Block Diagram

INTVAL—User Timer Interval Select Register

Function:

User code writes the required time interval to this register. When the 8-bit interval counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled.

SFR Address:A6HPower-On Default:00HBit Addressable:NoValid Value:0 to 255 decimal

HTHSEC—Hundredths of Seconds Time Register

Function:	This register is incremented in 1/128-second intervals once TCEN in TIMECON is active. The HTHSEC SFR counts from 0 to 127 before rolling over to increment the SEC time register.
SFR Address:	A2H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 127 decimal

SEC—Seconds Time Register

Function:	This register is incremented in 1-second intervals once TCEN in TIMECON is active. The SEC SFR counts from 0 to 59 before rolling over to increment the MIN time register.
SFR Address:	A3H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

MIN-Minutes Time Register

Function	This register is incremented in 1-minute intervals once TCEN in TIMECON is active. The MIN SFR counts from 0 to 59
	before rolling over to increment the HOUR time register.
SFR Address:	A4H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 59 decimal

HOUR-Hours Time Register

Function:	This register is incremented in 1-hour intervals once TCEN in TIMECON is active. The HOUR SFR counts from 0 to 23 before rolling over to 0.
SFR Address:	A5H
Power-On Default:	00H
Bit Addressable:	No
Valid Value:	0 to 23 decimal

To enable the TIC as a real-time clock, the HOUR, MIN, SEC, and HTHSEC registers can be loaded with the current time. Once the TCEN bit is high, the TIC starts. To use the TIC as a time interval counter, select the count interval—hundredths of seconds, seconds, minutes, and hours via the ITS0 and ITS1 bits in the TIMECON SFR. Load the count required into the INTVAL SFR.

Note that INTVAL is only an 8-bit register, so user software must take into account any intervals longer than are possible with 8 bits. Therefore, to count an interval of 20 seconds, use the following procedure:

MOV TIMECON, #0D0H ;Enable 24Hour mode, count seconds, Clear TCEN. MOV INTVAL, #14H ;Load INTVAL with required count interval...in this case 14H = 20 MOV TIMECON, #0D3H ;Start TIC counting and enable the 8bit INTVAL counter.

P2.5 and P2.6 can also be used as PWM outputs, while P2.7 can act as an alternate PWM clock source. When selected as the PWM outputs, they overwrite anything written to P2.5 or P2.6.

Table 47. Port 2 Alternate Functions

Pin No.	Alternate Function
P2.0	SCLOCK for SPI
P2.1	MOSI for SPI
P2.2	MISO for SPI
P2.3	SS and T2 clock input
P2.4	T2EX alternate control for T2
P2.5	PWM0 output
P2.6	PWM1 output
P2.7	PWMCLK



Port 3

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR (B0H). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins pulled externally low source current because of the internal pull-ups.

Port 3 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 4 mA. Port 3 pins also have various secondary functions as described in Table 48. The alternate functions of Port 3 pins can be activated only if the corresponding bit latch in the P3 SFR contains a 1. Otherwise, the port pin remains at 0.

Table 48	Port 3	Alternate	Functions
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Pin No.	Alternate Function
P3.0	RxD (UART input pin, or serial data I/O in Mode 0)
P3.1	TxD (UART output pin, or serial clock output in Mode 0)
P3.2	INT0 (External Interrupt 0)
P3.3	INT1 (External Interrupt 1)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)



Read-Modify-Write Instructions

Some 8051 instructions read the latch while others read the pin. The instructions that read the latch rather than the pins are the ones that read a value, possibly change it, and rewrite it to the latch. These are called read-modify-write instructions, which are listed in Table 49. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 49. Read-Modify-Write Instructions

Instruction	Description		
ANL	Logical AND, for example, ANL P1, A		
ORL	Logical OR, for example, ORL P2, A		
XRL	Logical EX-OR, for example, XRL P3, A		
JBC	Jump if Bit = 1 and clear bit, for example, JBC P1.1, LABEL		
CPL	Complement bit, for example, CPL P3.0		
INC	Increment, for example, INC P2		
DEC	Decrement, for example, DEC P2		
DJNZ	Decrement and jump if not zero, for example, DJNZ P3, LABEL		
MOV PX.Y, C ¹	Move Carry to Bit Y of Port X		
CLR PX.Y ¹	Clear Bit Y of Port X		
SETB PX.Y ¹	Set Bit Y of Port X		

¹These instructions read the port byte (all 8 bits), modify the addressed bit, and write the new byte back to the latch.

Read-modify-write instructions are directed to the latch rather than to the pin to avoid a possible misinterpretation of the voltage level of a pin. For example, a port pin might be used to drive the base of a transistor. When 1 is written to the bit, the transistor is turned on. If the CPU reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as Logic 0. Reading the latch rather than the pin returns the correct value of 1.

TIMERS/COUNTERS

The ADuC845/ADuC847/ADuC848 have three 16-bit timer/ counters: Timer 0, Timer 1, and Timer 2. The timer/counter hardware is included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each timer/counter consists of two 8-bit registers: THx and TLx (x = 0, 1, or 2). All three can be configured to operate either as timers or as event counters.

When functioning as a timer, the TLx register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Because a machine cycle on a single-cycle core consists of one core clock period, the maximum count rate is the core clock frequency.

When functioning as a counter, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin:

TMOD—Timer/Counter 0 and 1 Mode Register

SFR Address:	89H
Power-On Default:	00H
Bit Addressable:	No

T0, T1, or T2. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. Because it takes two machine cycles (two core clock periods) to recognize a 1-to-0 transition, the maximum count rate is half the core clock frequency.

There are no restrictions on the duty cycle of the external input signal, but, to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. User configuration and control of all timer operating modes is achieved via three SFRs:

TMOD, TCON—Control and Configuration for Timers 0 and 1

T2CON—Control and Configuration for Timer 2.

Bit No.	Name	Descri	iption		
7	Gate	Timer 1 Gating Control.			
		Set by software to enable Timer/Counter 1 only while the INT1 pin is high and the TR1 control is set.			
		Cleared by software to enable Timer 1 whenever the TR1control bit is set.			
6	C/T	Timer	1 Timer or	Counter Select Bit.	
		Set by	software	to select counter operation (input from T1 pin).	
		Cleared by software to select the timer operation (input from internal system clock).			
5, 4	M1, M0	Timer 1 Mode Select Bits.			
		M1	MO	Description	
		0	0	TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler.	
		0	1	16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler.	
		1	0	8-Bit Autoreload Timer/Counter. TH1 holds a value that is to be reloaded into TL1 each time it overflows.	
		1	1	Timer/Counter 1 Stopped.	
3	Gate	Timer 0 Gating Control.			
		Set by software to enable Timer/Counter 0 only while the $\overline{INT0}$ pin is high and the TR0 control bit is set.			
		Cleared by software to enable Timer 0 whenever the TR0 control bit is set.			
2	C/T	Timer 0 Timer or Counter Select Bit.			
		Set by software to the select counter operation (input from T0 pin).			
		Cleared by software to the select timer operation (input from internal system clock).			
1, 0	M1, M0	Timer 0 Mode Select Bits.			
		M1	MO	Description	
		0	0	TH0 operates as an 8-bit timer/counter. TL0 serves as a 5-bit prescaler.	
		0	1	16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler.	
		1	0	8-Bit Autoreload Timer/Counter. TH0 holds a value that is to be reloaded into TL0 each time it overflows.	
		1	1	TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits.	
				TH0 is an 8-bit timer only, controlled by Timer 1 control bits.	

Table 50. TMOD SFR Bit Designation

Timer/Counter 0 and 1 Operating Modes

This section describes the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 52 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.



1. THE CORE CLOCK IS THE OUTPUT OF THE PLL (SEE THE ON-CHIP PLL SECTION)

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulsewidth measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 53.



Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload as shown in Figure 54. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.



Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 55. TL0 uses the Timer 0 Control Bits C/T, Gate, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 then controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.



INTERRUPT SYSTEM

The ADuC845/ADuC847/ADuC848 provide nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE	Interrupt Enable	Register
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- IP Interrupt Priority Register
- IEIP2 Secondary Interrupt Enable Register

IE—Interrupt Enable Register

SFR Address:A8HPower-On Default:00HBit Addressable:Yes

Table 58. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable all interrupt sources.
		Cleared by the user to disable all interrupt sources.
6	EADC	Set by the user to enable the ADC interrupt.
		Cleared by the user to disable the ADC interrupt.
5	ET2	Set by the user to enable the Timer 2 interrupt.
		Cleared by the user to disable the Timer 2 interrupt.
4	ES	Set by the user to enable the UART serial port interrupt.
		Cleared by the user to disable the UART serial port interrupt.
3	ET1	Set by the user to enable the Timer 1 interrupt.
		Cleared by the user to disable the Timer 1 interrupt.
2	EX1	Set by the user to enable External Interrupt 1 (INTO).
		Cleared by the user to disable External Interrupt 1 (INT0).
1	ET0	Set by the user to enable the Timer 0 interrupt.
		Cleared by the user to disable the Timer 0 interrupt.
0	EX0	Set by the user to enable External Interrupt 0 (INTO).
		Cleared by the user to disable External Interrupt 0 (INT0).

IP—Interrupt Priority Register

SFR Address:B8HPower-On Default:00HBit Addressable:Yes

Table 59. IP SFR Bit Designations

Bit No.	Name	Description
7		Not Implemented. Write Don't Care.
6	PADC	ADC Interrupt Priority (1 = High; $0 = Low$).
5	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	PX1	\overline{INTO} (External Interrupt 1) priority (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	PX0	\overline{INTO} (External Interrupt 0) Priority (1 = High; 0 = Low).

Table 71. SPI SLAVE MODE TIMING (CPHA = 0) Parameter

		Min	Тур	Max	Unit
tss	SS to SCLOCK Edge	0			ns
tsL	SCLOCK Low Pulse Width		330		ns
t _{sн}	SCLOCK High Pulse Width		330		ns
t _{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t DSU	Data Input Setup Time Before SCLOCK Edge	100			ns
t DHD	Data Input Hold Time After SCLOCK Edge	100			ns
t _{DF}	Data Output Fall Time		10	25	ns
t _{DR}	Data Output Rise Time		10	25	ns
t _{sr}	SCLOCK Rise Time		10	25	ns
t _{SF}	SCLOCK Fall Time		10	25	ns
t _{DOSS}	Data Output Valid After SS Edge			20	ns
tsfs	SS High After SCLOCK Edge				ns



Figure 79. SPI Slave Mode Timing (CHPA = 0)

NOTES