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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc847bsz32-3

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AUXILIARY ADC ANALOG INPUTS (ADuC845 ONLY)					
Differential Input Voltage Ranges[5,6]					
Bipolar Mode (ADC1CON.5 = 0)		$\pm V_{REF}$		V	REFIN = REFIN(+) − REFIN(−) (or Int 1.25 V_{REF})
Unipolar Mode (ADC1CON.5 = 1)		0 − V_{REF}		V	REFIN = REFIN(+) − REFIN(−) (or Int 1.25 V_{REF})
Average Analog Input Current		125		nA/V	
Analog Input Current Drift		±2		pA/V/°C	
Absolute AIN/AINCOM Voltage Limits[2,7]	A_{GND} − 0.03		AV_{DD} + 0.03	V	
Normal Mode Rejection 50 Hz/60 Hz[2]					
On AIN and REFIN	75			dB	50 Hz/60 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off
ADC SYSTEM CALIBRATION					
Full-Scale Calibration Limit			+1.05 × FS	V	
Zero-Scale Calibration Limit	−1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	
DAC					
Voltage Range		0 − V_{REF}		V	DACCON.2 = 0
		0 − AV_{DD}		V	DACCON.2 = 1
Resistive Load		10		kΩ	From DAC output to AGND
Capactive Load		100		pF	From DAC output to AGND
Output Impedance		0.5		Ω	
I_{SINK}		50		µA	
DC Specifications[8]					
Resolution	12			Bits	
Relative Accuracy		±3		LSB	
Differential Nonlinearity			−1	LSB	Guaranteed 12-bit monotonic
Offset Error			±50	mV	
Gain Error			±1	%	AV_{DD} range
		±1		%	V_{REF} range
AC Specifications[2,8]					
Voltage Output Settling Time		15		µs	Settling time to 1 LSB of final value
Digital-to-Analog Glitch Energy		10		nVs	1 LSB change at major carry
INTERNAL REFERENCE					
ADC Reference					Chop enabled
Reference Voltage	1.25 − 1%	1.25	1.25 + 1%	V	Initial tolerance @ 25°C, V_{DD} = 5 V
Power Supply Rejection		45		dB	
Reference Tempco		100		ppm/°C	
DAC Reference					
Reference Voltage	2.5 − 1%	2.5	2.5 + 1%	±1% V	Initial tolerance @ 25°C, V_{DD} = 5 V
Power Supply Rejection		50		dB	
Reference Tempco		±100		ppm/°C	
TEMPERATURE SENSOR (ADuC845 ONLY)					
Accuracy		±2		°C	
Thermal Impedance		90		°C/W	MQFP
		52		°C/W	LFCSP

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSDUCER BURNOUT CURRENT SOURCES					
AIN+ Current		−100		nA	AIN+ is the selected positive input (AIN4 or AIN6 only) to the primary ADC
AIN− Current		100		nA	AIN− is the selected negative input (AIN5 or AIN7 only) to the primary ADC
Initial Tolerance at 25°C		±10		%	
Drift		0.03		%/°C	
EXCITATION CURRENT SOURCES					
Output Current		200		µA	Available from each current source
Initial Tolerance at 25°C		±10		%	
Drift		200		ppm/°C	
Initial Current Matching at 25°C		±1		%	Matching between both current sources
Drift Matching		20		ppm/°C	
Line Regulation (AV_{DD})		1		µA/V	AV_{DD} = 5 V ± 5%
Load Regulation		0.1		µA/V	
Output Compliance[2]	AGND		AV_{DD} − 0.6	V	
POWER SUPPLY MONITOR (PSM)					
AV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
AV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
DV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
DV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)					
Logic Inputs, XTAL1 Only[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	3.5			V	DV_{DD} = 5 V
	2.5			V	DV_{DD} = 3 V
XTAL1 Input Capacitance		18		pF	
XTAL2 Output Capacitance		18		pF	
LOGIC INPUTS					
All Inputs Except SCLOCK, RESET, and XTAL1[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	2.0			V	
SCLOCK and RESET Only (Schmidt Triggered Inputs)[2]					
V_{T+}	1.3		3.0	V	DV_{DD} = 5 V
	0.95		2.5	V	DV_{DD} = 3 V
V_{T-}	0.8		1.4	V	DV_{DD} = 5 V
	0.4		1.1	V	DV_{DD} = 3 V
$V_{T+} - V_{T-}$	0.3		0.85	V	DV_{DD} = 5 V or 3 V
Input Currents					
Port 0, P1.0 to P1.7, $\overline{EA}$			±10	µA	V_{IN} = 0 V or V_{DD}
RESET			±10	µA	V_{IN} = 0 V, DV_{DD} = 5 V
	35		105	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V, internal pull-down
Port 2, Port 3			±10	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V
	−180		−660	µA	V_{IN} = 2 V, DV_{DD} = 5 V
	−20		−75	µA	V_{IN} = 0.45 V, DV_{DD} = 5 V
Input Capacitance		10		pF	All digital inputs

ADC Noise Performance with Chop Enabled ($\overline{CHOP}$ = 0)

Table 10, Table 11, Table 12, and Table 13 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates for the ADuC845, ADuC847, and ADuC848. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are in the same range as the bipolar figures, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution.

Table 10. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	1.75	1.30	1.65	1.5	2.1	3.1	7.15	13.3
23	59.36	1.25	0.95	1.08	0.94	1.0	1.87	3.24	7.1
27	50.56	1.0	1.0	0.85	0.85	1.13	1.56	2.9	3.6
69	19.79	0.63	0.68	0.52	0.7	0.61	1.1	1.3	2.75
255	5.35	0.31	0.38	0.34	0.32	0.4	0.45	0.68	1.22

Table 11. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	12	13	14	15	15.5	16	16	16
23	59.36	12	13.5	14.5	15.5	16.5	16.5	17	16.5
27	50.56	12.5	13.5	15	16	16.5	17	17	17.5
69	19.79	13	14	15.5	16	17.5	17.5	18	18
255	5.35	14.5	15	16	17	18	18.5	19	19.5

Table 12. ADuC848 Typical Output Noise (μV) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	1.75	1.30	1.65	1.5	2.1	3.1	7.15	13.3
23	59.36	1.25	0.95	1.08	0.94	1.0	1.87	3.24	7.1
27	50.56	1.0	1.0	0.85	0.85	1.13	1.56	2.9	3.6
69	19.79	0.63	0.68	0.52	0.7	0.61	1.1	1.3	2.75
255	5.35	0.31	0.38	0.34	0.32	0.4	0.45	0.68	1.22

Table 13. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Enabled

		Input Range							
SF Word	Data Update Rate (Hz)	±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.03	12	13	14	15	15.5	16	16	16
23	59.36	12	13.5	14.5	15.5	16	16	17	16
27	50.56	12.5	13.5	15	16	16	16	16	16
69	19.79	13	14	15.5	16	16	16	16	16
255	5.35	14.5	15	16	16	16	16	16	16

that the internal calibration procedure for full-scale calibration automatically selects the reference in voltage at PGA = 1.

Therefore, the full-scale endpoint calibration automatically subtracts the offset calibration error, it is advisable to perform an offset calibration at the same gain range as that used for full-scale calibration. There is no penalty to the full-scale calibration in redoing the zero-scale calibration at the required PGA range because the full-scale calibration has very good matching at all the PGA ranges.

This procedure also applies when chop is disabled.

Note that for internal calibration to be effective, the AIN− pin should be held at a steady voltage, within the allowable common-mode range to keep it from floating during calibration.

System Calibration Example

With chop enabled, a system zero-scale or offset calibration should never be required. However, if a full-scale or gain calibration is required for any reason, use the following typical procedure for doing so.

1. Apply a differential voltage of 0 V to the selected analog inputs (AIN+ to AIN−) that are held at a common-mode voltage.

   Perform a system zero-scale or offset calibration by setting the MD2...0 bits in the ADCMODE register to 110B.

2. Apply a full-scale differential voltage across the ADC inputs again at the same common-mode voltage.

   Perform a system full-scale or gain calibration by setting the MD2...0 bits in the ADCMODE register to 111B.

Perform a system calibration at the required PGA range to be used since the ADC scales to the differential voltages that are applied to the ADC during the calibration routines.

In bipolar mode, the zero-scale calibration determines the mid-scale point of the ADC (800000H) or 0 V.

PROGRAMMABLE GAIN AMPLIFIER

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different ranges, which are programmed via the range bits (RN0 to RN2) in the ADC0CON1 register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V and 0 V to 2.56 V, while in bipolar mode the ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±64 0 mV, ±1.28 V, and ±2.56 V. These ranges should appear on the input to the on-chip PGA. The ADC range-matching specification of 2 µV (typical with chop enabled) means that calibration need only be carried out on a single range and need not be repeated when the ADC range is changed. This is a significant advantage compared to similar mixed-signal solutions available on the market. The auxiliary (ADuC845 only) ADC does not incorporate a PGA, and the gain is fixed at 0 V to 2.50 V in unipolar mode, and ±2.50 V in bipolar mode.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog inputs of the ADuC845/ADuC847/ADuC848 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the device can handle negative voltages with respect to system AGND, but rather with respect to the negative reference input. Unipolar and bipolar signals on the AIN(+) input on the ADC are referenced to the voltage on the respective AIN(−) input. AIN(+) and AIN(−) refer to the signals seen by the ADC.

For example, if AIN(−) is biased to 2.5 V (tied to the external reference voltage) and the ADC is configured for a unipolar analog input range of 0 mV to >20 mV, the input voltage range on AIN(+) is 2.5 V to 2.52 V. On the other hand, if AIN(−) is biased to 2.5 V (again the external reference voltage) and the ADC is configured for a bipolar analog input range of ±1.28 V, the analog input range on the AIN(+) is 1.22 V to 3.78 V, that is, 2.5 V ± 1.28 V.

The modes of operation for the ADC are fully differential mode or pseudo differential mode. In fully differential mode, AIN1 to AIN2 are one differential pair, and AIN3 to AIN4 are another pair (AIN5 to AIN6, AIN7 to AIN8, and AIN9 to AIN10 are the others). In differential mode, all AIN(−) pin names imply the negative analog input of the selected differential pair, that is, AIN2, AIN4, AIN6, AIN8, AIN10. The term AIN(+) implies the positive input of the selected differential pair, that is, AIN1, AIN3, AIN5, AIN7, AIN9. In pseudo differential mode, each analog input is paired with the AINCOM pin, which can be biased up or tied to AGND. In this mode, the AIN(−) implies AINCOM, and AIN(+) implies any one of the ten analog input channels.

The configuration of the inputs (unipolar vs. bipolar) is shown in Figure 17.

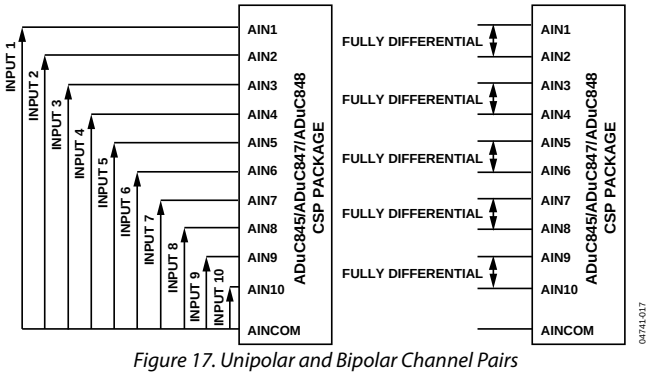

Figure 17. Unipolar and Bipolar Channel Pairs

TYPICAL PERFORMANCE CHARACTERISTICS

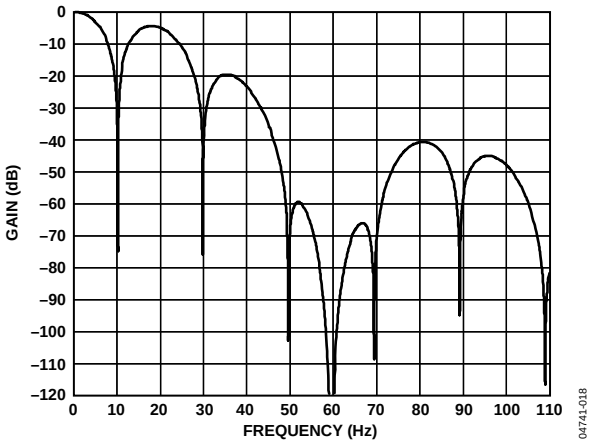

Figure 18. Filter Response, Chop On, SF = 69 Decimal

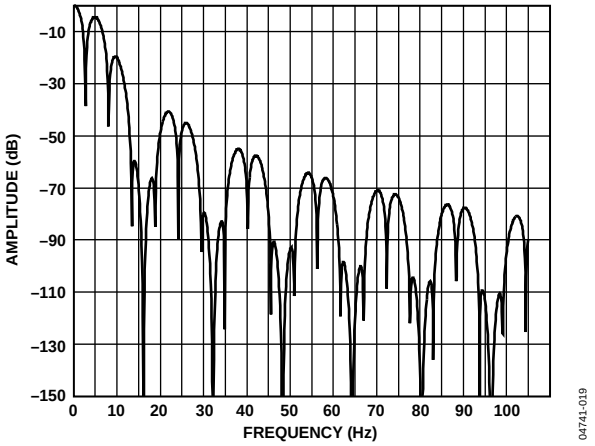

Figure 19. Filter Response, Chop On, SF = 255 Decimal

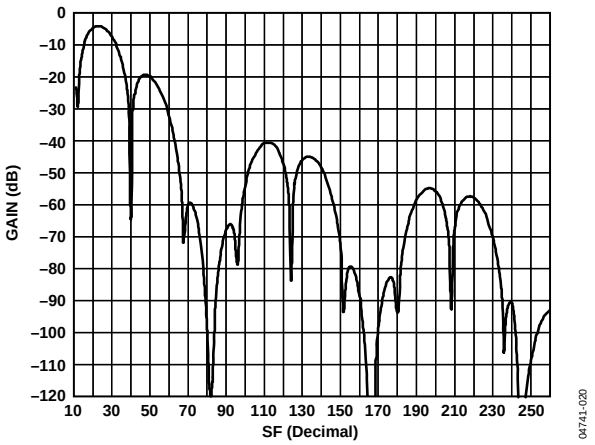

Figure 20. 50 Hz Normal Mode Rejection vs. SF Word, Chop On

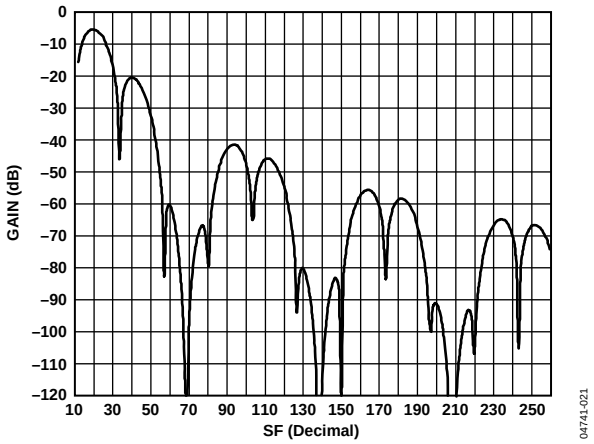

Figure 21. 60 Hz Normal Mode Rejection vs. SF, Chop On

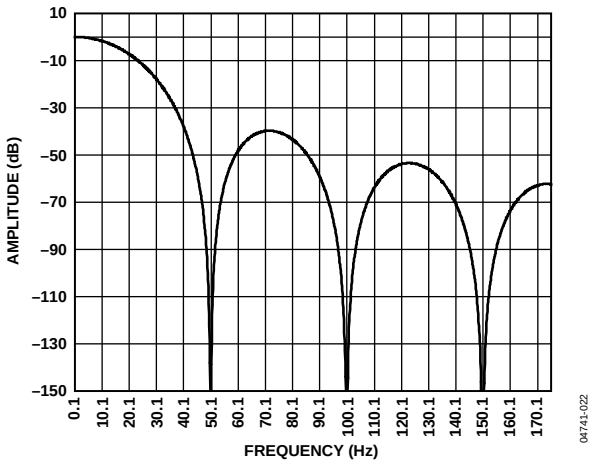

Figure 22. Chop Off, Fadc = 50 Hz, SF = 52H

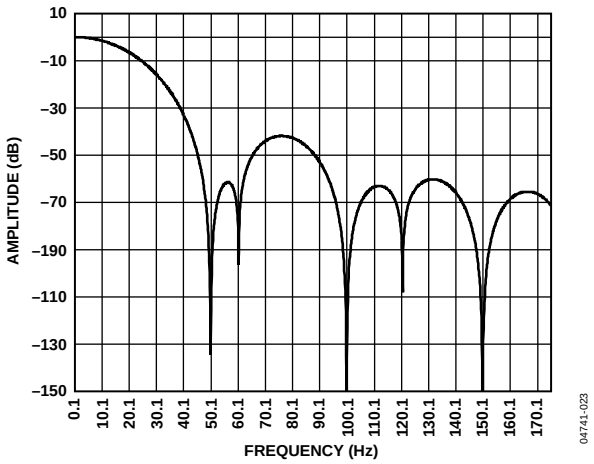

Figure 23. Chop Off, SF = 52H, REJ60 Enabled

USER DOWNLOAD MODE (ULOAD)

Figure 28 shows that it is possible to use the 62 kbytes of Flash/EE program memory available to the user as one single block of memory. In this mode, all the Flash/EE memory is read-only to user code.

However, most of the Flash/EE program memory can also be written to during run time simply by entering ULOAD mode. In ULOAD mode, the lower 56 kbytes of program memory can be erased and reprogrammed by the user software as shown in Figure 30. ULOAD mode can be used to upgrade the code in the field via any user-defined download protocol. By configuring the SPI port on the ADuC845/ADuC847/ADuC848 as a slave, it is possible to completely reprogram the 56 kbytes of Flash/EE program memory in under 5 s (see the AN-1074 Application Note).

Alternatively, ULOAD mode can be used to save data to the 56 kbytes of Flash/EE memory. This can be extremely useful in data logging applications where the devices can provide up to 60 kbytes of data memory on-chip (4 kbytes of dedicated Flash/EE data memory also exist).

The upper 6 kbytes of the 62 kbytes of Flash/EE program memory (8 kbytes on the 32-kbyte parts) are programmable only via serial download or parallel programming. This means that this space appears as read-only to user code; therefore, it cannot be accidentally erased or reprogrammed by erroneous code execution, making it very suitable to use the 6 kbytes as a bootloader. A bootload enable option exists in the Windows® serial downloader (WSD) to "Always RUN from E000H after Reset." If using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset.

Programming the Flash/EE program memory via ULOAD mode is described in the Flash/EE Memory Control SFR section of ECON and also in the AN-1074 Application Note.

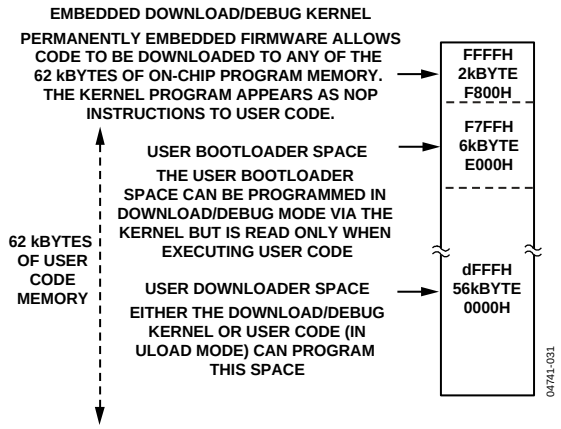

Figure 30. Flash/EE Program Memory Map in ULOAD Mode (62-kbyte Part)

The 32-kbyte memory parts have the user bootload space starting at 6000H. The memory mapping is shown in Figure 31.

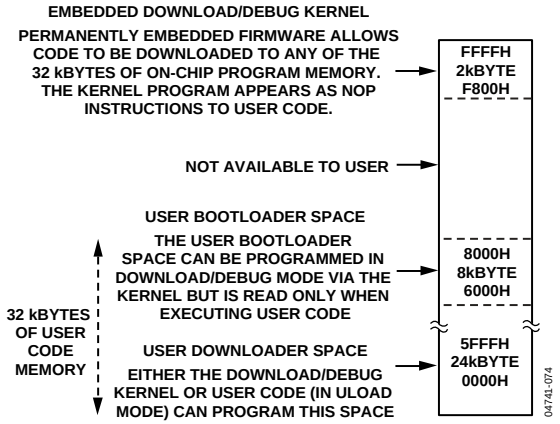

Figure 31. Flash/EE Program Memory Map in ULOAD Mode (32-kbyte Part)

ULOAD mode is not available on the 8-kbyte Flash/EE program memory parts.

Flash/EE Program Memory Security

The ADuC845/ADuC847/ADuC848 facilitate three modes of Flash/EE program memory security: the lock, secure, and serial safe modes. These modes can be independently activated, restricting access to the internal code space. They can be enabled as part of serial download protocol, as described in the AN-1074 Application Note, or via parallel programming.

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in parallel mode and reading the memory via a MOVC command from external memory are still allowed. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Secure Mode

This mode locks the code memory, disabling parallel programming of the program memory. Reading/verifying the memory in parallel mode and reading the internal memory via a MOVC command from external memory are also disabled. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the device into serial download mode, that is, RESET asserted (pulled high) and de-asserted (pulled low) with $\overline{\text{PSEN}}$ low, the device interprets the serial download reset as a normal reset only. It therefore does not enter serial download mode, but executes only a normal reset sequence. Serial safe mode can be disabled only by initiating an ERASE CODE AND DATA command in parallel programming mode.

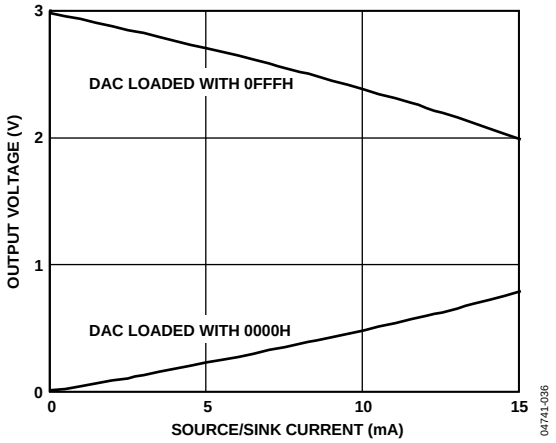

Figure 36. Source and Sink Current Capability with V_{REF} = AV_{DD} = 3 V

For larger loads, the current drive capability may not be sufficient. To increase the source and sink current capability of the DAC, an external buffer should be added as shown in Figure 37.

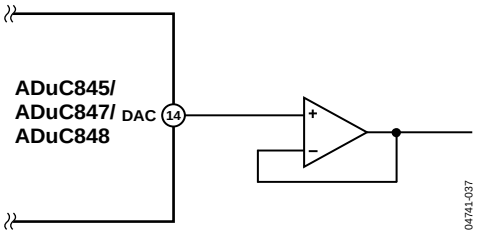

Figure 37. Buffering the DAC Output

The internal DAC output buffer also features a high impedance disable function. In the chip's default power-on state, the DAC is disabled and its output is in a high impedance state (or three-state) where it remains inactive until enabled in software. This means that if a zero output is desired during power-on or power-down transient conditions, a pull-down resistor must be added to each DAC output. Assuming that this resistor is in place, the DAC output remains at ground potential whenever the DAC is disabled.

PULSE-WIDTH MODULATOR (PWM)

The ADuC845/ADuC847/ADuC848 has a highly flexible PWM offering programmable resolution and an input clock. The PWM can be configured in six different modes of operation. Two of these modes allow the PWM to be configured as a Σ-Δ DAC with up to 16 bits of resolution. A block diagram of the PWM is shown in Figure 38.

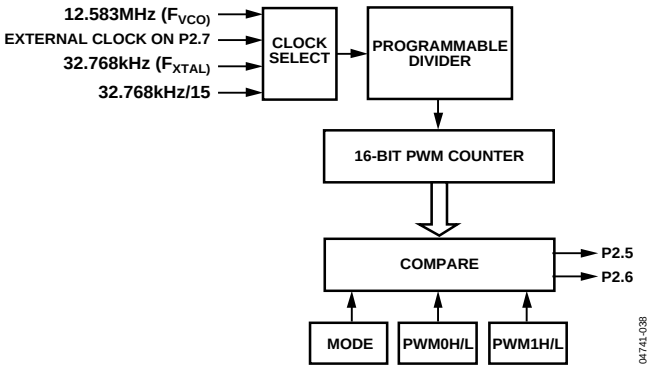

Figure 38. PWM Block Diagram

The PWM uses control SFR, PWMCON, and four data SFRs: PWM0H, PWM0L, PWM1H, and PWM1L.

PWMCON (as described in Table 34) controls the different modes of operation of the PWM as well as the PWM clock frequency. PWM0H/L and PWM1H/L are the data registers that determine the duty cycles of the PWM outputs at P2.5 and P2.6.

To use the PWM user software, first write to PWMCON to select the PWM mode of operation and the PWM input clock. Writing to PWMCON also resets the PWM counter. In any of the 16-bit modes of operation (Modes 1, 3, 4, 6), user software should write to the PWM0L or PWM1L SFRs first. This value is written to a hidden SFR. Writing to the PWM0H or PWM1H SFRs updates both the PWMxH and the PWMxL SFRs but does not change the outputs until the end of the PWM cycle in progress. The values written to these 16-bit registers are then used in the next PWM cycle.

The outputs of the PWM at P2.5 and P2.6 are shown in Figure 40. As can be seen, the output of PWM0 (P2.5) goes low when the PWM counter equals PWM0L. The output of PWM1 (P2.6) goes high when the PWM counter equals PWM1H and goes low again when the PWM counter equals PWM0H. Setting PWM1H to 0 ensures that both PWM outputs start simultaneously.

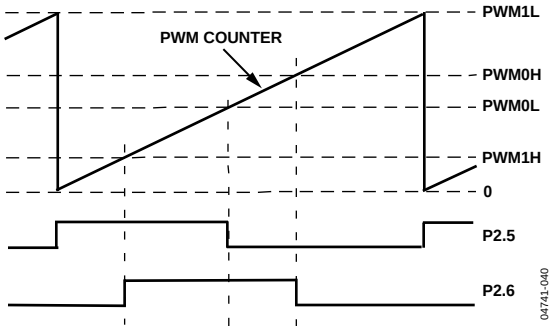

Figure 40. PWM Mode 2

Mode 3 (Twin 16-Bit PWM)

In Mode 3, the PWM counter is fixed to count from 0 to 65536, giving a fixed 16-bit PWM. Operating from the 12.58 MHz core clock results in a PWM output rate of 192 Hz. The duty cycle of the PWM outputs at P2.5 and P2.6 are independently programmable.

As shown in Figure 41, while the PWM counter is less than PWM0H/L, the output of PWM0 (P2.5) is high. Once the PWM counter equals PWM0H/L, PWM0 (P2.5) goes low and remains low until the PWM counter rolls over.

Similarly, while the PWM counter is less than PWM1H/L, the output of PWM1 (P2.6) is high. Once the PWM counter equals PWM1H/L, PWM1 (P2.6) goes low and remains low until the PWM counter rolls over.

In this mode, both PWM outputs are synchronized, that is, once the PWM counter rolls over to 0, both PWM0 (P2.5) and PWM1 (P2.6) go high.

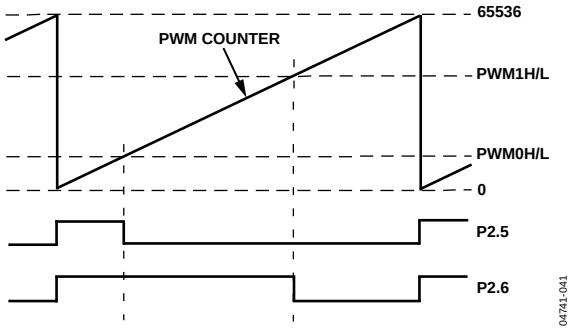

Figure 41. PWM Mode 3

Mode 4 (Dual NRZ 16-Bit Σ-Δ DAC)

Mode 4 provides a high speed PWM output similar to that of a Σ-Δ DAC. Typically, this mode is used with the PWM clock equal to 12.58 MHz.

In this mode, P2.5 and P2.6 are updated every PWM clock (80 ns in the case of 12.58 MHz). Over any 65536 cycles (16-bit PWM), PWM0 (P2.5) is high for PWM0H/L cycles and low for (65536 – PWM0H/L) cycles. Similarly, PWM1 (P2.6) is high for PWM1H/L cycles and low for (65536 – PWM1H/L) cycles.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three clocks and high for one clock (each clock is approximately 80 ns). Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale, by having a high cycle followed by only two low cycles.

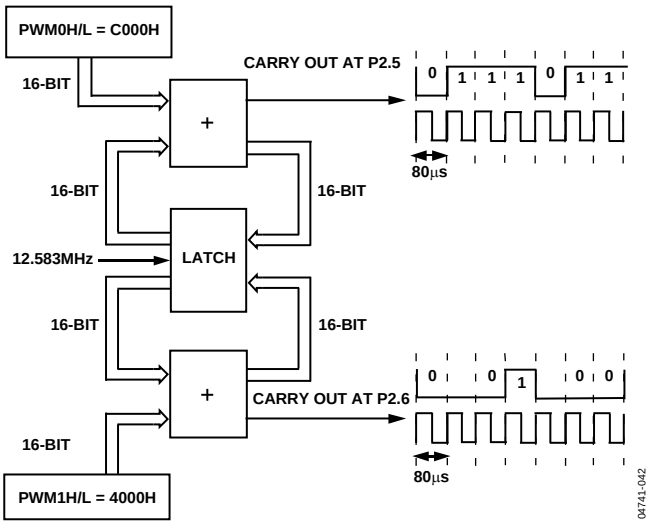

Figure 42. PWM Mode 4

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

ON-CHIP PLL (PLLCON)

The ADuC845/ADuC847/ADuC848 are intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple (384) of this to provide a stable 12.582912 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power saving when maximum core performance is not required. The default core clock is the PLL clock divided by 8 or 1.572864 MHz. The ADC clocks are also derived from the PLL clock, with the modulator rate being the same as the crystal oscillator frequency. The control register for the PLL is called PLLCON and is described as follows.

The 5 V parts can be set to a maximum core frequency of 12.58 MHz (CD2...0 = 000) while at 3 V, the maximum core clock rate is 6.29 MHz (CD2...0 = 001). The CD bits should not be set to 000b on the 3 V parts.

The 3 V parts are limited to a core clock speed of 6.29 MHz (CD = 1).

PLLCON PLL Control Register

SFR Address: D7H
Power-On Default: 53H
Bit Addressable: No

Table 39. PLLCON PLL Control Register

Bit No.	Name	Description
7	OSC_PD	Oscillator Power-Down Bit. If low, the 32 kHz crystal oscillator continues running in power-down mode. If high, the 32.768 kHz oscillator is powered down. When this bit is low, the seconds counter continues to count in power-down mode and can interrupt the CPU to exit power-down. The oscillator is always enabled in normal mode.
6	LOCK	PLL Lock Bit. This is a read-only bit. Set automatically at power-on to indicate that the PLL loop is correctly tracking the crystal clock. After power-down, this bit can be polled to wait for the PLL to lock. Cleared automatically at power-on to indicate that the PLL is not correctly tracking the crystal clock. This might be due to the absence of a crystal clock or an external crystal at power-on. In this mode, the PLL output can be 12.58 MHz ± 20%. After the device wakes up from power-down, user code can poll this bit to wait for the PLL to lock. If LOCK = 0, the PLL is not locked.
5	–––	Not Implemented. Write Don't Care.
4	LTEA	EA Status. Read-only bit. Reading this bit returns the state of the external $\overline{EA}$ pin latched at reset or power-on.
3	FINT	Fast Interrupt Response Bit. Set by the user to enable the response to any interrupt to be executed at the fastest core clock frequency. Cleared by the user to disable the fast interrupt response feature. This function must not be used on 3 V parts.
2, 1, 0	CD2, CD1, CD0	CPU (Core Clock) Divider Bits. This number determines the frequency at which the core operates. CD2 CD1 CD0 Core Clock Frequency (MHz) 0 0 0 12.582912. Not a valid selection on 3 V parts. 0 0 1 6.291456 (Maximum core clock rate allowed on the 3 V parts) 0 1 0 3.145728 0 1 1 1.572864 (Default core frequency) 1 0 0 0.786432 1 0 1 0.393216 1 1 0 0.196608 1 1 1 0.098304 On 3 V parts (ADuC84xBCPxx-3 or ADuC84xBSxx-3), the CD settings can be only CD = 1; CD = 0 is not a valid selection. If CD = 0 is selected on a 3 V part by writing to PLLCON, the instruction is ignored, and the previous CD value is retained. The Fast Interrupt bit (FINT) must not be used on 3 V parts since it automatically sets the CD bits to 0, which is not a valid setting.

SPICON—SPI Control Register

SFR Address: F8H
Power-On Default: 05H
Bit Addressable: Yes

Table 41. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user code to enable SPI functionality. Cleared by user code to enable standard Port 2 functionality.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user code to enable master mode operation (SCLOCK is an output). Cleared by user code to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Bit. Set by user code to enable SCLOCK idle high. Cleared by user code to enable SCLOCK idle low.
2	CPHA[1]	Clock Phase Select Bit. Set by user code if the leading SCLOCK edge is to transmit data. Cleared by user code if the trailing SCLOCK edge is to transmit data.
1, 0	SPR1, SPR0	SPI Bit-Rate Bits. SPR1 SPR0 Selected Bit Rate 0 0 $f_{core}/2$ 0 1 $f_{core}/4$ 1 0 $f_{core}/8$ 1 1 $f_{core}/16$

[1] The CPOL and CPHA bits should both contain the same values for master and slave devices.

Note that both SPI and I²C use the same ISR (Vector Address 3BH); therefore, when using SPI and I²C simultaneously, it is necessary to check the interfaces following an interrupt to determine which one caused the interrupt.

SPIDAT: SPI Data Register

SFR Address: 7FH
Power-On Default: 00H
Bit Addressable: No

USING THE SPI INTERFACE

Depending on the configuration of the bits in the SPICON SFR shown in Table 41, the SPI interface transmits or receives data in a number of possible modes. Figure 46 shows all possible ADuC845/ADuC847/ADuC848 SPI configurations and the timing relationships and synchronization among the signals involved. Also shown in this figure is the SPI interrupt bit (ISPI) and how it is triggered at the end of each byte-wide communication.

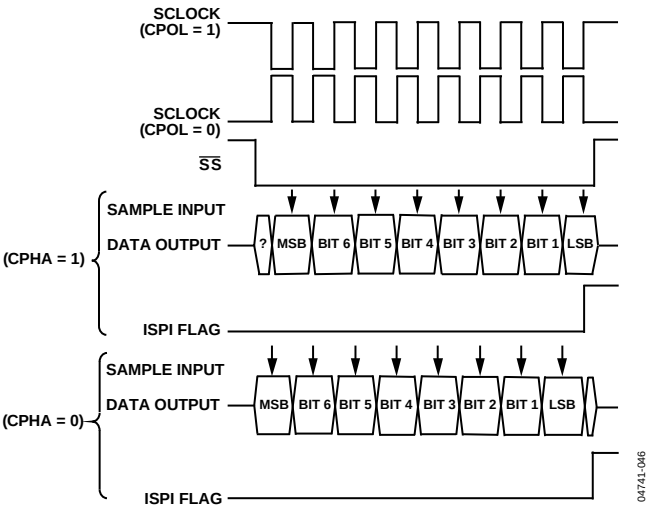

Figure 46. SPI Timing, All Modes

SPI Interface—Master Mode

In master mode, the SCLOCK pin is always an output and generates a burst of eight clocks whenever user code writes to the SPIDAT register. The SCLOCK bit rate is determined by SPR0 and SPR1 in SPICON. Also note that the $\overline{SS}$ pin is not used in master mode. If the devices need to assert the $\overline{SS}$ pin on an external slave device, use a port digital output pin.

In master mode, a byte transmission or reception is initiated by a byte write to SPIDAT. The hardware automatically generates eight clock periods via the SCLOCK pin, and the data is transmitted via MOSI. With each SCLOCK period, a data bit is also sampled via MISO. After eight clocks, the transmitted byte is completely transmitted (via MOSI), and the input byte (if required) is waiting in the input shift register (after being received via MISO). The ISPI flag is set automatically, and an interrupt occurs if enabled. The value in the input shift register is latched into SPIDAT.

SPI Interface—Slave Mode

In slave mode, the SCLOCK is an input. The $\overline{SS}$ pin must also be driven low externally during the byte communication. Transmission is also initiated by a write to SPIDAT. In slave mode, a data bit is transmitted via MISO, and a data bit is received via MOSI through each input SCLOCK period. After eight clocks, the transmitted byte is completely transmitted, and the input byte is waiting in the input shift register. The ISPI flag is set automatically, and an interrupt occurs, if enabled. The value in the shift register is latched into SPIDAT only when the transmission/reception of a byte has been completed. The end of transmission occurs after the eighth clock has been received if CPHA = 1, or when $\overline{SS}$ returns high if CPHA = 0.

P2.5 and P2.6 can also be used as PWM outputs, while P2.7 can act as an alternate PWM clock source. When selected as the PWM outputs, they overwrite anything written to P2.5 or P2.6.

Table 47. Port 2 Alternate Functions

Pin No.	Alternate Function
P2.0	SCLOCK for SPI
P2.1	MOSI for SPI
P2.2	MISO for SPI
P2.3	$\overline{SS}$ and T2 clock input
P2.4	T2EX alternate control for T2
P2.5	PWM0 output
P2.6	PWM1 output
P2.7	PWMCLK

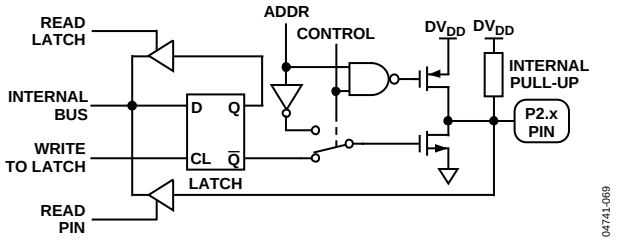

Figure 50. Port 2 Bit Latch and I/O Buffer

Port 3

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR (B0H). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins pulled externally low source current because of the internal pull-ups.

Port 3 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 4 mA. Port 3 pins also have various secondary functions as described in Table 48. The alternate functions of Port 3 pins can be activated only if the corresponding bit latch in the P3 SFR contains a 1. Otherwise, the port pin remains at 0.

Table 48. Port 3 Alternate Functions

Pin No.	Alternate Function
P3.0	RxD (UART input pin, or serial data I/O in Mode 0)
P3.1	TxD (UART output pin, or serial clock output in Mode 0)
P3.2	$\overline{INT0}$ (External Interrupt 0)
P3.3	$\overline{INT1}$ (External Interrupt 1)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

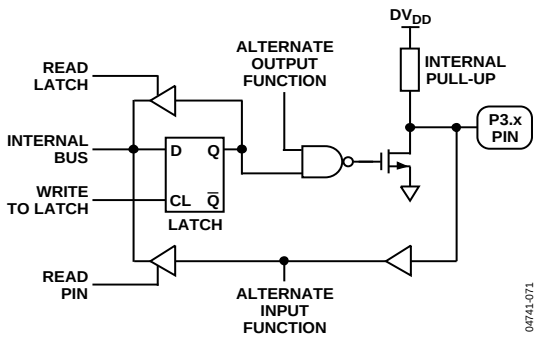

Figure 51. Port 3 Bit Latch and I/O Buffer

Read-Modify-Write Instructions

Some 8051 instructions read the latch while others read the pin. The instructions that read the latch rather than the pins are the ones that read a value, possibly change it, and rewrite it to the latch. These are called read-modify-write instructions, which are listed in Table 49. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 49. Read-Modify-Write Instructions

Instruction	Description
ANL	Logical AND, for example, ANL P1, A
ORL	Logical OR, for example, ORL P2, A
XRL	Logical EX-OR, for example, XRL P3, A
JBC	Jump if Bit = 1 and clear bit, for example, JBC P1.1, LABEL
CPL	Complement bit, for example, CPL P3.0
INC	Increment, for example, INC P2
DEC	Decrement, for example, DEC P2
DJNZ	Decrement and jump if not zero, for example, DJNZ P3, LABEL
MOV PX.Y, C[1]	Move Carry to Bit Y of Port X
CLR PX.Y[1]	Clear Bit Y of Port X
SETB PX.Y[1]	Set Bit Y of Port X

[1] These instructions read the port byte (all 8 bits), modify the addressed bit, and write the new byte back to the latch.

Read-modify-write instructions are directed to the latch rather than to the pin to avoid a possible misinterpretation of the voltage level of a pin. For example, a port pin might be used to drive the base of a transistor. When 1 is written to the bit, the transistor is turned on. If the CPU reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as Logic 0. Reading the latch rather than the pin returns the correct value of 1.

TCON—Timer/Counter 0 and 1 Control Register

SFR Address: 88H
Power-On Default: 00H
Bit Addressable: Yes

Table 51. TCON SFR Bit Designations

Bit No.	Name	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the program counter (PC) vectors to the interrupt service routine.
6	TR1	Timer 1 Run Control Bit. Set by the user to turn on Timer/Counter 1. Cleared by the user to turn off Timer/Counter 1.
5	TF0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	TR0	Timer 0 Run Control Bit. Set by the user to turn on Timer/Counter 0. Cleared by the user to turn off Timer/Counter 0.
3	IE1[1]	External Interrupt 1 ($\overline{INT1}$) Flag. Set by hardware by a falling edge or by a zero level applied to the external interrupt pin, $\overline{INT1}$, depending on the state of Bit IT1. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
2	IT1[1]	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.
1	IE0[1]	External Interrupt 0 ($\overline{INT0}$) Flag. Set by hardware by a falling edge or by a zero level being applied to the external interrupt pin, $\overline{INT0}$, depending on the statue of Bit IT0. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag rather than the on-chip hardware.
0	IT0[1]	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge-sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level-sensitive detection, that is, zero level.

[1] These bits are not used to control Timer/Counters 0 and 1, but are used instead to control and monitor the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Timer/Counter 0 and 1 Data Registers

Each timer consists of two 8-bit registers. These can be used as independent registers or combined into a single 16-bit register, depending on the timers' mode configuration.

TH0 and TL0—Timer 0 high and low bytes.
SFR Address: 8CH and 8AH, respectively.
Power-On Default: 00H and 00H, respectively.

TH1 and TL1—Timer 1 high and low bytes.
SFR Address: 8DH and 8BH, respectively.
Power-On Default: 00H and 00H, respectively.

INTERRUPT SYSTEM

The ADuC845/ADuC847/ADuC848 provide nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE Interrupt Enable Register
IP Interrupt Priority Register
IEIP2 Secondary Interrupt Enable Register

IE—Interrupt Enable Register

SFR Address: A8H
Power-On Default: 00H
Bit Addressable: Yes

Table 58. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	Set by the user to enable External Interrupt 1 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 1 ($\overline{INT0}$).
1	ET0	Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	Set by the user to enable External Interrupt 0 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 0 ($\overline{INT0}$).

IP—Interrupt Priority Register

SFR Address: B8H
Power-On Default: 00H
Bit Addressable: Yes

Table 59. IP SFR Bit Designations

Bit No.	Name	Description
7	-----	Not Implemented. Write Don't Care.
6	PADC	ADC Interrupt Priority (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	PX1	$\overline{INT0}$ (External Interrupt 1) priority (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	PX0	$\overline{INT0}$ (External Interrupt 0) Priority (1 = High; 0 = Low).

as op amps and voltage reference) can be powered from the AV_{DD} supply line as well.

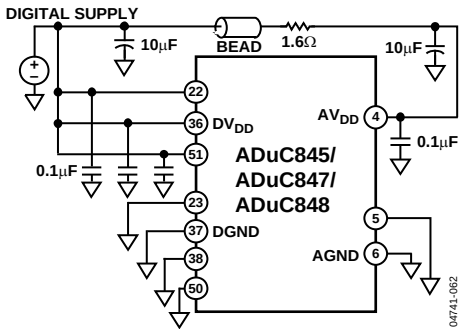

Figure 65. External Single-Supply Connections (56-Lead LFCSP Pin Numbering)

Notice that in both Figure 64 and Figure 65 a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local decoupling capacitors (0.1 µF) are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are closer than the 10 µF capacitors to each V_{DD} pin with lead lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that, at all times, the analog and digital ground pins on the device must be referenced to the same system ground reference point. It is recommended that the LFCSP paddle be soldered to ensure mechanical stability but be floated with respect to system V_{DD}s or grounds.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC845/ADuC847/ADuC848.

3 V Part

For DV_{DD} below 2.63 V, the internal POR holds the device in reset. As DV_{DD} rises above 2.63 V, an internal timer times out for typically 128 ms before the device is released from reset. The user must ensure that the power supply has at least reached a stable 2.7 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 66 illustrates the operation of the internal POR.

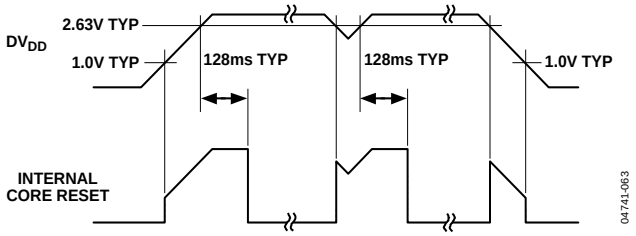

Figure 66. 3 V Part POR operation

5 V Part

For DV_{DD} below 4.5 V, the internal POR holds the device in reset. As DV_{DD} rises above 4.5 V, an internal timer times out for approximately 128 ms before the device is released from reset. The user must ensure that the power supply has reached a stable 4.75 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 67 illustrates this operation.

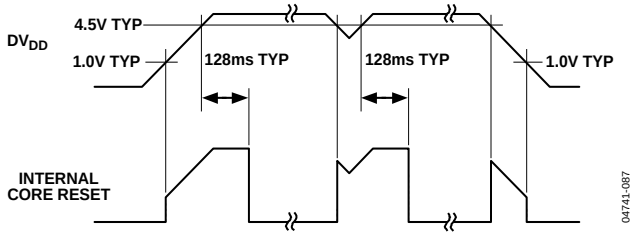

Figure 67. 5 V Part POR Operation

POWER CONSUMPTION

The DV_{DD} power supply current consumption is specified in normal and power-down modes. The AV_{DD} power supply current is specified with the analog peripherals disabled. The normal mode power consumption represents the current drawn from DV_{DD} by the digital core. The other on-chip peripherals (such as the watchdog timer and power supply monitor) consume negligible current and are therefore included with the normal operating current. The user must add any currents sourced by the parallel and serial I/O pins, and those sourced by the DAC to determine the total current needed at the ADuC845/ADuC847/ADuC848 DV_{DD} and AV_{DD} supply pins. Also, current drawn from the DV_{DD} supply increases by approximately 5 mA during Flash/EE erase and program cycles.

POWER-SAVING MODES

Setting the power-down mode bit, PCON.1, in the PCON SFR described in Table 6, allows the chip to be switched from normal mode into full power-down mode.

In power-down mode, both the PLL and the clock to the core are stopped. The on-chip oscillator can be halted or can continue to oscillate, depending on the state of the oscillator power-down bit (OSC_PD) in the PLLCON SFR. The TIC, driven directly from the oscillator, can also be enabled during power-down. However, all other on-chip peripherals are shut down. Port pins retain their logic levels in this mode, but the DAC output goes to a high impedance state (three-state) while ALE and $\overline{PSEN}$ outputs are held low. There are five ways to terminate power-down mode:

- **Asserting the RESET Pin**
  Returns to normal mode. All registers are set to their reset default value and program execution starts at the reset vector once the RESET pin is de-asserted.

QuickStart DEVELOPMENT SYSTEM

The QuickStart Development System is an entry-level, low cost development tool suite supporting the ADuC8xx MicroConverter product family. The system consists of the following PC-based (Windows®-compatible) hardware and software development tools:

Hardware:	Evaluation board and serial port programming cable.
Software:	Serial download software.
Miscellaneous:	CD-ROM documentation and prototype evaluation board.

A brief description of some of the software tools and components in the QuickStart system follows.

Download—In-Circuit Serial Downloader

The serial downloader is a Windows application that allows the user to serially download an assembled program (Intel® hexa-decimal format file) to the on-chip program flash memory via the serial COM port on a standard PC. The AN-1074 Application Note details this serial download protocol.

ASPIRE—IDE

The ASPIRE® integrated development environment is a Windows application that allows the user to compile, edit, and debug code in the same environment. The ASPIRE software allows users to debug code execution on silicon using the MicroConverter UART serial port. The debugger provides access to all on-chip peripherals during a typical debug session as well as single-step, animate (automatic single stepping), and break-point code execution control.

Note that the ASPIRE IDE is also included as part of the QuickStart-PLUS system. As part of the QuickStart-PLUS system the ASPIRE IDE also supports mixed level and C source debugging. This is not available in the QuickStart system where the program is limited to assembly only.

QuickStart-PLUS DEVELOPMENT SYSTEM

The QuickStart-PLUS development system offers users enhanced nonintrusive debug and emulation tools. The system consists of the following PC-based (Windows-compatible) hardware and software development tools:

Hardware:	Prototype Board, Accutron NonIntrusive Single-Pin Emulator.
Software:	ASPIRE Integrated Development Environment. Features full C and Assembly emulation using the Accutron single-pin emulator.
Miscellaneous:	CD-ROM documentation.

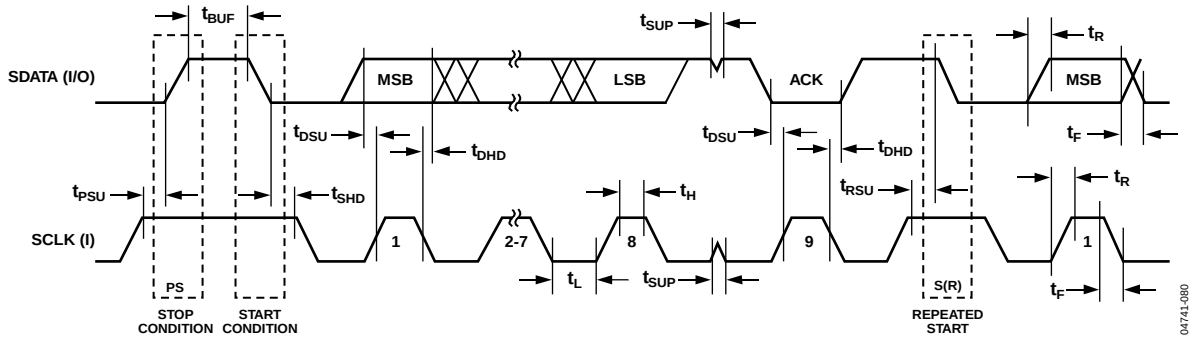

Figure 75. I²C-Compatible Interface Timing

Table 68. SPI MASTER MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		635		ns
t_{SH}	SCLOCK High Pulse Width[1]		635		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 1.57 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

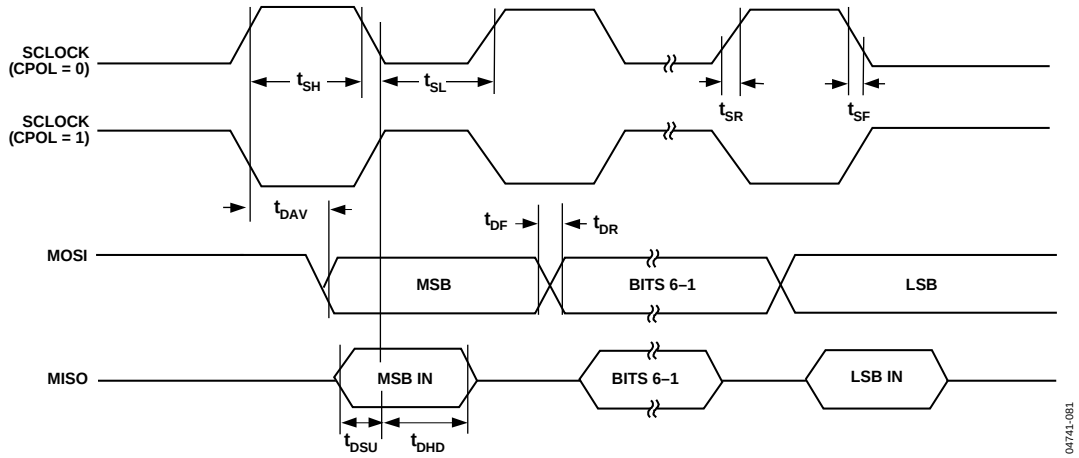

Figure 76. SPI Master Mode Timing (CHPA = 1)

Table 69. SPI MASTER MODE TIMING (CPHA = 0) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		635		ns
t_{SH}	SCLOCK High Pulse Width[1]		635		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DOSU}	Data Output Setup Before SCLOCK Edge			150	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 1.57 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

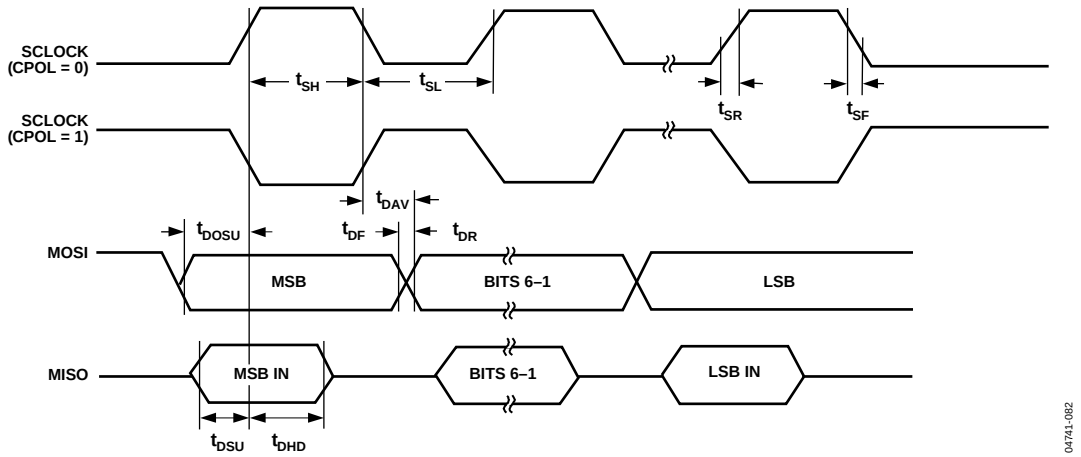

Figure 77. SPI Master Mode Timing (CHPA = 0)

Table 70. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

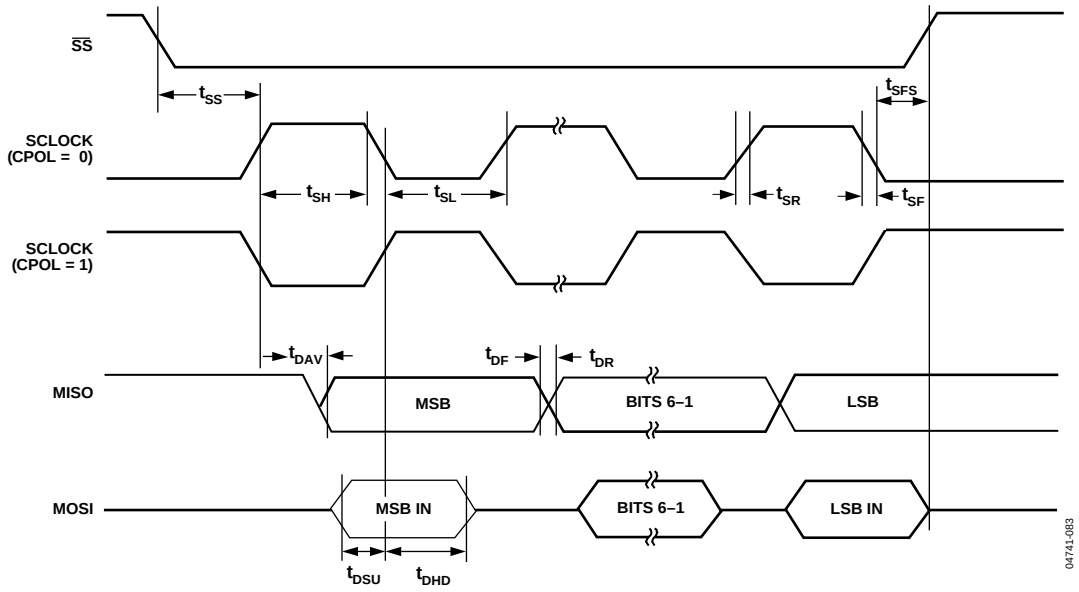

Figure 78. SPI Slave Mode Timing (CHPA = 1)