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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x24b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc847bsz8-3

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSDUCER BURNOUT CURRENT SOURCES					
AIN+ Current		−100		nA	AIN+ is the selected positive input (AIN4 or AIN6 only) to the primary ADC
AIN− Current		100		nA	AIN− is the selected negative input (AIN5 or AIN7 only) to the primary ADC
Initial Tolerance at 25°C		±10		%	
Drift		0.03		%/°C	
EXCITATION CURRENT SOURCES					
Output Current		200		µA	Available from each current source
Initial Tolerance at 25°C		±10		%	
Drift		200		ppm/°C	
Initial Current Matching at 25°C		±1		%	Matching between both current sources
Drift Matching		20		ppm/°C	
Line Regulation (AV_{DD})		1		µA/V	AV_{DD} = 5 V ± 5%
Load Regulation		0.1		µA/V	
Output Compliance[2]	AGND		AV_{DD} − 0.6	V	
POWER SUPPLY MONITOR (PSM)					
AV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
AV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
DV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
DV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)					
Logic Inputs, XTAL1 Only[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	3.5			V	DV_{DD} = 5 V
	2.5			V	DV_{DD} = 3 V
XTAL1 Input Capacitance		18		pF	
XTAL2 Output Capacitance		18		pF	
LOGIC INPUTS					
All Inputs Except SCLOCK, RESET, and XTAL1[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	2.0			V	
SCLOCK and RESET Only (Schmidt Triggered Inputs)[2]					
V_{T+}	1.3		3.0	V	DV_{DD} = 5 V
	0.95		2.5	V	DV_{DD} = 3 V
V_{T-}	0.8		1.4	V	DV_{DD} = 5 V
	0.4		1.1	V	DV_{DD} = 3 V
$V_{T+} - V_{T-}$	0.3		0.85	V	DV_{DD} = 5 V or 3 V
Input Currents					
Port 0, P1.0 to P1.7, $\overline{EA}$			±10	µA	V_{IN} = 0 V or V_{DD}
RESET			±10	µA	V_{IN} = 0 V, DV_{DD} = 5 V
	35		105	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V, internal pull-down
Port 2, Port 3			±10	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V
	−180		−660	µA	V_{IN} = 2 V, DV_{DD} = 5 V
	−20		−75	µA	V_{IN} = 0.45 V, DV_{DD} = 5 V
Input Capacitance		10		pF	All digital inputs

GENERAL DESCRIPTION

The ADuC845, ADuC847, and ADuC848 are single-cycle, 12.58 MIPs, 8052 core upgrades to the ADuC834 and ADuC836. They include additional analog inputs for applications requiring more ADC channels.

The ADuC845, ADuC847, and ADuC848 are complete smart transducer front ends. The family integrates high resolution Σ-Δ ADCs with flexible, up to 10-channel, input multiplexing, a fast 8-bit MCU, and program and data Flash/EE memory on a single chip.

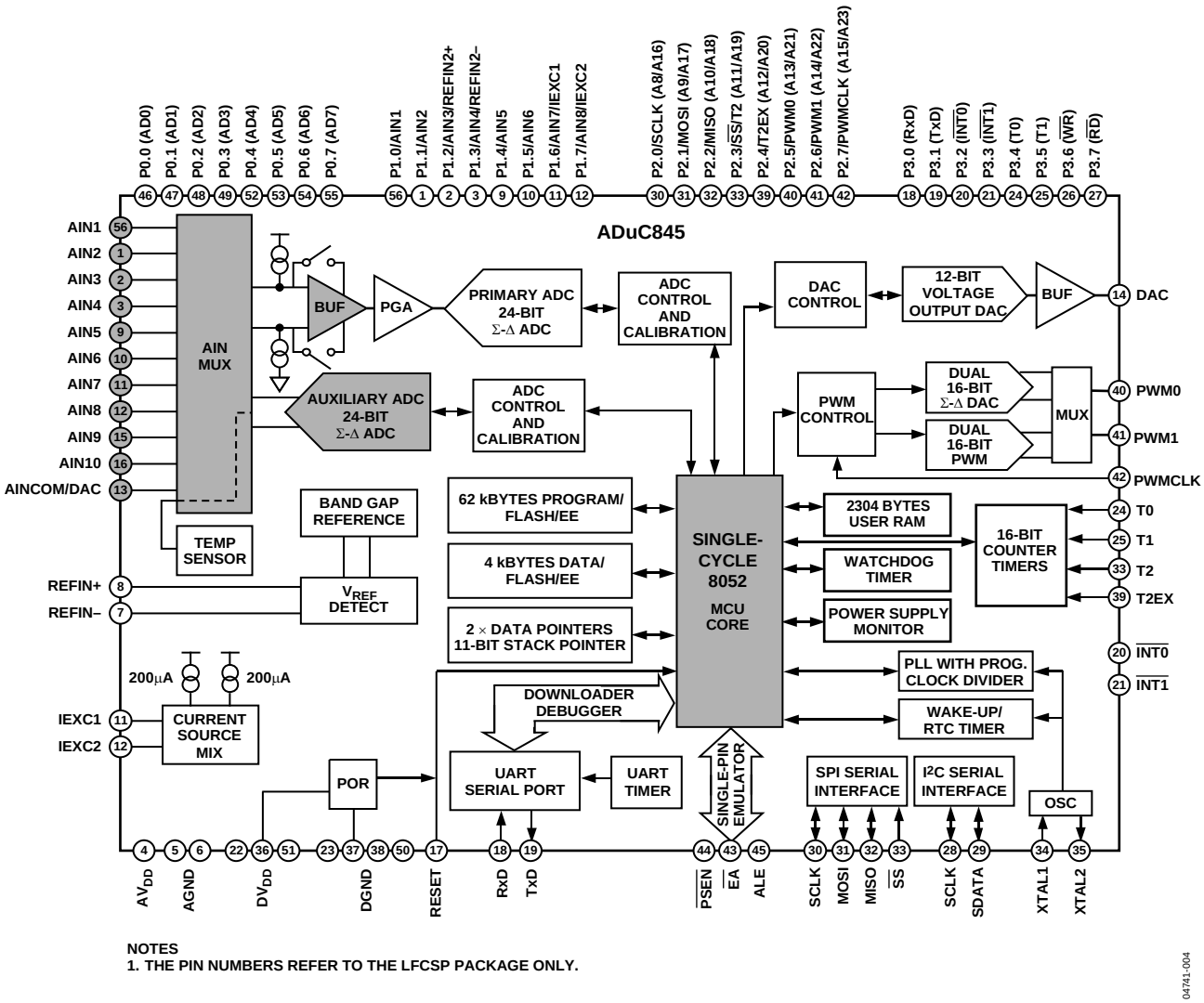
The ADuC845 includes two (primary and auxiliary) 24-bit Σ-Δ ADCs with internal buffering and PGA on the primary ADC. The ADuC847 includes the same primary ADC as the ADuC845 (auxiliary ADC removed). The ADuC848 is a 16-bit ADC version of the ADuC847.

The ADCs incorporate flexible input multiplexing, a temperature sensor (ADuC845 only), and a PGA (primary ADC only) allowing direct measurement of low-level signals. The ADCs include on-chip digital filtering and programmable output data rates that are intended for measuring wide dynamic range and low frequency signals, such as those in weigh scale, strain gage, pressure transducer, or temperature measurement applications.

The devices operate from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 12.58 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an optimized single-cycle 8052 offering up to 12.58 MIPs performance while maintaining 8051 instruction set compatibility.

The available nonvolatile Flash/EE program memory options are 62 kbytes, 32 kbytes, and 8 kbytes. 4 kbytes of nonvolatile Flash/EE data memory and 2304 bytes of data RAM are also provided on-chip. The program memory can be configured as data memory to give up to 60 kbytes of NV data memory in data logging applications.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the $\overline{EA}$ pin. The ADuC845, ADuC847, and ADuC848 are supported by the QuickStart™ development system featuring low cost software and hardware development tools.



NOTES
1. THE PIN NUMBERS REFER TO THE LFCSP PACKAGE ONLY.

Figure 4. Detailed Block Diagram of the ADuC845

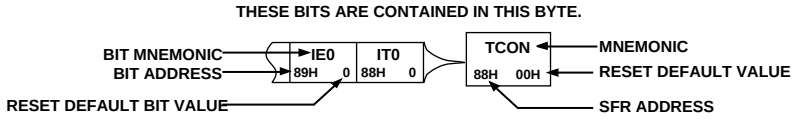
COMPLETE SFR MAP

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RS1 D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH 0	PT0 B9H 0	PX0 B8H 0	BITS
RD B7H 1	WR B6H 1	T1 B5H 1	T0 B4H 1	INT1 B3H 1	INT0 B2H 1	TxD B1H 1	RxD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	TI 99H 0	RI 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

SPICON F8H 05H	RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
B F0H 00H	RESERVED	I2CADD1 F2H 7FH	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
I2CCON E8H 00H	GN0L[2] E9H xxH	GN0M[2] EAH xxH	GN0H[2] EBH xxH	GN1L[2] ADuC845 ONLY ECH xxH	GN1H[2] ADuC845 ONLY EDH xxH	RESERVED	RESERVED
ACC E0H 00H	OF0L E1H xxH	OF0M E2H xxH	OF0H E3H xxH	OF1L ADuC845 ONLY E4H xxH	OF1H ADuC845 ONLY E5H xxH	ADC0CON2 E6H 00H	RESERVED
ADCSTAT D8H 00H	ADC0L NOT AVAILABLE ON ADuC848 D9H 00H	ADC0M DAH 00H	ADC0H DBH 00H	ADC1M ADuC845 ONLY DCH 00H	ADC1H ADuC845 ONLY DDH 00H	ADC1L ADuC845 ONLY DEH 00H	PSMCON DFH DEH
PSW D0H 00H	ADCMODE D1H 08H	ADC0CON1 D2H 07H	ADC1CON ADuC845 ONLY D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 53H
T2CON C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON C0H 10H	RESERVED	CHIPID C2H A0H	RESERVED	RESERVED	RESERVED	EDARL C6H 00H	EDARH C7H 00H
IP B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3 B0H FFH	PWM0L B1H 00H	PWM0H B2H 00H	PWM1L B3H 00H	PWM1H B4H 00H	RESERVED	RESERVED	SPH B7H 00H
IE A8H 00H	IEIP2 A9H A 0H	RESERVED	RESERVED	RESERVED	RESERVED	PWMCON AEH 00H	CFG845/7/8 AFH 00H
P2 A0H FFH	TIMECON A1H 00H	HTHSEC[1] A2H 00H	SEC[1] A3H 00H	MIN[1] A4H 00H	HOUR[1] A5H 00H	INTVAL A6H 00H	DPCON A7H 00H
SCON 98H 00H	SBUF 99H 00H	I2CDAT 9AH 00H	I2CADD 9BH 55H	RESERVED	T3FD 9DH 00H	T3CON 9EH 00H	EWAIT 9FH 00H
P1 90H FFH	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
TCON 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

[1] THESE SFRs MAINTAIN THEIR PRE-RESET VALUES AFTER A RESET IF TIMECON.0 = 1.
[2] CALIBRATION COEFFICIENTS ARE PRECONFIGURED ON POWER-UP TO FACTORY CALIBRATED VALUES.

SFR MAP KEY:



SFR NOTE:
SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT ADDRESSABLE.

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Figure 7. Complete SFR Map for the ADuC845, ADuC847, and ADuC848

Mnemonic	Description	Bytes	Cycles[1]
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2
MOV dir,A	Move A to direct byte	2	2
MOV Rn, dir	Move register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,@Ri	Move indirect to direct memory	2	2
MOV @Ri,dir	Move direct to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A	1	4
MOVX[2] A,@Ri	Move external (A8) data to A	1	4
MOVX[2] A,@DPTR	Move external (A16) data to A	1	4
MOVX[2] @Ri,A	Move A to external data (A8)	1	4
MOVX[2] @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit	OR direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3

ADC CIRCUIT INFORMATION

The ADuC845 incorporates two 10-channel (8-channel on the MQFP package) 24-bit Σ-Δ ADCs, while the ADuC847 and ADuC848 each incorporate a single 10-channel (8-channel on the MQFP package) 24-bit and 16-bit Σ-Δ ADC.

Each device also includes an on-chip programmable gain amplifier and configurable buffering (neither is available on the auxiliary ADC on the ADuC845). The devices also incorporate digital filtering intended for measuring wide dynamic range and low frequency signals such as those in weigh-scale, strain-gage, pressure transducer, or temperature measurement applications.

The ADuC845/ADuC847/ADuC848 can be configured as four or five (MQFP/LFCSP package) fully-differential input channels or as eight or ten (MQFP/LFCSP package) pseudo differential input channels referenced to AINCOM. The ADC on each device (primary only on the ADuC845) can be fully buffered internally, and can be programmed for one of eight input ranges from ±20 mV to ±2.56 V (V_{REF} × 1.024). Buffering the input channel means that the device can handle significant source impedances on the selected analog input and that RC filtering (for noise rejection or RFI reduction) can be placed on the analog inputs. If the ADC is used with internal buffering disabled (ADC0CON1.7 = 1, ADC0CON1.6 = 0), these unbuffered inputs provide a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the inputs can cause dc gain errors, depending on the output impedance of the source that is driving the ADC inputs.

Table 8 and Table 9 show the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 16-bit and 20-bit levels, respectively, is introduced. When used with internal buffering enabled, it is recommended that a capacitor (10 nF to 100 nF) be placed on the input to the ADC (usually as part of an antialiasing filter) to aid in noise performance.

The input channels are intended to convert signals directly from sensors without the need for external signal conditioning. With internal buffering disabled (relevant bits set/cleared in ADC0CON1), external buffering might be required.

When the internal buffer is enabled, it might be necessary to offset the negative input channel by +100 mV and to offset the positive channel by −100 mV if the reference range is AV_{DD}. This accounts for the restricted common-mode input range in the buffer. Some circuits, for example, bridge circuits, are inherently suitable to use without having to offset where the output voltage is balanced around $V_{REF}/2$ and is not sufficiently large to encroach on the supply rails. Internal buffering is not available on the auxiliary ADC (ADuC845 only). The auxiliary ADC (ADuC845 only) is fixed at a gain range of ±2.50 V.

The ADCs use a Σ-Δ conversion technique to realize up to 24 bits on the ADuC845 and the ADuC847, and up to 16 bits on the ADuC848 of no missing codes performance (20 Hz update rate, chop enabled). The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A $sinc^3$ programmable low-pass filter (see Table 28) is then used to decimate the modulator output data stream to give a valid data conversion result at programmable output rates. The signal chain has two modes of operation, chop enabled and chop disabled. The $\overline{CHOP}$ bit in the ADCMODE register enables or disables the chopping scheme.

Table 8. Maximum Resistance for No 16-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	111.3 kΩ	27.8 kΩ	16.7 kΩ	4.5 kΩ	2.58 kΩ	700 Ω
2	53.7 kΩ	13.5 kΩ	8.1 kΩ	2.2 kΩ	1.26 kΩ	360 Ω
4	25.4 kΩ	6.4 kΩ	3.9 kΩ	1.0 kΩ	600 Ω	170 Ω
8–128	10.7 kΩ	2.9 kΩ	1.7 kΩ	480 Ω	270 Ω	75 Ω

Table 9. Maximum Resistance for No 20-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	84.9 kΩ	21.1 kΩ	12.5 kΩ	3.2 kΩ	1.77 kΩ	440 Ω
2	42.0 kΩ	10.4 kΩ	6.1 kΩ	1.6 kΩ	880 Ω	220 Ω
4	20.5 kΩ	5.0 kΩ	2.9 kΩ	790 Ω	430 Ω	110 Ω
8–128	8.8 kΩ	2.3 k Ω	1.3 k Ω	370 Ω	195 Ω	50 Ω

This offset is removed by performing a running average of 2. This average by 2 means that the settling time to any change in programming of the ADC is twice the normal conversion time, while an asynchronous step change on the analog input is not fully reflected until the third subsequent output. See Figure 13.

$$t_{SETTLE} = \frac{2}{f_{ADC}} = 2 \times t_{ADC}$$

The allowable range for SF (chop enabled) is 13 to 255 with a default of 69 (45H). The corresponding conversion rates, rms and peak-to-peak noise performances are shown in Table 10, Table 11, Table 12, and Table 13. The numbers are typical and generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. Note that the conversion time increases by 0.732 ms for each increment in SF.

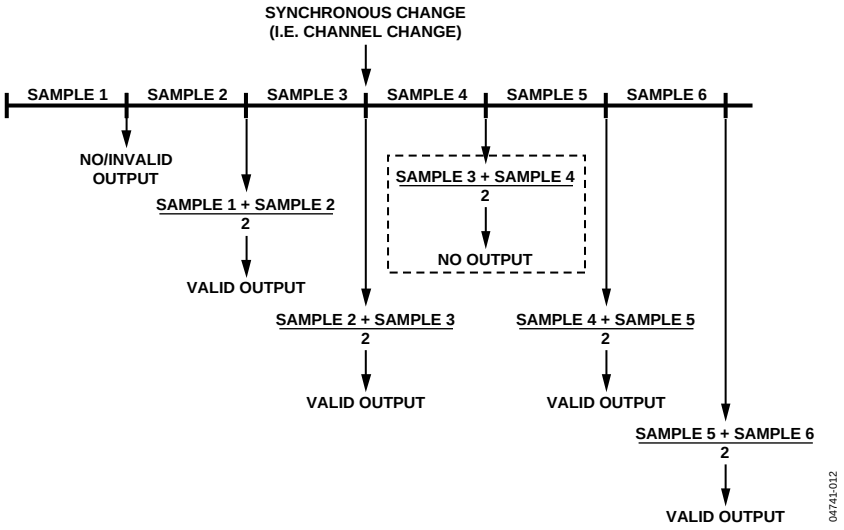

Figure 13. ADC Settling Time Following a Synchronous Change with Chop Enabled

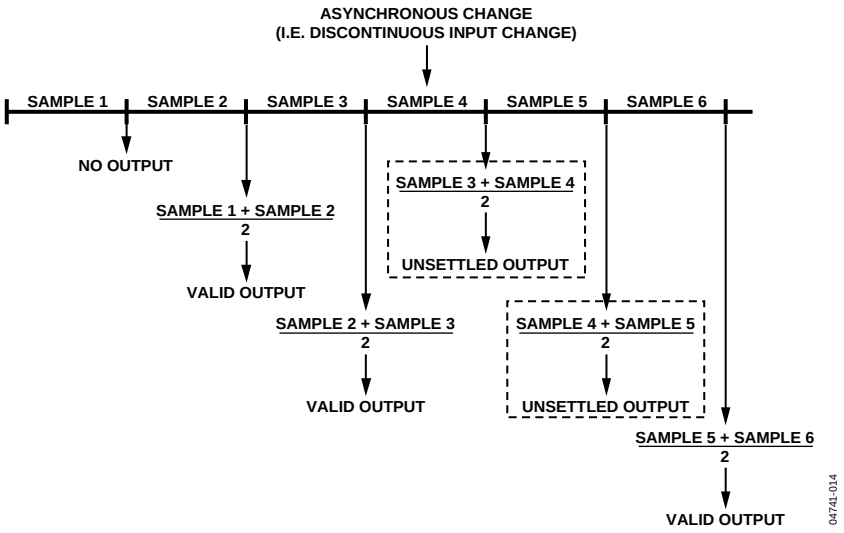

Figure 14. ADC Settling Time Following an Asynchronous Change with Chop Enabled

AUXILIARY ADC (ADUC845 ONLY)

Table 18. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Enabled

SF Word	Data Update Rate (Hz)	μV
13	105.03	17.46
23	59.36	3.13
27	50.56	4.56
69	19.79	2.66
255	5.35	1.13

Table 19. ADuC845 Typical Peak-to-Peak Resolution (Bits) vs. Update Rate[1] with Chop Enabled

SF Word	Data Update Rate (Hz)	Bits
13	105.03	15.5
23	59.36	18
27	50.56	17.5
69	19.79	18
255	5.35	19.5

[1] ADC converting in bipolar mode.

Table 20. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	μV
3	1365.33	1386.58
13	315.08	34.94
66	62.06	3.2
69	59.36	3.19
81	50.57	3.14
255	16.06	1.71

Table 21. ADuC845 Peak-to-Peak Resolution (Bits) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Bits
3	1365.33	9
13	315.08	14.5
66	62.06	18
69	59.36	18
81	50.57	18
255	16.06	19

REFERENCE INPUTS

The ADuC845/ADuC847/ADuC848 each have two separate differential reference inputs, REFIN± and REFIN2±. While both references are available for use with the primary ADC, only REFIN± is available for the auxiliary ADC (ADuC845 only). The common-mode range for these differential references is from AGND to AV_{DD}. The nominal external reference voltage is 2.5 V, with the primary and auxiliary (ADuC845 only) reference select bits configured from the ADC0CON2 and ADC1CON (ADuC845 only), respectively.

When an external reference voltage is used, the primary ADC sees this internally as a 2.56 V reference ($V_{REF} \times 1.024$). Therefore, any calculations of LSB size should account for this. For instance, with a 2.5 V external reference connected and using a gain of 1 on a unipolar range (2.56 V), the LSB size is $(2.56/2^{24}) = 152.6$ nV (if using the 24-bit ADC on the ADuC845 or ADuC847). If a bipolar gain of 4 is used (±640 mV), the LSB size is $(±640 \text{ mV})/2^{24}) = 76.3$ nV (again using the 24-bit ADC on the ADuC845 or ADuC847).

The ADuC845/ADuC847/ADuC848 can also be configured to use the on-chip band gap reference via the XREF0/1 bits in the ADC0CON2 SFR (for primary ADC) or the AXREF bit in ADC1CON (for auxiliary ADC (ADuC845 only)). In this mode of operation, the ADC sees the internal reference of 1.25 V, thereby halving all the input ranges. A consequence of using the internal band gap reference is a noticeable degradation in peak-to-peak resolution. For this reason, operation with an external reference is recommended.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference inputs for the device, the effect of any low frequency noise in the excitation source is removed because the application is ratiometric. If the devices are not used in a ratiometric configuration, use a low noise reference. Recommended reference voltage sources for the ADuC845/ADuC847/ADuC848 include the ADR421, REF43, and REF192.

The reference inputs provide a high impedance, dynamic load to external connections. Because the impedance of each reference input is dynamic, resistor/capacitor combinations on these pins can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources, such as those mentioned above, for example, the ADR421, typically have low output impedances, and, therefore, decoupling capacitors on the REFIN± or REFIN2± inputs would be recommended (typically 0.1 μF). Deriving the reference voltage from an external resistor configuration means that the reference input sees a significant external source impedance. External decoupling of the REFIN± and/or REFIN2± inputs is not recommended in this type of configuration.

BURNOUT CURRENT SOURCES

The primary ADC on the ADuC845 and the ADC on the ADuC847 and ADuC848 incorporate two 100 nA constant current generators that are used to detect a failure in a connected sensor. One sources current from the AV_{DD} to AIN(+), and one sinks current from AIN(−) to AGND. These currents are only configurable for use on AIN5/AIN6 and/or AIN7/AIN8 in differential mode only, from the ICON.6 bit in the ICON SFR

that the internal calibration procedure for full-scale calibration automatically selects the reference in voltage at PGA = 1.

Therefore, the full-scale endpoint calibration automatically subtracts the offset calibration error, it is advisable to perform an offset calibration at the same gain range as that used for full-scale calibration. There is no penalty to the full-scale calibration in redoing the zero-scale calibration at the required PGA range because the full-scale calibration has very good matching at all the PGA ranges.

This procedure also applies when chop is disabled.

Note that for internal calibration to be effective, the AIN− pin should be held at a steady voltage, within the allowable common-mode range to keep it from floating during calibration.

System Calibration Example

With chop enabled, a system zero-scale or offset calibration should never be required. However, if a full-scale or gain calibration is required for any reason, use the following typical procedure for doing so.

1. Apply a differential voltage of 0 V to the selected analog inputs (AIN+ to AIN−) that are held at a common-mode voltage.

   Perform a system zero-scale or offset calibration by setting the MD2...0 bits in the ADCMODE register to 110B.

2. Apply a full-scale differential voltage across the ADC inputs again at the same common-mode voltage.

   Perform a system full-scale or gain calibration by setting the MD2...0 bits in the ADCMODE register to 111B.

Perform a system calibration at the required PGA range to be used since the ADC scales to the differential voltages that are applied to the ADC during the calibration routines.

In bipolar mode, the zero-scale calibration determines the mid-scale point of the ADC (800000H) or 0 V.

PROGRAMMABLE GAIN AMPLIFIER

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different ranges, which are programmed via the range bits (RN0 to RN2) in the ADC0CON1 register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V and 0 V to 2.56 V, while in bipolar mode the ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±64 0 mV, ±1.28 V, and ±2.56 V. These ranges should appear on the input to the on-chip PGA. The ADC range-matching specification of 2 µV (typical with chop enabled) means that calibration need only be carried out on a single range and need not be repeated when the ADC range is changed. This is a significant advantage compared to similar mixed-signal solutions available on the market. The auxiliary (ADuC845 only) ADC does not incorporate a PGA, and the gain is fixed at 0 V to 2.50 V in unipolar mode, and ±2.50 V in bipolar mode.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog inputs of the ADuC845/ADuC847/ADuC848 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the device can handle negative voltages with respect to system AGND, but rather with respect to the negative reference input. Unipolar and bipolar signals on the AIN(+) input on the ADC are referenced to the voltage on the respective AIN(−) input. AIN(+) and AIN(−) refer to the signals seen by the ADC.

For example, if AIN(−) is biased to 2.5 V (tied to the external reference voltage) and the ADC is configured for a unipolar analog input range of 0 mV to >20 mV, the input voltage range on AIN(+) is 2.5 V to 2.52 V. On the other hand, if AIN(−) is biased to 2.5 V (again the external reference voltage) and the ADC is configured for a bipolar analog input range of ±1.28 V, the analog input range on the AIN(+) is 1.22 V to 3.78 V, that is, 2.5 V ± 1.28 V.

The modes of operation for the ADC are fully differential mode or pseudo differential mode. In fully differential mode, AIN1 to AIN2 are one differential pair, and AIN3 to AIN4 are another pair (AIN5 to AIN6, AIN7 to AIN8, and AIN9 to AIN10 are the others). In differential mode, all AIN(−) pin names imply the negative analog input of the selected differential pair, that is, AIN2, AIN4, AIN6, AIN8, AIN10. The term AIN(+) implies the positive input of the selected differential pair, that is, AIN1, AIN3, AIN5, AIN7, AIN9. In pseudo differential mode, each analog input is paired with the AINCOM pin, which can be biased up or tied to AGND. In this mode, the AIN(−) implies AINCOM, and AIN(+) implies any one of the ten analog input channels.

The configuration of the inputs (unipolar vs. bipolar) is shown in Figure 17.

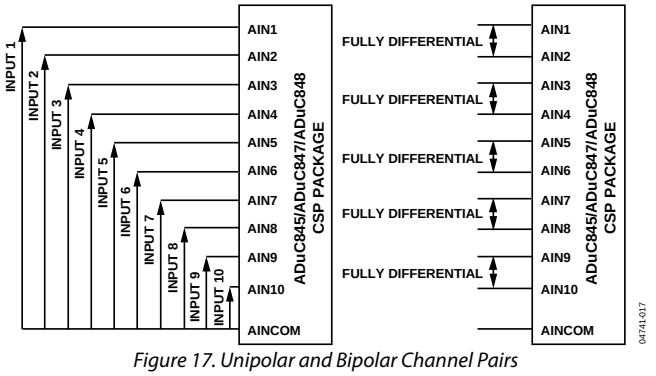

Figure 17. Unipolar and Bipolar Channel Pairs

ADCSTAT (ADC STATUS REGISTER)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including REFIN± reference detect and conversion overflow/underflow flags.

SFR Address: D8H
Power-On Default: 00H
Bit Addressable: Yes

Table 23. ADCSTAT SFR Bit Designation

Bit No.	Name	Description
7	RDY0	Ready Bit for the Primary ADC. Set by hardware on completion of conversion or calibration. Cleared directly by the user, or indirectly by a write to the mode bits, to start calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary (ADuC845 only) ADC. Same definition as RDY0 referred to the auxiliary ADC. Valid on the ADuC845 only.
5	CAL	Calibration Status Bit. Set by hardware on completion of calibration. Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration. Note that calibration with the temperature sensor selected (auxiliary ADC on the ADuC845 only) fails to complete.
4	NOXREF	No External Reference Bit (only active if primary or auxiliary (ADuC845 only) ADC is active). Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When set, conversion results are clamped to all 1s. Only detects invalid REFIN±, does not check REFIN2±. Cleared to indicate valid V_{REF}.
3	ERR0	Primary ADC Error Bit. Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC. Valid on the ADuC845 only.
1	–––	Not Implemented. Write Don't Care.
0	–––	Not Implemented. Write Don't Care.

ICON (EXCITATION CURRENT SOURCES CONTROL REGISTER)

The ICON register is used to configure the current sources and the burnout detection source.

SFR Address: D5H
Power-On Default: 00H
Bit Addressable: No

Table 30. Excitation Current Source SFR Bit Designations

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	ICON.6	Burnout Current Enable Bit. When set, this bit enables the sensor burnout current sources on primary ADC channels AIN5/AIN6 or AIN7/AIN8. Not available on any other ADC input pins or on the auxiliary ADC (ADuC845 only).
5	ICON.5	Not Implemented. Write Don't Care.
4	ICON.4	Not Implemented. Write Don't Care.
3	ICON.3	IEXC2 Pin Select. 0 selects AIN8, 1 selects AIN7
2	ICON.2	IEXC1 Pin Select. 0 selects AIN7, 1 selects AIN8
1	ICON.1	IEXC2 Enable Bit (0 = disable).
0	ICON.0	IEXC1 Enable Bit (0 = disable).

A write to the ICON register has an immediate effect but does not reset the ADCs. Therefore, if a current source is changed while an ADC is already converting, the user must wait until the third or fourth output at least (depending on the status of the chop mode) to see a fully settled new output.

Both IEXC1 and IEXC2 can be configured to operate on the same output pin thereby increasing the current source capability to 400 μA.

USER DOWNLOAD MODE (ULOAD)

Figure 28 shows that it is possible to use the 62 kbytes of Flash/EE program memory available to the user as one single block of memory. In this mode, all the Flash/EE memory is read-only to user code.

However, most of the Flash/EE program memory can also be written to during run time simply by entering ULOAD mode. In ULOAD mode, the lower 56 kbytes of program memory can be erased and reprogrammed by the user software as shown in Figure 30. ULOAD mode can be used to upgrade the code in the field via any user-defined download protocol. By configuring the SPI port on the ADuC845/ADuC847/ADuC848 as a slave, it is possible to completely reprogram the 56 kbytes of Flash/EE program memory in under 5 s (see the AN-1074 Application Note).

Alternatively, ULOAD mode can be used to save data to the 56 kbytes of Flash/EE memory. This can be extremely useful in data logging applications where the devices can provide up to 60 kbytes of data memory on-chip (4 kbytes of dedicated Flash/EE data memory also exist).

The upper 6 kbytes of the 62 kbytes of Flash/EE program memory (8 kbytes on the 32-kbyte parts) are programmable only via serial download or parallel programming. This means that this space appears as read-only to user code; therefore, it cannot be accidentally erased or reprogrammed by erroneous code execution, making it very suitable to use the 6 kbytes as a bootloader. A bootload enable option exists in the Windows® serial downloader (WSD) to "Always RUN from E000H after Reset." If using a bootloader, this option is recommended to ensure that the bootloader always executes correct code after reset.

Programming the Flash/EE program memory via ULOAD mode is described in the Flash/EE Memory Control SFR section of ECON and also in the AN-1074 Application Note.

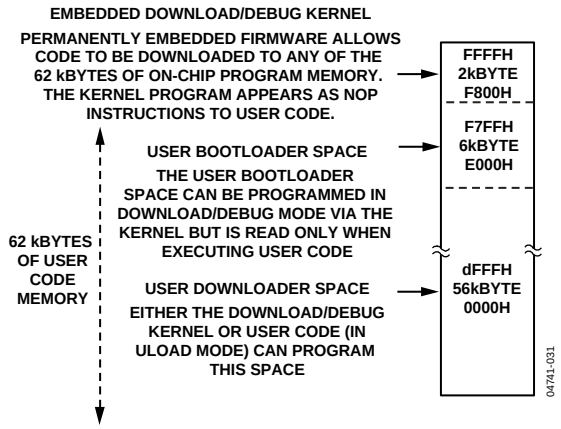

Figure 30. Flash/EE Program Memory Map in ULOAD Mode (62-kbyte Part)

The 32-kbyte memory parts have the user bootload space starting at 6000H. The memory mapping is shown in Figure 31.

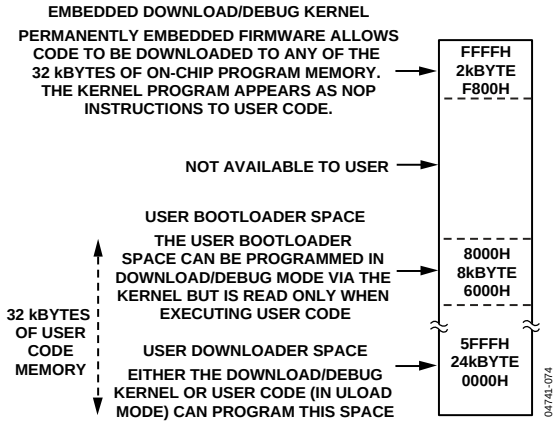

Figure 31. Flash/EE Program Memory Map in ULOAD Mode (32-kbyte Part)

ULOAD mode is not available on the 8-kbyte Flash/EE program memory parts.

Flash/EE Program Memory Security

The ADuC845/ADuC847/ADuC848 facilitate three modes of Flash/EE program memory security: the lock, secure, and serial safe modes. These modes can be independently activated, restricting access to the internal code space. They can be enabled as part of serial download protocol, as described in the AN-1074 Application Note, or via parallel programming.

Lock Mode

This mode locks the code memory, disabling parallel programming of the program memory. However, reading the memory in parallel mode and reading the memory via a MOVC command from external memory are still allowed. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Secure Mode

This mode locks the code memory, disabling parallel programming of the program memory. Reading/verifying the memory in parallel mode and reading the internal memory via a MOVC command from external memory are also disabled. This mode is deactivated by initiating an ERASE CODE AND DATA command in serial download or parallel programming modes.

Serial Safe Mode

This mode disables serial download capability on the device. If serial safe mode is activated and an attempt is made to reset the device into serial download mode, that is, RESET asserted (pulled high) and de-asserted (pulled low) with $\overline{\text{PSEN}}$ low, the device interprets the serial download reset as a normal reset only. It therefore does not enter serial download mode, but executes only a normal reset sequence. Serial safe mode can be disabled only by initiating an ERASE CODE AND DATA command in parallel programming mode.

Table 36. PWM0L: PWM Pulse Width Low Byte

PWM0L.7	PWM0L.6	PWM0L.5	PWM0L.4	PWM0L.3	PWM0L.2	PWM0L.1	PWM0L.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Cycle Width High Byte (PWM1H)

SFR Address: B4H
Power-On Default: 00H
Bit Addressable: No

Table 37. PWM1H: PWM Cycle Width High Byte

PWM1H.7	PWM1H.6	PWM1H.5	PWM1H.4	PWM1H.3	PWM1H.2	PWM1H.1	PWM1H.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Cycle Width Low Byte (PWM1L)

SFR Address: B3H
Power-On Default: 00H
Bit Addressable: No

Table 38. PWM1L: PWM Cycle Width Low Byte

PWM1L.7	PWM1L.6	PWM1L.5	PWM1L.4	PWM1L.3	PWM1L.2	PWM1L.1	PWM1L.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Mode 0

In Mode 0, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal digital I/Os.

Mode 1 (Single-Variable Resolution PWM)

In Mode 1, both the pulse length and the cycle time (period) are programmable in user code, allowing the resolution of the PWM to be variable. PWM1H/L sets the period of the output waveform. Reducing PWM1H/L reduces the resolution of the PWM output but increases the maximum output rate of the PWM. For example, setting PWM1H/L to 65536 gives a 16-bit PWM with a maximum output rate of 192 Hz (12.583 MHz/65536). Setting PWM1H/L to 4096 gives a 12-bit PWM with a maximum output rate of 3072 Hz (12.583 MHz/4096).

PWM0H/L sets the duty cycle of the PWM output waveform as shown in Figure 39.

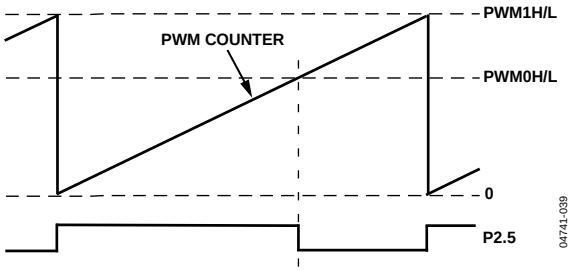

Figure 39. PWM in Mode 1

Mode 2 (Twin 8-Bit PWM)

In Mode 2, the duty cycle and the resolution of the PWM outputs are programmable. The maximum resolution of the PWM output is 8 bits.

PWM1L sets the period for both PWM outputs. Typically, this is set to 255 (FFH) to give an 8-bit PWM, although it is possible to reduce this as necessary. A value of 100 can be loaded here to give a percentage PWM, that is, the PWM is accurate to 1%.

Mode 5 (Dual 8-Bit PWM)

In Mode 5, the duty cycle and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

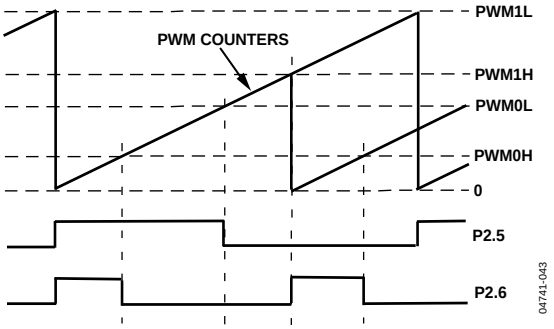

Figure 43. PWM Mode 5

Mode 6 (Dual RZ 16-Bit Σ-Δ DAC)

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4; however, the key difference is that Mode 6 provides return to zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. RZ mode ensures that any difference in the rise and fall times does not affect the Σ-Δ DAC INL. However, RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V– to AV_{DD} down to 0 V to $AV_{DD}/2$. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three full clocks (3 × 80 ns), high for one-half a clock (40 ns), and then low again for one-half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

The output resolution is set by the PWM1L and PWM1H SFRs for the P2.5 and P2.6 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P2.5 and P2.6, respectively. Both PWMs have the same clock source and clock divider.

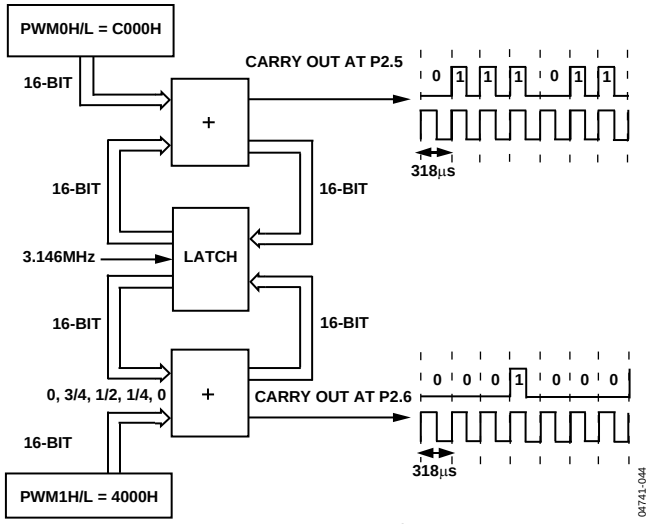

Figure 44. PWM Mode 6

Mode 7

In Mode 7, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal.

$\overline{SS}$ (Slave Select Input Pin)

Pin 31 (MQFP Package), Pin 33 (LFCSP Package)
The $\overline{SS}$ pin is used only when the ADuC845/ADuC847/ADuC848 are configured in SPI slave mode. This line is active low. Data is received or transmitted in slave mode only when the $\overline{SS}$ pin is low, allowing the devices to be used in single-master, multislave SPI configurations. If CPHA = 1, the $\overline{SS}$ input can be pulled low permanently. If CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte-wide transmission or reception and must return high again after the last bit in that byte-wide transmission or reception. In SPI slave mode, the logic level on the external $\overline{SS}$ pin (Pin 31/Pin 33) can be read via the SPR0 bit in the SPICON SFR.

The SFR register in Table 41 is used to control the SPI interface.

USING THE SPI INTERFACE

Depending on the configuration of the bits in the SPICON SFR shown in Table 41, the SPI interface transmits or receives data in a number of possible modes. Figure 46 shows all possible ADuC845/ADuC847/ADuC848 SPI configurations and the timing relationships and synchronization among the signals involved. Also shown in this figure is the SPI interrupt bit (ISPI) and how it is triggered at the end of each byte-wide communication.

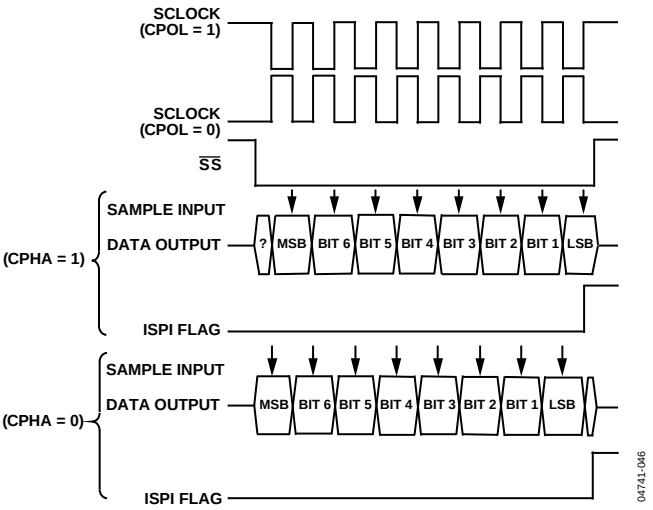

Figure 46. SPI Timing, All Modes

SPI Interface—Master Mode

In master mode, the SCLOCK pin is always an output and generates a burst of eight clocks whenever user code writes to the SPIDAT register. The SCLOCK bit rate is determined by SPR0 and SPR1 in SPICON. Also note that the $\overline{SS}$ pin is not used in master mode. If the devices need to assert the $\overline{SS}$ pin on an external slave device, use a port digital output pin.

In master mode, a byte transmission or reception is initiated by a byte write to SPIDAT. The hardware automatically generates eight clock periods via the SCLOCK pin, and the data is transmitted via MOSI. With each SCLOCK period, a data bit is also sampled via MISO. After eight clocks, the transmitted byte is completely transmitted (via MOSI), and the input byte (if required) is waiting in the input shift register (after being received via MISO). The ISPI flag is set automatically, and an interrupt occurs if enabled. The value in the input shift register is latched into SPIDAT.

SPI Interface—Slave Mode

In slave mode, the SCLOCK is an input. The $\overline{SS}$ pin must also be driven low externally during the byte communication. Transmission is also initiated by a write to SPIDAT. In slave mode, a data bit is transmitted via MISO, and a data bit is received via MOSI through each input SCLOCK period. After eight clocks, the transmitted byte is completely transmitted, and the input byte is waiting in the input shift register. The ISPI flag is set automatically, and an interrupt occurs, if enabled. The value in the shift register is latched into SPIDAT only when the transmission/reception of a byte has been completed. The end of transmission occurs after the eighth clock has been received if CPHA = 1, or when $\overline{SS}$ returns high if CPHA = 0.

IEIP2—Secondary Interrupt Enable Register

SFR Address: A9H
Power-On Default: A0H
Bit Addressable: No

Table 60. IEIP2 Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	PTI	Time Interval Counter Interrupt Priority Setting (1 = High, 0 = Low).
5	PPSM	Power Supply Monitor Interrupt Priority Setting (1 = High, 0 = Low).
4	PSI	SPI/I²C Interrupt Priority Setting (1 = High, 0 = Low).
3	----	This bit must contain 0.
2	ETI	Set by the user to enable the time interval counter interrupt. Cleared by the user to disable the time interval counter interrupt.
1	EPSMI	Set by the user to enable the power supply monitor interrupt. Cleared by the user to disable the power supply monitor interrupt.
0	ESI	Set by the user to enable the SPI/I²C serial port interrupt. Cleared by the user to disable the SPI/I²C serial port interrupt.

INTERRUPT PRIORITY

The interrupt enable registers are written by the user to enable individual interrupt sources; the interrupt priority registers allow the user to select one of two priority levels for each interrupt. A high priority interrupt can interrupt the service routine of a low priority interrupt, and if two interrupts of different priorities occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, the polling sequence, as shown in Table 61, is observed.

Table 61. Priority within Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt
WDS	2	Watchdog Timer Interrupt
IE0	2	External Interrupt 0
RDY0/RDY1	3	ADC Interrupt
TF0	4	Timer/Counter 0 Interrupt
IE1	5	External Interrupt 1
TF1	6	Timer/Counter 1 Interrupt
ISPI/I2CI	7	SPI/I²C Interrupt
RI/TI	8	UART Serial Port Interrupt
TF2/EXF2	9	Timer/Counter 2 Interrupt
TII	11 (Lowest)	Timer Interval Counter Interrupt

INTERRUPT VECTORS

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 62.

Table 62. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
RDY0/RDY1 (ADuC845 only)	0033H
ISPI/I2CI	003BH
PSMI	0043H
TII	0053H
WDS	005BH

Table 70. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

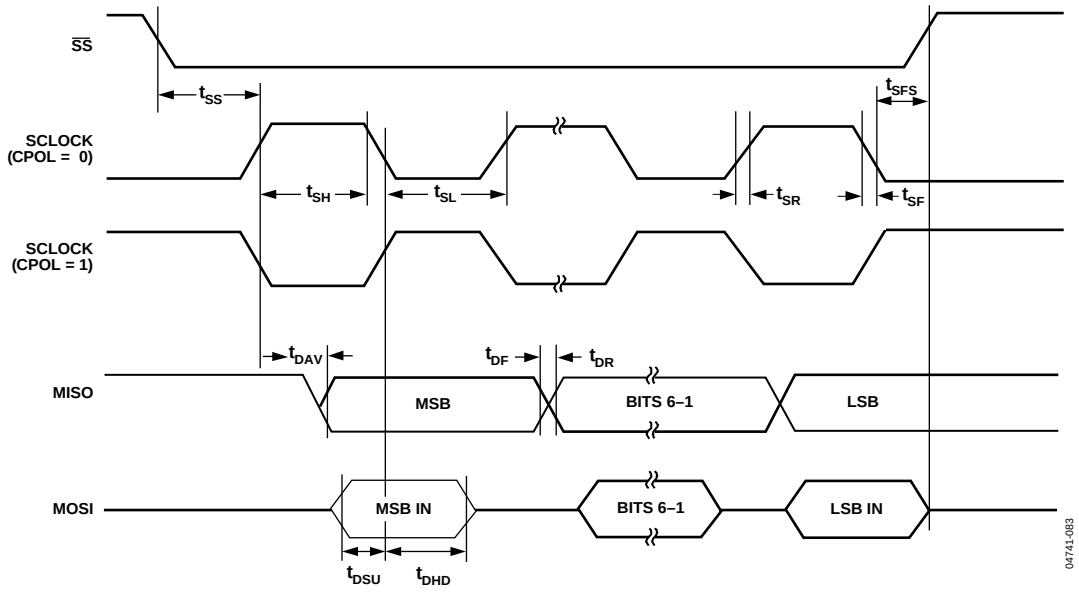

Figure 78. SPI Slave Mode Timing (CHPA = 1)

Table 72. UART TIMING (SHIFT REGISTER MODE) Parameter

		12.58 MHz Core_Clk			Variable Core_Clk			
		Min	Typ	Max	Min	Typ	Max	Unit
TXLXL	Serial Port Clock Cycle Time		954			$12t_{core}$		ns
TQVXH	Output Data Setup to Clock	662						ns
TDVXH	Input Data Setup to Clock	292						ns
TXHDX	Input Data Hold After Clock	0						ns
TXHQX	Output Data Hold After Clock	22						ns

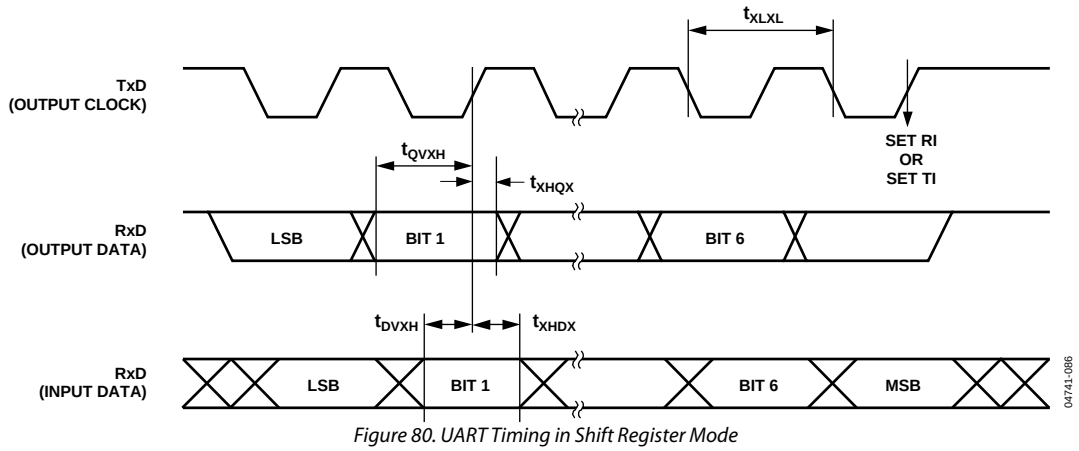

Figure 80. UART Timing in Shift Register Mode

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADuC845BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC845BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC845BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC845BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC845BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC845BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC847BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC847BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC847BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC847BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC847BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC847BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC847BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC847BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC847BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC847BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC848BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC848BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC848BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC848BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC848BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC848BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC848BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC848BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC848BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC848BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
EVAL-ADuC845QSZ		QuickStart Development System	
EVAL-ADuC845QSPZ		QuickStart-PLUS Development System	
EVAL-ADuC847QSZ		QuickStart Development System	
EVAL-ADUC-CABLE1Z		ADuC Serial Downloader Cable for UART	

[1] The -3 and -5 in the Model column indicate the DV_{DD} operating voltage.
[2] Z = RoHS Compliant Part.
[3] The QuickStart Plus system can only be ordered directly from Accutron. It can be purchased from the website http://www.accutron.com.