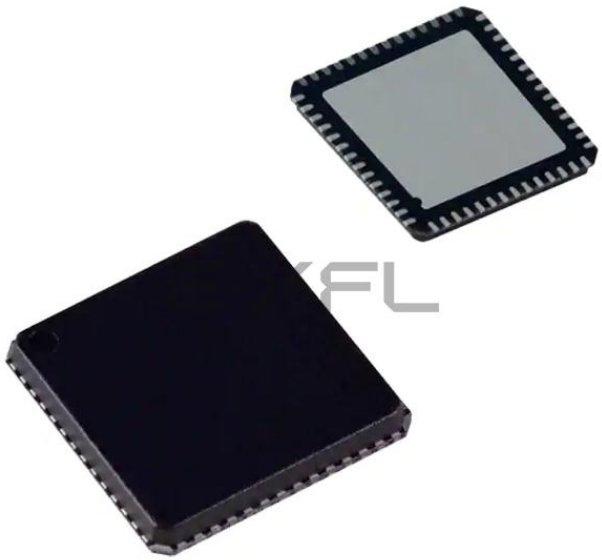

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x16b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc848bcpz62-3

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Normal Mode Rejection 50 Hz/60 Hz[2]					
On AIN	75			dB	50 Hz/60 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off
Analog Input Current[2]			±1	nA	T_{MAX} = 85°C, buffer on
			±5	nA	T_{MAX} = 125°C, buffer on
Analog Input Current Drift		±5		pA/°C	T_{MAX} = 85°C, buffer on
		±15		pA/°C	T_{MAX} = 125°C, buffer on
Average Input Current		±125		nA/V	±2.56 V range, buffer bypassed
Average Input Current Drift		±2		pA/V/°C	Buffer bypassed
Absolute AIN Voltage Limits[2]	A_{GND} + 0.1		AV_{DD} − 0.1	V	AIN1 … AIN10 and AINCOM with buffer enabled
Absolute AIN Voltage Limits[2]	A_{GND} − 0.03		AV_{DD} + 0.03	V	AIN1 … AIN10 and AINCOM with buffer bypassed
EXTERNAL REFERENCE INPUTS					
REFIN(+) to REFIN(–) Voltage		2.5		V	REFIN refers to both REFIN and REFIN2
REFIN(+) to REFIN(–) Range[2]	1		AV_{DD}	V	REFIN refers to both REFIN and REFIN2
Average Reference Input Current		±1		µA/V	Both ADCs enabled
Average Reference Input Current Drift		±0.1		nA/V/°C	
NOXREF Trigger Voltage	0.3		0.65	V	NOXREF (ADCSTAT.4) bit active if V_{REF} > 0.3 V, and inactive if V_{REF} > 0.65 V
Common-Mode Rejection					
DC Rejection		125		dB	AIN = 1 V, range = ±2.56 V
50 Hz/60 Hz Rejection[2]	90			dB	50 Hz/60 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 82
Normal Mode Rejection 50 Hz/60 Hz[2]	75			dB	50 Hz/60 Hz ±1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, AIN = 1 V, range = ±2.56 V, SF = 52H, chop off
AUXILIARY ADC (ADuC845 Only)					
Conversion Rate	5.4		105	Hz	Chop on
	16.06		1365	Hz	Chop off
No Missing Codes[2]	24			Bits	≤26.7 Hz update rate, chop enabled
	24			Bits	80.3 Hz update rate, chop disabled
Resolution	See Table 19 and Table 21				
Output Noise	See Table 18 and Table 20				Output noise varies with selected update rates.
Integral Nonlinearity			±15	ppm of FSR	1 LSB_{16}
Offset Error[3]		±3		µV	Chop on
		±0.25		LSB_{16}	Chop off
Offset Error Drift[2]		10		nV/°C	Chop on
		200		nV/°C	Chop off
Full-Scale Error[4]		±0.5		LSB_{16}	
Gain Error Drift[4]		±0.5		ppm/°C	
Power Supply Rejection	80			dB	AIN = 1 V, range = ±2.56 V, chop enabled
		80		dB	AIN = 1 V, range = ±2.56 V, chop disabled

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSDUCER BURNOUT CURRENT SOURCES					
AIN+ Current		−100		nA	AIN+ is the selected positive input (AIN4 or AIN6 only) to the primary ADC
AIN− Current		100		nA	AIN− is the selected negative input (AIN5 or AIN7 only) to the primary ADC
Initial Tolerance at 25°C		±10		%	
Drift		0.03		%/°C	
EXCITATION CURRENT SOURCES					
Output Current		200		µA	Available from each current source
Initial Tolerance at 25°C		±10		%	
Drift		200		ppm/°C	
Initial Current Matching at 25°C		±1		%	Matching between both current sources
Drift Matching		20		ppm/°C	
Line Regulation (AV_{DD})		1		µA/V	AV_{DD} = 5 V ± 5%
Load Regulation		0.1		µA/V	
Output Compliance[2]	AGND		AV_{DD} − 0.6	V	
POWER SUPPLY MONITOR (PSM)					
AV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
AV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
DV_{DD} Trip Point Selection Range	2.63		4.63	V	Four trip points selectable in this range
DV_{DD} Trip Point Accuracy			±3.0	%	T_{MAX} = 85°C
			±4.0	%	T_{MAX} = 125°C
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)					
Logic Inputs, XTAL1 Only[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	3.5			V	DV_{DD} = 5 V
	2.5			V	DV_{DD} = 3 V
XTAL1 Input Capacitance		18		pF	
XTAL2 Output Capacitance		18		pF	
LOGIC INPUTS					
All Inputs Except SCLOCK, RESET, and XTAL1[2]					
V_{INL}, Input Low Voltage			0.8	V	DV_{DD} = 5 V
			0.4	V	DV_{DD} = 3 V
V_{INH}, Input Low Voltage	2.0			V	
SCLOCK and RESET Only (Schmidt Triggered Inputs)[2]					
V_{T+}	1.3		3.0	V	DV_{DD} = 5 V
	0.95		2.5	V	DV_{DD} = 3 V
V_{T-}	0.8		1.4	V	DV_{DD} = 5 V
	0.4		1.1	V	DV_{DD} = 3 V
$V_{T+} - V_{T-}$	0.3		0.85	V	DV_{DD} = 5 V or 3 V
Input Currents					
Port 0, P1.0 to P1.7, $\overline{EA}$			±10	µA	V_{IN} = 0 V or V_{DD}
RESET			±10	µA	V_{IN} = 0 V, DV_{DD} = 5 V
	35		105	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V, internal pull-down
Port 2, Port 3			±10	µA	V_{IN} = DV_{DD}, DV_{DD} = 5 V
	−180		−660	µA	V_{IN} = 2 V, DV_{DD} = 5 V
	−20		−75	µA	V_{IN} = 0.45 V, DV_{DD} = 5 V
Input Capacitance		10		pF	All digital inputs

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PWM					
–Fxtal		3		µA	
–Fvco		0.5		mA	
TIC		1		µA	
3 V Power Consumption					2.7 V < DV_{DD} < 3.6 V, AV_{DD} = 3.6 V
Normal Mode[11, 12]					
DV_{DD} Current			4.8	mA	Core clock = 1.57 MHz
		9	11	mA	Core clock = 6.29 MHz (CD = 1)
AV_{DD} Current			180	µA	ADC not enabled
Power-Down Mode[11, 12]					
DV_{DD} Current		20	26	µA	T_{MAX} = 85°C; OSC on; TIC on
		29		µA	T_{MAX} = 125°C; OSC on; TIC on
		14	20	µA	T_{MAX} = 85°C; OSC off
		21		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off

[1] Temperature range is for ADuC845BS; for the ADuC847BS and ADuC848BS (MQFP package), the range is –40°C to +125°C. Temperature range for ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) is –40°C to +85°C.
[2] These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[3] System zero-scale calibration can remove this error.
[4] Gain error drift is a span drift. To calculate full-scale error drift, add the offset error drift to the gain error drift times the full-scale input.
[5] In general terms, the bipolar input voltage range to the primary ADC is given by the ADC range = ±(V_{REF} 2^{RN})/1.25, where: V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected. RN = decimal equivalent of RN2, RN1, RN0. For example, if V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0, respectively, then the ADC range = ±1.28 V. In unipolar mode, the effective range is 0 V to 1.28 V in this example.
[6] 1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0/XREF1 or AXREF bits in ADC0CON2 and ADC1CON, respectively. (AXREF is available only on the ADuC845.)
[7] In bipolar mode, the auxiliary ADC can be driven only to a minimum of AGND – 30 mV as indicated by the auxiliary ADC absolute AIN voltage limits. The bipolar range is still –V_{REF} to +V_{REF}.
[8] DAC linearity and ac specifications are calculated using a reduced code range of 48 to 4095, 0 V to V_{REF}, reduced code range of 100 to 3950, 0 V to V_{DD}.
[9] Endurance is qualified to 100 kcycle per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 kcycles.
[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.
[11] Power supply current consumption is measured in normal mode following the power-on sequence, and in power-down modes under the following conditions: Normal mode: reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, core executing internal software loop. Power-down mode: reset = 0.4 V, all P0 pins and P1.2 to P1.7 pins = 0.4 V. All other digital I/O pins are open circuit, core Clk changed via CD bits in PLLCON, PCON.1 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[12] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

General Notes about Specifications

- DAC gain error is a measure of the span error of the DAC.
- The ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) have been qualified and tested with the base of the LFCSP package floating. The base of the LFCSP package should be soldered to the board, but left floating electrically, to ensure good mechanical stability.
- Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
9	9	P1.4/AIN5	I	On power-on default, P1.4/AIN5 is configured as the AIN5 analog input. AIN5 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN6. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
10	10	P1.5/AIN6	I	On power-on default, P1.5/AIN6 is configured as the AIN6 analog input. AIN6 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN5. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
11	11	P1.6/AIN7/IEXC1	I/O	On power-on default, P1.6/AIN7 is configured as the AIN7 analog input. AIN7 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN8. One or both current sources can also be configured at this pin. P1.6 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
12	12	P1.7/AIN8/IEXC2	I/O	On power-on default, P1.7/AIN8 is configured as the AIN8 analog input. AIN8 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN7. One or both current sources can also be configured at this pin. P1.7 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
13	13	AINCOM/DAC	I/O	All analog inputs can be referred to this pin, provided that a relevant pseudo differential input mode is selected. This pin also functions as an alternative pin out for the DAC.
14	14	DAC	O	The voltage output from the DAC, if enabled, appears at this pin.
Not applicable	15	AIN9	I	AIN9 can be used as a pseudo differential analog input when used with AINCOM or as the positive input of a fully differential pair when used with AIN10 (LFCSP version only).
Not applicable	16	AIN10	I	AIN10 can be used as a pseudo differential analog input when used with AINCOM or as the negative input of a fully differential pair when used with AIN9 (LFCSP version only).
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. This pin has an internal weak pull-down and a Schmitt trigger input stage.
16 to 19, 22 to 25	18 to 21, 24 to 27	P3.0 to P3.7	I/O	P3.0 to P3.7 are bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active for one core clock period of the instruction cycle. Port 3 pins also have the various secondary functions described in this table.
16	18	P3.0/RxD		Receiver Data for UART Serial Port.
17	19	P3.1/TxD		Transmitter Data for UART Serial Port.
18	20	P3.2/$\overline{\text{INT0}}$		External Interrupt 0. This pin can also be used as a gate control input to Timer 0.
19	21	P3.3/$\overline{\text{INT1}}$		External Interrupt 1. This pin can also be used as a gate control input to Timer 1.
22	24	P3.4/T0		Timer/Counter 0 External Input.
23	25	P3.5/T1		Timer/Counter 1 External Input.
24	26	P3.6/$\overline{\text{WR}}$		External Data Memory Write Strobe. This pin latches the data byte from Port 0 into an external data memory.
25	27	P3.7/$\overline{\text{RD}}$		External Data Memory Read Strobe. This pin enables the data from an external data memory to Port 0.

FUNCTIONAL DESCRIPTION

8051 INSTRUCTION SET

Table 4. Optimized Single-Cycle 8051 Instruction Set

Mnemonic	Description	Bytes	Cycles[1]
Arithmetic			
A A,Rn	Add register to A	1	1
ADD A,@Ri	Add indirect memory to A	1	2
ADD A,dir	Add direct byte to A	2	2
ADD A,#data	Add immediate to A	2	2
ADDC A,Rn	Add register to A with carry	1	1
ADDC A,@Ri	Add indirect memory to A with carry	1	2
ADDC A,dir	Add direct byte to A with carry	2	2
ADD A,#data	Add immediate to A with carry	2	2
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	2
SUBB A,dir	Subtract direct from A with borrow	2	2
SUBB A,#data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC @Ri	Increment indirect memory	1	2
INC dir	Increment direct byte	2	2
INC DPTR	Increment data pointer	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC @Ri	Decrement indirect memory	1	2
DEC dir	Decrement direct byte	2	2
MUL AB	Multiply A by B	1	4
DIV AB	Divide A by B	1	9
DA A	Decimal adjust A	1	2
Logic			
ANL A,Rn	AND register to A	1	1
ANL A,@Ri	AND indirect memory to A	1	2
ANL A,dir	AND direct byte to A	2	2
ANL A,#data	AND immediate to A	2	2
ANL dir,A	AND A to direct byte	2	2
ANL dir,#data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to A	1	1
ORL A,@Ri	OR indirect memory to A	1	2
ORL A,dir	OR direct byte to A	2	2
ORL A,#data	OR immediate to A	2	2
ORL dir,A	OR A to direct byte	2	2
ORL dir,#data	OR immediate data to direct byte	3	3
XRL A,Rn	Exclusive-OR register to A	1	1
XRL A,@Ri	Exclusive-OR indirect memory to A	2	2
XRL A,#data	Exclusive-OR immediate to A	2	2
XRL dir,A	Exclusive-OR A to direct byte	2	2
XRL A,dir	Exclusive-OR indirect memory to A	2	2
XRL dir,#data	Exclusive-OR immediate data to direct	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1

Mnemonic	Description	Bytes	Cycles[1]
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2
MOV dir,A	Move A to direct byte	2	2
MOV Rn, dir	Move register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,@Ri	Move indirect to direct memory	2	2
MOV @Ri,dir	Move direct to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A	1	4
MOVX[2] A,@Ri	Move external (A8) data to A	1	4
MOVX[2] A,@DPTR	Move external (A16) data to A	1	4
MOVX[2] @Ri,A	Move A to external data (A8)	1	4
MOVX[2] @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit	OR direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3

This offset is removed by performing a running average of 2. This average by 2 means that the settling time to any change in programming of the ADC is twice the normal conversion time, while an asynchronous step change on the analog input is not fully reflected until the third subsequent output. See Figure 13.

$$t_{SETTLE} = \frac{2}{f_{ADC}} = 2 \times t_{ADC}$$

The allowable range for SF (chop enabled) is 13 to 255 with a default of 69 (45H). The corresponding conversion rates, rms and peak-to-peak noise performances are shown in Table 10, Table 11, Table 12, and Table 13. The numbers are typical and generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. Note that the conversion time increases by 0.732 ms for each increment in SF.

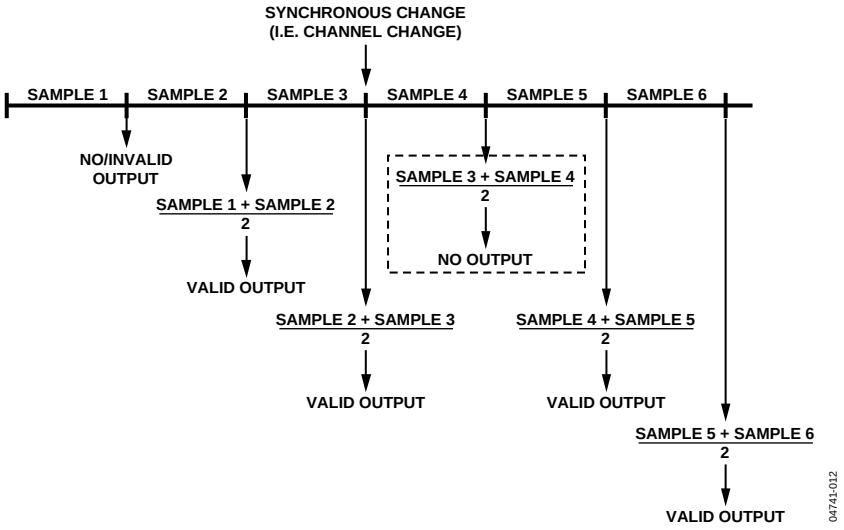

Figure 13. ADC Settling Time Following a Synchronous Change with Chop Enabled

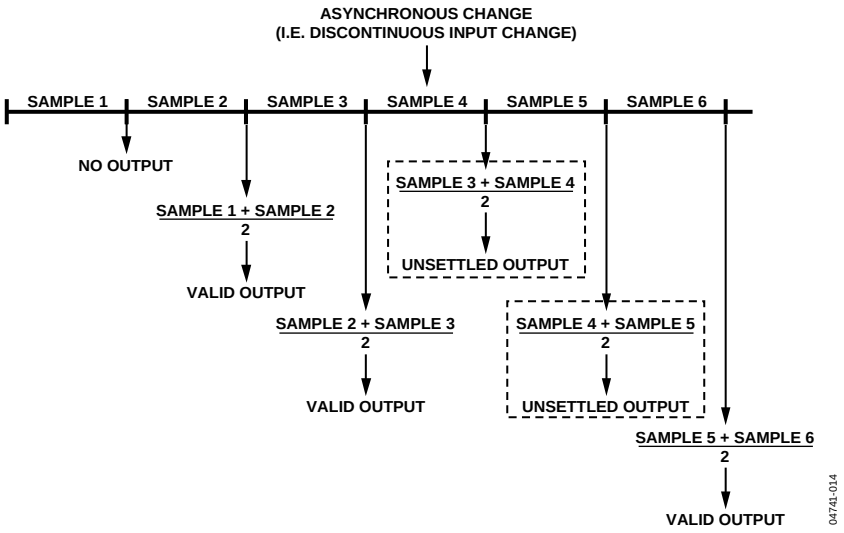

Figure 14. ADC Settling Time Following an Asynchronous Change with Chop Enabled

ADC Noise Performance with Chop Disabled ($\overline{CHOP}$ = 1)

Table 14 through Table 17 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. Note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution. Typically, the performance of the ADC with chop disabled shows a 0.5 LSB degradation over the performance with chop enabled.

Table 14. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
68	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 15. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	17	17	17.5	18
82	49.95	13	14	15	16	16.5	17.5	18	18
255	16.06	13.5	14.5	15.5	16.5	17.5	18.5	18.5	19

Table 16. ADuC848 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
69	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 17. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320mV	±640mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	16	16	16	16
82	49.95	13	14	15	16	16	16	16	16
255	16.06	13.5	14.5	15.5	16	16	16	16	16

AUXILIARY ADC (ADUC845 ONLY)

Table 18. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Enabled

SF Word	Data Update Rate (Hz)	μV
13	105.03	17.46
23	59.36	3.13
27	50.56	4.56
69	19.79	2.66
255	5.35	1.13

Table 19. ADuC845 Typical Peak-to-Peak Resolution (Bits) vs. Update Rate[1] with Chop Enabled

SF Word	Data Update Rate (Hz)	Bits
13	105.03	15.5
23	59.36	18
27	50.56	17.5
69	19.79	18
255	5.35	19.5

[1] ADC converting in bipolar mode.

Table 20. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	μV
3	1365.33	1386.58
13	315.08	34.94
66	62.06	3.2
69	59.36	3.19
81	50.57	3.14
255	16.06	1.71

Table 21. ADuC845 Peak-to-Peak Resolution (Bits) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Bits
3	1365.33	9
13	315.08	14.5
66	62.06	18
69	59.36	18
81	50.57	18
255	16.06	19

REFERENCE INPUTS

The ADuC845/ADuC847/ADuC848 each have two separate differential reference inputs, REFIN± and REFIN2±. While both references are available for use with the primary ADC, only REFIN± is available for the auxiliary ADC (ADuC845 only). The common-mode range for these differential references is from AGND to AV_{DD}. The nominal external reference voltage is 2.5 V, with the primary and auxiliary (ADuC845 only) reference select bits configured from the ADC0CON2 and ADC1CON (ADuC845 only), respectively.

When an external reference voltage is used, the primary ADC sees this internally as a 2.56 V reference ($V_{REF} \times 1.024$). Therefore, any calculations of LSB size should account for this. For instance, with a 2.5 V external reference connected and using a gain of 1 on a unipolar range (2.56 V), the LSB size is $(2.56/2^{24}) = 152.6$ nV (if using the 24-bit ADC on the ADuC845 or ADuC847). If a bipolar gain of 4 is used (±640 mV), the LSB size is $(±640 \text{ mV})/2^{24}) = 76.3$ nV (again using the 24-bit ADC on the ADuC845 or ADuC847).

The ADuC845/ADuC847/ADuC848 can also be configured to use the on-chip band gap reference via the XREF0/1 bits in the ADC0CON2 SFR (for primary ADC) or the AXREF bit in ADC1CON (for auxiliary ADC (ADuC845 only)). In this mode of operation, the ADC sees the internal reference of 1.25 V, thereby halving all the input ranges. A consequence of using the internal band gap reference is a noticeable degradation in peak-to-peak resolution. For this reason, operation with an external reference is recommended.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference inputs for the device, the effect of any low frequency noise in the excitation source is removed because the application is ratiometric. If the devices are not used in a ratiometric configuration, use a low noise reference. Recommended reference voltage sources for the ADuC845/ADuC847/ADuC848 include the ADR421, REF43, and REF192.

The reference inputs provide a high impedance, dynamic load to external connections. Because the impedance of each reference input is dynamic, resistor/capacitor combinations on these pins can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources, such as those mentioned above, for example, the ADR421, typically have low output impedances, and, therefore, decoupling capacitors on the REFIN± or REFIN2± inputs would be recommended (typically 0.1 μF). Deriving the reference voltage from an external resistor configuration means that the reference input sees a significant external source impedance. External decoupling of the REFIN± and/or REFIN2± inputs is not recommended in this type of configuration.

BURNOUT CURRENT SOURCES

The primary ADC on the ADuC845 and the ADC on the ADuC847 and ADuC848 incorporate two 100 nA constant current generators that are used to detect a failure in a connected sensor. One sources current from the AV_{DD} to AIN(+), and one sinks current from AIN(−) to AGND. These currents are only configurable for use on AIN5/AIN6 and/or AIN7/AIN8 in differential mode only, from the ICON.6 bit in the ICON SFR

(REJ60 bit, ADCMODE.6). This fixed filter can be enabled or disabled by setting or clearing the REJ60 bit in the ADCMODE register (ADCMODE.6). This 60 Hz drop-in notch filter can be enabled for any SF word that yields an ADC throughput that is less than 20 Hz with chop enabled (SF ≥ 68 decimal).

ADC CHOPPING

The ADCs on the ADuC845/ADuC847/ADuC848 implement a chopping scheme whereby the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc^3 filter, therefore, have a positive and negative offset term included. As a result, a final summing stage is included in each ADC so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data SFRs. The ADC throughput or update rate is listed in Table 29. The chopping scheme incorporated into the devices results in excellent dc offset and offset drift specifications, and is extremely beneficial in applications where drift, noise rejection, and optimum EMI performance are important. ADC chop can be disabled via the chop bit in the ADCMODE SFR (ADCMODE.3). Setting this bit to 1 (logic high) disables chop mode.

CALIBRATION

The ADuC845/ADuC847/ADuC848 incorporate four calibration modes that can be programmed via the mode bits in the ADCMODE SFR detailed in Table 24. Every device is calibrated before it leaves the factory. The resulting offset and gain calibration coefficients for both the primary and auxiliary (ADuC845 only) ADCs are stored on-chip in manufacturing-specific Flash/EE memory locations. At power-on or after a reset, these factory calibration registers are automatically downloaded to the ADC calibration registers in the SFR space of the device. To facilitate user calibration, each of the primary and auxiliary (ADuC845 only) ADCs have dedicated calibration control SFRs, which are described in the ADC SFR Interface section. Once a user initiates a calibration procedure, the factory calibration values that were initially downloaded during the power-on sequence to the ADC calibration SFRs are overwritten. The ADC to be calibrated must be enabled via the ADC enable bits in the ADCMODE register.

Even though an internal offset calibration mode is described in this section, note that the ADCs can be chopped. This chopping scheme inherently minimizes offset errors and means that an offset calibration should never be required. Also, because factory 5 V/25°C gain calibration coefficients are automatically present at power-on, an internal full-scale calibration is required only if the device is operated at 3 V or at temperatures significantly different from 25°C.

If the device is operated in chop disabled mode, a calibration may need to be done with every gain range change that occurs via the PGA.

The ADuC845/ADuC847/ADuC848 each offer internal or system calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two input conditions: zero-scale and full-scale points. These points are derived by performing a conversion on the different input voltages (zero-scale and full-scale) provided to the input of the modulator during calibration. The result of the zero-scale calibration conversion is stored in the offset calibration registers for the appropriate ADC. The result of the full-scale calibration conversion is stored in the gain calibration registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an internal zero-scale or full-scale calibration, the respective zero-scale input or full-scale input is automatically connected to the ADC inputs internally. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied externally to the ADC pins by the user before the calibration mode is initiated. In this way, external errors are taken into account and minimized. Note that all ADuC845/ADuC847/ADuC848 ADC calibrations are carried out at the user-selected SF word update rate. To optimize calibration accuracy, it is recommended that the slowest possible update rate be used.

Internally in the devices, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient.

From an operational point of view, a calibration should be treated just like an ordinary ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 bit in the ADCSTAT SFR to determine the end of calibration by using a polling sequence or an interrupt driven routine. If required, the NOEXREF0/1 bits can be monitored to detect unconnected or low voltage errors in the reference during conversion. In the event of the reference becoming disconnected, causing a NOXREF flag during a calibration, the calibration is immediately halted and no write to the calibration SFRs takes place.

Internal Calibration Example

With chop enabled, a zero-scale or offset calibration should never be required, although a full-scale or gain calibration may be required. However, if a full internal calibration is required, the procedure should be to select a PGA gain of 1 (±2.56 V) and perform a zero-scale calibration (MD2...0 = 100B in the ADCMODE register). Next, select and perform full-scale calibration by setting MD2...0 = 101B in the ADCMODE SFR. Now select the desired PGA range and perform a zero-scale calibration again (MD2..0 = 100B in ADCMODE) at the new PGA range. The reason for the double zero-scale calibration is

FUNCTIONAL DESCRIPTION

ADC SFR INTERFACE

The ADCs are controlled and configured via a number of SFRs that are mentioned here and described in more detail in the following sections.

Table 22. ADC SFR Interface

Name	Description
ADCSTAT	ADC Status Register. Holds the general status of the primary and auxiliary (ADuC845 only) ADCs.
ADCMODE	ADC Mode Register. Controls the general modes of operation for primary and auxiliary (ADuC845 only) ADCs.
ADC0CON1	Primary ADC Control Register 1. Controls the specific configuration of the primary ADC.
ADC0CON2	Primary ADC Control Register 2. Controls the specific configuration of the primary ADC.
ADC1CON	Auxiliary ADC Control Register. Controls the specific configuration of the auxiliary ADC. ADuC845 only.
SF	Sinc Filter Register. Configures the decimation factor for the Sinc^3 filter and, therefore, the primary and auxiliary (ADuC845 only) ADC update rates.
ICON	Current Source Control Register. Allows user control of the various on-chip current source options.
ADC0L/M/H	Primary ADC 24-bit (16-bit on the ADuC848) conversion result is held in these three 8-bit registers. ADC0L is not available on the ADuC848.
ADC1L/M/H	Auxiliary ADC 24-bit conversion result is held in these two 8-bit registers. ADuC845 only.
OF0L/M/H	Primary ADC 24-bit offset calibration coefficient is held in these three 8-bit registers. OF0L is not available on the ADuC848.
OF1L/H	Auxiliary ADC 16-bit offset calibration coefficient is held in these two 8-bit registers. ADuC845 only.
GN0L/M/H	Primary ADC 24-bit gain calibration coefficient is held in these three 8-bit registers. GN0L is not available on the ADuC848.
GN1L/H	Auxiliary ADC 16-bit gain calibration coefficient is held in these two 8-bit registers. ADuC845 only.

ADCMODE (ADC MODE REGISTER)

Used to control the operational mode of both ADCs.

SFR Address: D1H
Power-On Default: 08H
Bit Addressable: No

Table 24. ADCMODE SFR Bit Designations

Bit No.	Name	Description
7	---	Not Implemented. Write Don't Care.
6	REJ60	Automatic 60 Hz Notch Select Bit. Setting this bit places a notch in the frequency response at 60 Hz, allowing simultaneous 50 Hz and 60 Hz rejection at an SF word of 82 decimal. This 60 Hz notch can be set only if SF ≥68 decimal, that is, the regular filter notch must be ≤60 Hz. This second notch is placed at 60 Hz only if the device clock is at 32.768 kHz.
5	ADC0EN	Primary ADC Enable. Set by the user to enable the primary ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the primary ADC into power-down mode.
4	ADC1EN (ADuC845 only)	Auxiliary (ADuC845 only) ADC Enable. Set by the user to enable the auxiliary (ADuC845 only) ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the auxiliary (ADuC845 only) ADC in power-down mode.
3	$\overline{\text{CHOP}}$	Chop Mode Disable. Set by the user to disable chop mode on both the primary and auxiliary (ADuC845 only) ADC allowing a three times higher ADC data throughput. SF values as low as 3 are allowed with this bit set, giving up to 1.3 kHz ADC update rates. Cleared by the user to enable chop mode on both the primary and auxiliary (ADuC845 only) ADC.
2, 1, 0	MD2, MD1, MD0	Primary and Auxiliary (ADuC845 only) ADC Mode Bits. These bits select the operational mode of the enabled ADC as follows: MD2 MD1 MD0 0 0 0 ADC Power-Down Mode (Power-On Default). 0 0 1 Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided. 0 1 0 Single Conversion Mode. In single conversion mode, a single conversion is performed on the enabled ADC. Upon completion of a conversion, the ADC data registers (ADC0H/M/L and/or ADC1H/M/L (ADuC845 only)) are updated. The relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000. Note that ADC0L is not available on the ADuC848. 0 1 1 Continuous Conversion. In continuous conversion mode, the ADC data registers are regularly updated at the selected update rate (see the Sinc Filter SFR Bit Designations in Table 28). 1 0 0 Internal Zero-Scale Calibration. Internal short automatically connected to the enabled ADC input(s). 1 0 1 Internal Full-Scale Calibration. Internal or external REFIN± or REFIN2± V_{REF} (as determined by XREF bits in ADC0CON2 and/or AXREF (ADuC845 only) in ADC1CON (ADuC845 only) is automatically connected to the enabled ADC input(s) for this calibration. 1 1 0 System Zero-Scale Calibration. User should connect system zero-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers. 1 1 1 System Full-Scale Calibration. User should connect system full-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers.

ADC0CON1 (PRIMARY ADC CONTROL REGISTER)

ADC0CON1 is used to configure the primary ADC for buffer, unipolar, or bipolar coding, and ADC range configuration.

SFR Address: D2H
Power-On Default: 07H
Bit Addressable: No

Table 25. ADC0CON1 SFR Bit Designations

Bit No.	Name	Description			
7, 6	BUF1, BUF0	Buffer Configuration Bits.			
		BUF1	BUF0		Buffer Configuration
		0	0		ADC0+ and ADC0– are buffered
		0	1		Reserved
		1	0		Buffer Bypass
		1	1		Reserved
5	UNI	Primary ADC Unipolar Bit.			
		Set by the user to enable unipolar coding; zero differential input results in 000000H output.			
		Cleared by the user to enable bipolar coding; zero differential input results in 800000H output.			
4	–––	Not Implemented. Write Don't Care.			
3	–––	Not Implemented. Write Don't Care.			
2, 1, 0	RN2, RN1, RN0	Primary ADC Range Bits. Written by the user to select the primary ADC input range as follows:			
		RN2	RN1	RN0	Selected primary ADC input range (V_{REF} = 2.5 V)
		0	0	0	±20 mV (0 mV to 20 mV in unipolar mode)
		0	0	1	±40 mV (0 mV to 40 mV in unipolar mode)
		0	1	0	±80 mV (0 mV to 80 mV in unipolar mode)
		0	1	1	±160 mV (0 mV to 160 mV in unipolar mode)
		1	0	0	±320 mV (0 mV to 320 mV in unipolar mode)
		1	0	1	±640 mV (0 mV to 640 mV in unipolar mode)
		1	1	0	±1.28 V (0 V to 1.28 V in unipolar mode)
		1	1	1	±2.56 V (0 V to 2.56 V in unipolar mode)

Mode 5 (Dual 8-Bit PWM)

In Mode 5, the duty cycle and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

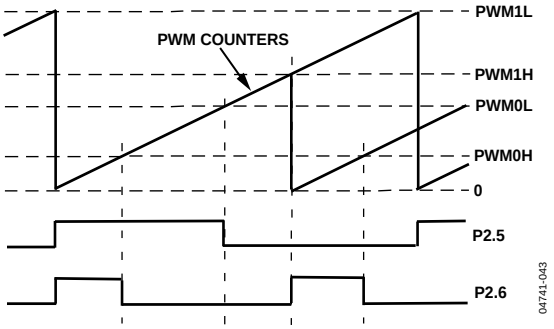

Figure 43. PWM Mode 5

Mode 6 (Dual RZ 16-Bit Σ-Δ DAC)

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4; however, the key difference is that Mode 6 provides return to zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. RZ mode ensures that any difference in the rise and fall times does not affect the Σ-Δ DAC INL. However, RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V– to AV_{DD} down to 0 V to $AV_{DD}/2$. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three full clocks (3 × 80 ns), high for one-half a clock (40 ns), and then low again for one-half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

The output resolution is set by the PWM1L and PWM1H SFRs for the P2.5 and P2.6 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P2.5 and P2.6, respectively. Both PWMs have the same clock source and clock divider.

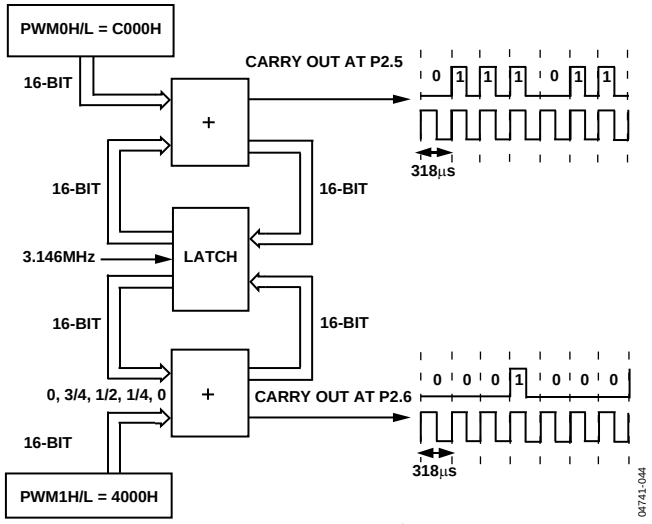

Figure 44. PWM Mode 6

Mode 7

In Mode 7, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal.

Hardware Slave Mode

After reset, the ADuC845/ADuC847/ADuC848 default to hardware slave mode. Slave mode is enabled by clearing the I2CM bit in I2CCON. The devices have a full hardware slave. In slave mode, the I²C address is stored in the I2CADD register. Data received or to be transmitted is stored in the I2CDAT register.

Once enabled in I²C slave mode, the slave controller waits for a start condition. If the parts detect a valid start condition, followed by a valid address, followed by the R/W bit, then the I2CI interrupt bit is automatically set by hardware. The I²C peripheral generates a core interrupt only if the user has pre-configured the I²C interrupt enable bit in the IEIP2 SFR as well as the global interrupt bit, EA, in the IE SFR. Therefore,

```
MOV IEIP2, #01h    ;Enable I²C Interrupt
SETB EA
```

An autoclear of the I2CI bit is implemented on the devices so that this bit is cleared automatically upon read or write access to the I2CDAT SFR.

```
MOV I2CDAT, A      ;I2CI auto-cleared
MOV A, I2CDAT      ;I2CI auto-cleared
```

If for any reason the user tries to clear the interrupt more than once, that is, access the data SFR more than once per interrupt, the I²C controller stops. The interface then must be reset by using the I2CRS bit.

The user can choose to poll the I2CI bit or to enable the interrupt. In the case of the interrupt, the PC counter vectors to 003BH at the end of each complete byte. For the first byte, when the user gets to the I2CI ISR, the 7-bit address and the R/W bit appear in the I2CDAT SFR.

The I2CTX bit contains the R/W bit sent from the master. If I2CTX is set, the master is ready to receive a byte; therefore the slave transmits data by writing to the I2CDAT register. If I2CTX is cleared, the master is ready to transmit a byte; therefore the slave receives a serial byte. Software can interrogate the state of I2CTX to determine whether it should write to or read from I2CDAT.

Once the device has received a valid address, hardware holds SCLOCK low until the I2CI bit is cleared by software. This allows the master to wait for the slave to be ready before transmitting the clocks for the next byte.

The I2CI interrupt bit is set every time a complete data byte is received or transmitted, provided that it is followed by a valid ACK. If the byte is followed by a NACK, an interrupt is not generated.

The device continues to issue interrupts for each complete data byte transferred until a stop condition is received or the interface is reset.

When a stop condition is received, the interface resets to a state in which it is waiting to be addressed (idle). Similarly, if the interface receives a NACK at the end of a sequence, it also returns to the default idle state. The I2CRS bit can be used to reset the I²C interface. This bit can be used to force the interface back to the default idle state.

SPI SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 integrate a complete hardware serial peripheral interface (SPI) interface on-chip. SPI is an industry-standard synchronous serial interface that allows 8 bits of data to be synchronously transmitted and received simultaneously, that is, full duplex. Note that the SPI pins are multiplexed with the Port 2 pins, P2.0, P2.1, P2.2, and P2.3. These pins have SPI functionality only if SPE is set. Otherwise, with SPE cleared, standard Port 2 functionality is maintained. SPI can be configured for master or slave operation and typically consists of Pins SCLOCK, MISO, MOSI, and $\overline{SS}$.

SCLOCK (Serial Clock I/O Pin)

Pin 28 (MQFP Package), Pin 30 (LFCSP Package)
The master clock (SCLOCK) is used to synchronize the data transmitted and received through the MOSI and MISO data lines.

A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table 41). In slave mode, the SPICON register must be configured with the same phase and polarity (CPHA and CPOL) as the master. The data is transmitted on one edge of the SCLOCK signal and sampled on the other.

MISO (Master In, Slave Out Pin)

Pin 30 (MQFP Package), Pin 32 (LFCSP Package)
The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

Pin 29 (MQFP Package), Pin31 (LFCSP Package)
The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

DUAL DATA POINTERS

The devices incorporate two data pointers. The second data pointer is a shadow data pointer and is selected via the data pointer control SFR (DPCON). DPCON features automatic hardware post-increment and post-decrement as well as an automatic data pointer toggle.

DPCON—Data Pointer Control SFR

SFR Address: A7H
Power-On Default: 00H
Bit Addressable: No

Table 42. DPCON SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	DPT	Data Pointer Automatic Toggle Enable. Cleared by the user to disable autoswapping of the DPTR. Set in user software to enable automatic toggling of the DPTR after each MOVX or MOVC instruction.
5, 4	DP1m1, DP1m0	Shadow Data Pointer Mode. These bits enable extra modes of the shadow data pointer operation, allowing more compact and more efficient code size and execution. DP1m1 DP1m0 Behavior of the Shadow Data Pointer 0 0 8052 behavior. 0 1 DPTR is post-incremented after a MOVX or a MOVC instruction. 1 0 DPTR is post-decremented after a MOVX or MOVC instruction. 1 1 DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction can be useful for moving 8-bit blocks to/from 16-bit devices.)
3, 2	DP0m1, DP0m0	Main Data Pointer Mode. These bits enable extra modes of the main data pointer operation, allowing more compact and more efficient code size and execution. DP0m1 DP0m0 Behavior of the Main Data Pointer 0 0 8052 behavior. 0 1 DPTR is post-incremented after a MOVX or a MOVC instruction. 1 0 DPTR is post-decremented after a MOVX or MOVC instruction. 1 1 DPTR LSB is toggled after a MOVX or MOVC instruction. (This instruction is useful for moving 8-bit blocks to/from 16-bit devices.)
1	----	Not Implemented. Write Don't Care.
0	DPSEL	Data Pointer Select. Cleared by the user to select the main data pointer. This means that the contents of this 24-bit register are placed into the DPL, DPH, and DPP SFRs. Set by the user to select the shadow data pointer. This means that the contents of a separate 24-bit register appear in the DPL, DPH, and DPP SFRs.

Note the following:

- The Dual Data Pointer section is the only place in which main and shadow data pointers are distinguished. Whenever the DPTR is mentioned elsewhere in this data sheet, active DPTR is implied.
- Only the MOVC/MOVX @DPTR instructions automatically post-increment and post-decrement the DPTR. Other MOVC/MOVX instructions, such as MOVC PC or MOVC @Ri, do not cause the DPTR to automatically post-increment and post-decrement.

To illustrate the operation of DPCON, the following code copies 256 bytes of code memory at Address D000H into XRAM, starting from Address 0000H.

```
        MOV DPTR,#0       ;Main DPTR = 0
        MOV DPCON,#55H    ;Select shadow DPTR
                          ;DPTR1 increment mode
                          ;DPTR0 increment mode
                          ;DPTR auto toggling ON
        MOV DPTR,#0D000H  ;DPTR = D000H
MOVELOOP: CLR A
        MOVC A,@A+DPTR    ;Get data
                          ;Post Inc DPTR
                          ;Swap to Main DPTR(Data)
         MOVX @DPTR,A     ;Put ACC in XRAM
                          ;Increment main DPTR
                          ;Swap Shadow DPTR(Code)
         MOV A, DPL
         JNZ MOVELOOP
```

IEIP2—Secondary Interrupt Enable Register

SFR Address: A9H
Power-On Default: A0H
Bit Addressable: No

Table 60. IEIP2 Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	PTI	Time Interval Counter Interrupt Priority Setting (1 = High, 0 = Low).
5	PPSM	Power Supply Monitor Interrupt Priority Setting (1 = High, 0 = Low).
4	PSI	SPI/I²C Interrupt Priority Setting (1 = High, 0 = Low).
3	----	This bit must contain 0.
2	ETI	Set by the user to enable the time interval counter interrupt. Cleared by the user to disable the time interval counter interrupt.
1	EPSMI	Set by the user to enable the power supply monitor interrupt. Cleared by the user to disable the power supply monitor interrupt.
0	ESI	Set by the user to enable the SPI/I²C serial port interrupt. Cleared by the user to disable the SPI/I²C serial port interrupt.

INTERRUPT PRIORITY

The interrupt enable registers are written by the user to enable individual interrupt sources; the interrupt priority registers allow the user to select one of two priority levels for each interrupt. A high priority interrupt can interrupt the service routine of a low priority interrupt, and if two interrupts of different priorities occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, the polling sequence, as shown in Table 61, is observed.

Table 61. Priority within Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt
WDS	2	Watchdog Timer Interrupt
IE0	2	External Interrupt 0
RDY0/RDY1	3	ADC Interrupt
TF0	4	Timer/Counter 0 Interrupt
IE1	5	External Interrupt 1
TF1	6	Timer/Counter 1 Interrupt
ISPI/I2CI	7	SPI/I²C Interrupt
RI/TI	8	UART Serial Port Interrupt
TF2/EXF2	9	Timer/Counter 2 Interrupt
TII	11 (Lowest)	Timer Interval Counter Interrupt

INTERRUPT VECTORS

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 62.

Table 62. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
RDY0/RDY1 (ADuC845 only)	0033H
ISPI/I2CI	003BH
PSMI	0043H
TII	0053H
WDS	005BH

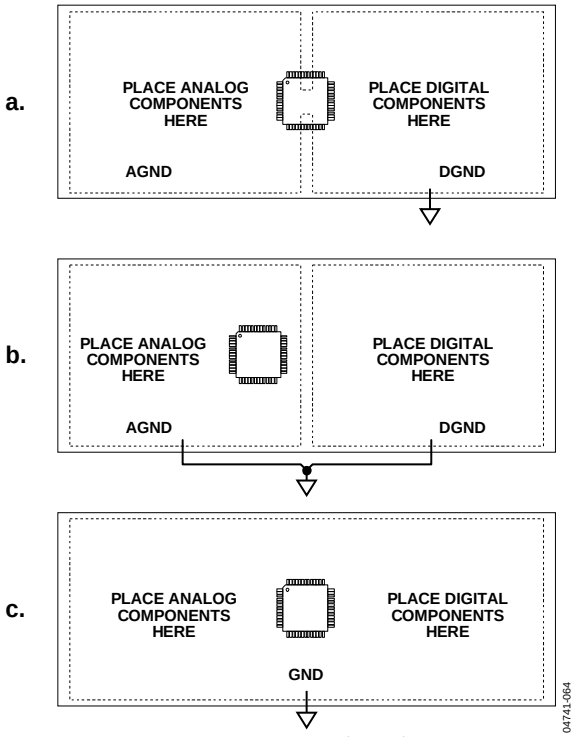

Figure 68. System Grounding Schemes

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the digital inputs of the ADuC845/ADuC847/ADuC848 add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the device. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the device and affecting the accuracy of ADC conversions.

When using the LFCSP package, it is recommended that the paddle underneath the chip be soldered to the board to provide maximum mechanical stability. However, it is recommended that this paddle not be grounded but left floating. All results and specifications contained in this data sheet are taken or recorded with the paddle floating.

System Self-Identification

In some hardware designs, it may be advantageous for the software to be able to identify the host MicroConverter.

The CHIPID SFR is a read-only register located at SFR address C2H. The upper nibble of this SFR designates the MicroConverter within the Σ-Δ ADC family. User software can read this SFR to identify the host MicroConverter and therefore execute slightly different code if required. The CHIPID SFR reads as follows for the Σ-Δ ADC family of MicroConverter products. Note that the ADuC845/ADuC847/ADuC848 are treated as one device as far as the CHIPID is concerned.

Table 63. CHIPID Values for Σ-Δ MicroConverter Products

Device	CHIPID
ADuC816	1xH
ADuC824	0xH
ADuC836	3xH
ADuC834	2xH
ADuC845/ADuC847/ADuC848	AxH

Clock Oscillator

As described earlier, the core clock frequency for the ADuC845/ADuC847/ADuC848 is generated from an on-chip PLL that locks onto a multiple (384 times) of 32.768 kHz. The latter is generated from an internal clock oscillator. To use the internal clock oscillator, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2 as shown in Figure 69.

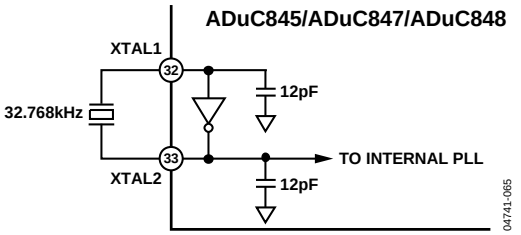

Figure 69. Crystal Connectivity to ADuC845/ADuC847/ADuC848

As shown in the typical external crystal connection diagram in Figure 69, two internal 12 pF capacitors are provided on-chip. These are connected internally, directly to the XTAL1 and XTAL2 pins. The total input capacitance at both pins is detailed in the Specifications table. Note that the total capacitance required for a particular crystal must be in accordance with the crystal manufacturer. However, in most cases, no additional external capacitance is required above that already supplied on-chip.

OTHER HARDWARE CONSIDERATIONS

In-Circuit Serial Download Access

Nearly all ADuC845/ADuC847/ADuC848 designs can take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the UART of the devices, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is shown in Figure 70 with a simple ADM3202-based circuit. If users would rather not include an RS-232 chip on the target board, refer to the uC006 Application Note, *A 4-Wire UART-to-PC Interface*, for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the device.

Table 70. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

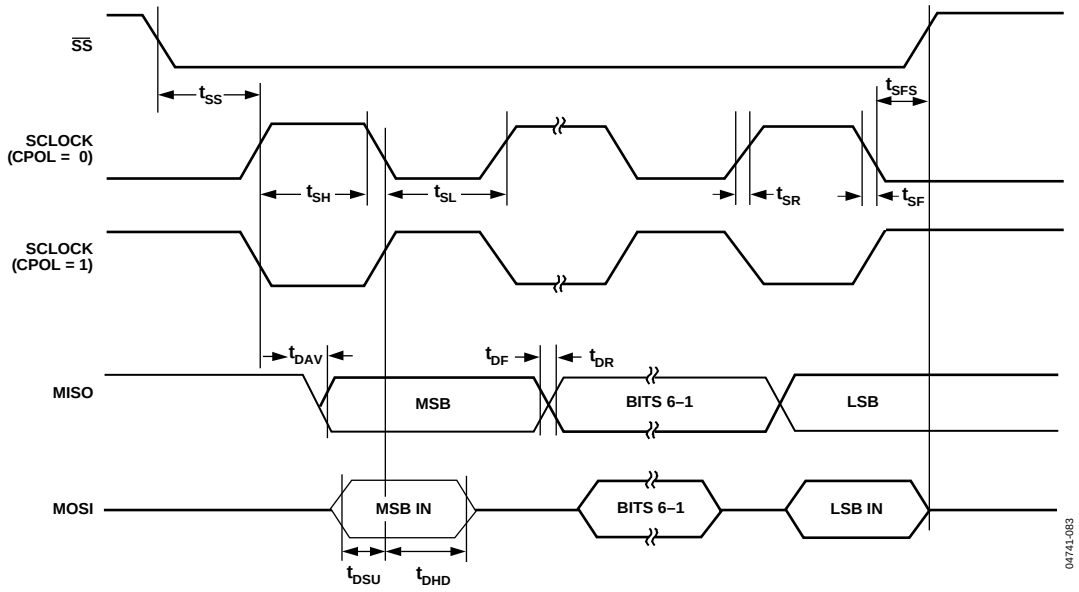

Figure 78. SPI Slave Mode Timing (CHPA = 1)

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADuC845BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC845BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC845BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC845BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC845BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC845BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC847BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC847BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC847BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC847BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC847BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC847BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC847BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC847BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC847BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC847BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC848BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC848BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC848BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC848BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC848BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC848BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC848BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC848BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC848BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC848BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
EVAL-ADuC845QSZ		QuickStart Development System	
EVAL-ADuC845QSPZ		QuickStart-PLUS Development System	
EVAL-ADuC847QSZ		QuickStart Development System	
EVAL-ADUC-CABLE1Z		ADuC Serial Downloader Cable for UART	

[1] The -3 and -5 in the Model column indicate the DV_{DD} operating voltage.
[2] Z = RoHS Compliant Part.
[3] The QuickStart Plus system can only be ordered directly from Accutron. It can be purchased from the website http://www.accutron.com.