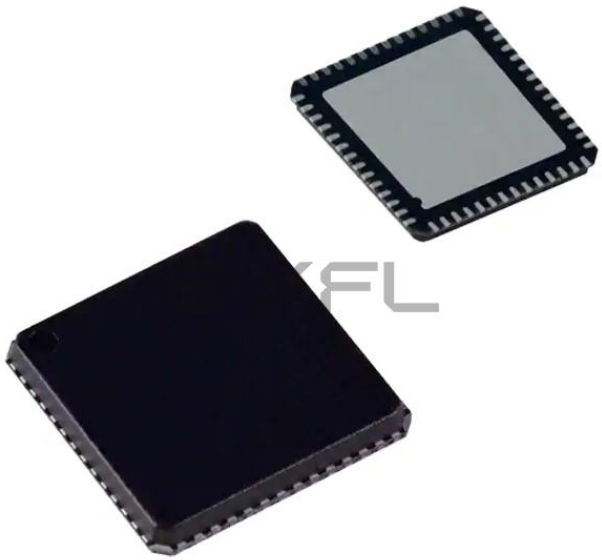

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 10x16b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc848bcpz62-5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (ALL DIGITAL OUTPUTS EXCEPT XTAL2)					
V_{OH}, Output High Voltage[2]	2.4			V	DV_{DD} = 5 V, I_{SOURCE} = 80 µA
	2.4			V	DV_{DD} = 3 V, I_{SOURCE} = 20 µA
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 8 mA, SCLOCK, SDATA
			0.4	V	I_{SINK} = 1.6 mA on P0, P1, P2
Floating State Leakage Current[2]			±10	µA	
Floating State Output Capacitance		10		pF	
START-UP TIME					
At Power-On		600		ms	
After Ext RESET in Normal Mode		3		ms	
After WDT RESET in Normal Mode		2		ms	Controlled via WDCON SFR
From Power-Down Mode					
Oscillator Running					PLLCON.7 = 0
Wake-Up with $\overline{INT0}$ Interrupt		20		µs	
Wake-Up with SPI Interrupt		20		µs	
Wake-Up with TIC Interrupt		20		µs	
Oscillator Powered Down					PLLCON.7 = 1
Wake-Up with $\overline{INT0}$ Interrupt		30		µs	
Wake-Up with SPI Interrupt		30		µs	
FLASH/EE MEMORY RELIABILITY CHARACTERISTICS					
Endurance[9]	100,000			Cycles	
Data Retention[10]	100			Years	
POWER REQUIREMENTS					
Power Supply Voltages					
AV_{DD} 3 V Nominal	2.7		3.6	V	
AV_{DD} 5 V Nominal	4.75		5.25	V	
DV_{DD} 3 V Nominal	2.7		3.6	V	
DV_{DD} 5 V Nominal	4.75		5.25	V	
5 V Power Consumption					4.75 V < DV_{DD} < 5.25 V, AV_{DD} = 5.25 V
Normal Mode[11, 12]					
DV_{DD} Current			10	mA	Core clock = 1.57 MHz
		25	31	mA	Core clock = 12.58 MHz
AV_{DD} Current			180	µA	
Power-Down Mode[11, 12]					
DV_{DD} Current		40	53	µA	T_{MAX} = 85°C; OSC on; TIC on
		50		µA	T_{MAX} = 125°C; OSC on; TIC on
		20	33	µA	T_{MAX} = 85°C; OSC off
		30		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off
Typical Additional Peripheral Currents (AI_{DD} and DI_{DD})					5 V V_{DD}, CD = 3
Primary ADC		1		mA	
Auxiliary ADC (ADuC845 Only)		0.5		mA	
Power Supply Monitor		30		µA	
DAC		60		µA	DACH/L = 000H
Dual Excitation Current Sources		200		µA	200 µA each. Can be combined to give 400 µA on a single output.
ALE Off		−20		µA	PCON.4 = 1 (see Table 6)
WDT		10		µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PWM					
–Fxtal		3		µA	
–Fvco		0.5		mA	
TIC		1		µA	
3 V Power Consumption					2.7 V < DV_{DD} < 3.6 V, AV_{DD} = 3.6 V
Normal Mode[11, 12]					
DV_{DD} Current			4.8	mA	Core clock = 1.57 MHz
		9	11	mA	Core clock = 6.29 MHz (CD = 1)
AV_{DD} Current			180	µA	ADC not enabled
Power-Down Mode[11, 12]					
DV_{DD} Current		20	26	µA	T_{MAX} = 85°C; OSC on; TIC on
		29		µA	T_{MAX} = 125°C; OSC on; TIC on
		14	20	µA	T_{MAX} = 85°C; OSC off
		21		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off

[1] Temperature range is for ADuC845BS; for the ADuC847BS and ADuC848BS (MQFP package), the range is –40°C to +125°C. Temperature range for ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) is –40°C to +85°C.
[2] These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[3] System zero-scale calibration can remove this error.
[4] Gain error drift is a span drift. To calculate full-scale error drift, add the offset error drift to the gain error drift times the full-scale input.
[5] In general terms, the bipolar input voltage range to the primary ADC is given by the ADC range = ±(V_{REF} 2^{RN})/1.25, where: V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected. RN = decimal equivalent of RN2, RN1, RN0. For example, if V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0, respectively, then the ADC range = ±1.28 V. In unipolar mode, the effective range is 0 V to 1.28 V in this example.
[6] 1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0/XREF1 or AXREF bits in ADC0CON2 and ADC1CON, respectively. (AXREF is available only on the ADuC845.)
[7] In bipolar mode, the auxiliary ADC can be driven only to a minimum of AGND – 30 mV as indicated by the auxiliary ADC absolute AIN voltage limits. The bipolar range is still –V_{REF} to +V_{REF}.
[8] DAC linearity and ac specifications are calculated using a reduced code range of 48 to 4095, 0 V to V_{REF}, reduced code range of 100 to 3950, 0 V to V_{DD}.
[9] Endurance is qualified to 100 kcycle per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 kcycles.
[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.
[11] Power supply current consumption is measured in normal mode following the power-on sequence, and in power-down modes under the following conditions: Normal mode: reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, core executing internal software loop. Power-down mode: reset = 0.4 V, all P0 pins and P1.2 to P1.7 pins = 0.4 V. All other digital I/O pins are open circuit, core Clk changed via CD bits in PLLCON, PCON.1 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[12] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

General Notes about Specifications

- DAC gain error is a measure of the span error of the DAC.
- The ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) have been qualified and tested with the base of the LFCSP package floating. The base of the LFCSP package should be soldered to the board, but left floating electrically, to ensure good mechanical stability.
- Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
20, 34, 48	22, 36, 51	DV_{DD}	S	Digital Supply Voltage.
21, 35, 47	23, 37, 38, 50	DGND	S	Digital Ground.
26	28	SCLK (I^2C)	I/O	Serial Interface Clock for the I^2C Interface. As an input, this pin is a Schmitt-triggered input. A weak internal pull-up is present on this pin unless it is outputting logic low. This pin can also be controlled in software as a digital output pin.
27	29	SDATA	I/O	Serial Data Pin for the I^2C Interface. As an input, this pin has a weak internal pull-up present unless it is outputting logic low.
28 to 31, 36 to 39	30 to 33, 39 to 42	P2.0 to P2.7	I/O	Port 2 is a bidirectional port with internal pull-up resistors. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 2 pins being pulled externally low source current because of the internal pull-up resistors. Port 2 emits the middle and high-order address bytes during accesses to the 24-bit external data memory space. Port 2 pins also have the various secondary functions described in this table.
28	30	P2.0/SCLOCK (SPI)		Serial Interface Clock for the SPI Interface. As an input this pin is a Schmitt-triggered input. A weak internal pull-up is present on this pin unless it is outputting logic low.
29	31	P2.1/MOSI		Serial Master Output/Slave Input Data for the SPI Interface. A strong internal pull-up is present on this pin when the SPI interface outputs a logic high. A strong internal pull-down is present on this pin when the SPI interface outputs a logic low.
30	32	P2.2/MISO		Master Input/Slave Output for the SPI Interface. A weak pull-up is present on this input pin.
31	33	P2.3/$\overline{SS}$/T2		Slave Select Input for the SPI Interface. A weak pull-up is present on this pin. For both package options, this pin can also be used to provide a clock input to Timer 2. When enabled, Counter 2 is incremented in response to a negative transition on the T2 input pin.
36	39	P2.4/T2EX		Control Input to Timer 2. When enabled, a negative transition on the T2EX input pin causes a Timer 2 capture or reload event.
37	40	P2.5/PWM0		If the PWM is enabled, the PWM0 output appears at this pin.
38	41	P2.6/PWM1		If the PWM is enabled, the PWM1 output appears at this pin.
39	42	P2.7/PWMCLK		If the PWM is enabled, an external PWM clock can be provided at this pin.
32	34	XTAL1	I	Input to the Crystal Oscillator Inverter.
33	35	XTAL2	O	Output from the Crystal Oscillator Inverter. See the Hardware Design Considerations section for a description.
40	43	$\overline{EA}$		External Access Enable, Logic Input. When held high, this input enables the device to fetch code from internal program memory locations 0000H to F7FFH. No external program memory access is available on the ADuC845, ADuC847, or ADuC848. To determine the mode of code execution, the $\overline{EA}$ pin is sampled at the end of an external RESET assertion or as part of a device power cycle. $\overline{EA}$ can also be used as an external emulation I/O pin, and therefore the voltage level at this pin must not be changed during normal operation because this might cause an emulation interrupt that halts code execution.
41	44	$\overline{PSEN}$	O	Program Store Enable, Logic Output. This function is not used on the ADuC845, ADuC847, or ADuC848. This pin remains high during internal program execution. $\overline{PSEN}$ can also be used to enable serial download mode when pulled low through a resistor at the end of an external RESET assertion or as part of a device power cycle.
42	45	ALE	O	Address Latch Enable, Logic Output. This output is used to latch the low byte (and page byte for 24-bit data address space accesses) of the address to external memory during external data memory access cycles. It can be disabled by setting the PCON.4 bit in the PCON SFR.

Power Control Register (PCON)

The PCON SFR contains bits for power-saving options and general-purpose status flags as listed in Table 6.

SFR Address: 87H
Power-On Default: 00H
Bit Addressable: No

Table 6. PCON SFR Bit Designations

Bit No.	Name	Description
7	SMOD	Double UART Baud Rate. 0 = Normal, 1 = Double Baud Rate.
6	SERIPD	Serial Power-Down Interrupt Enable. If this bit is set, a serial interrupt from either SPI or I^2C can terminate the power-down mode.
5	INT0PD	INT0 Power-Down Interrupt Enable. If this bit is set, either a level ($\overline{IT0}$ = 0) or a negative-going transition ($\overline{IT0}$ = 1) on the INT0 pin terminates power-down mode.
4	ALEOFF	If set to 1, the ALE output is disabled.
3	GF1	General-Purpose Flag Bit.
2	GF0	General-Purpose Flag Bit.
1	PD	Power-Down Mode Enable. If set to 1, the device enters power-down mode.
0	-----	Not Implemented. Write Don't Care.

ADuC845/ADuC847/ADuC848 Configuration Register (CFG845/CFG847/CFG848)

The CFG845/CFG847/CFG848 SFR contains the bits necessary to configure the internal XRAM and the extended SP. By default, it configures the user into 8051 mode, that is, extended SP, and the internal XRAM are disabled. When using in a program, use the device name only, that is, CFG845, CFG847, or CFG848.

SFR Address: AFH
Power-On Default: 00H
Bit Addressable: No

Table 7. CFG845/CFG847/CFG848 SFR Bit Designations

Bit No.	Name	Description
7	EXSP	Extended SP Enable. If this bit is set to 1, the stack rolls over from SPH/SP = 00FFH to 0100H. If this bit is cleared to 0, SPH SFR is disabled and the stack rolls over from SP = FFH to SP = 00H.
6	----	Not Implemented. Write Don't Care.
5	----	Not Implemented. Write Don't Care.
4	----	Not Implemented. Write Don't Care.
3	----	Not Implemented. Write Don't Care.
2	----	Not Implemented. Write Don't Care.
1	----	Not Implemented. Write Don't Care.
0	XRAMEN	If this bit is set to 1, the internal XRAM is mapped into the lower 2 kbytes of the external address space. If this bit is cleared to 0, the internal XRAM is accessible and up to 16 MB of external data memory become available. See Figure 8.

Signal Chain Overview (Chop Enabled, $\overline{CHOP}$ = 0)

With the $\overline{CHOP}$ bit = 0 (see the ADCMODE SFR bit designations in Table 24), the chopping scheme is enabled. This is the default condition and gives optimum performance in terms of offset errors and drift performance. With chop enabled, the available output rates vary from 5.35 Hz to 105 Hz (SF = 255 and 13, respectively). A typical block diagram of the ADC input channel with chop enabled is shown in Figure 12.

The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency. The output of the Σ-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band limited, low noise output from the ADCs.

The ADC filter is a low-pass Sinc^3 or (sinx/x)^3 filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the Sinc filter word loaded into the filter (SF) register (see Table 28). The complete signal chain is chopped, resulting in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important.

With chop enabled, the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc^3 filter, therefore, have a positive offset and a negative offset term included. As a result, a final summing stage is included so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data register. Programming the Sinc^3 decimation factor is restricted to an 8-bit register called SF (see Table 28), the actual decimation factor is the register value times 8. Therefore, the decimated output rate from the Sinc^3 filter (and the ADC conversion rate) is

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

where:
f_{ADC} is the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The chop rate of the channel is half the output data rate:

$$f_{CHOP} = \frac{1}{2 \times f_{ADC}}$$

As shown in the block diagram (Figure 12), the Sinc^3 filter outputs alternately contain $+V_{OS}$ and $-V_{OS}$, where V_{OS} is the respective channel offset.

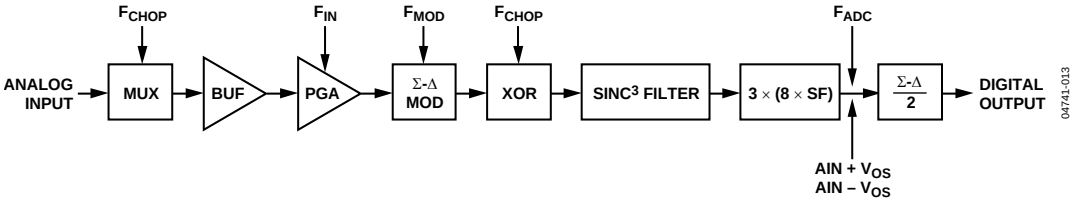

Figure 12. Block Diagram of the ADC Input Channel with Chop Enabled

Signal Chain Overview with Chop Disabled ($\overline{CHOP}$ = 1)

With $\overline{CHOP}$ = 1, chop is disabled and the available output rates vary from 16.06 Hz to 1.365 kHz. The range of applicable SF words is from 3 to 255. When switching between channels with chop disabled, the channel throughput rate is higher than when chop is enabled. The drawback with chop disabled is that the drift performance is degraded and offset calibration is required following a gain range change or significant temperature change. A block diagram of the ADC input channel with chop disabled is shown in Figure 15.

The signal chain includes a multiplex or buffer, PGA, Σ-Δ modulator, and digital filter. The modulator bit stream is applied to a Sinc^3 filter. Programming the Sinc^3 decimation factor is restricted to an 8-bit register SF; the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) is therefore

$$f_{ADC} = \frac{1}{8 \times SF} \times f_{MOD}$$

where:
f_{ADC} is the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register, valid range is from 3 to 255.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The settling time to a step input is governed by the digital filter. A synchronized step change requires a settling time of three times the programmed update rate; a channel change can be treated as a synchronized step change. This is one conversion longer than the case for chop enabled. However, because the ADC throughput is three times faster with chop disabled than it is with chop enabled, the actual time to a settled ADC output is significantly less also. This means that following a synchronized step change, the ADC requires three conversions (note: data is not output following a synchronized ADC change until data has settled) before the result accurately reflects the new input voltage.

$$t_{SETTLE} = \frac{3}{f_{ADC}} = 3 \times t_{ADC}$$

An unsynchronized step change requires four conversions to accurately reflect the new analog input at its output. Note that with an unsynchronized change the ADC continues to output data and so the user must take unsettled outputs into account. Again, this is one conversion longer than with chop enabled, but because the ADC throughput with chop disabled is faster than with chop enabled, the actual time taken to obtain a settled ADC output is less.

The allowable range for SF is 3 to 255 with a default of 69 (45H). The corresponding conversion rates, rms, and peak-to-peak noise performances are shown in Table 14, Table 15, Table 16, and Table 17. Note that the conversion time increases by 0.244 ms for each increment in SF.

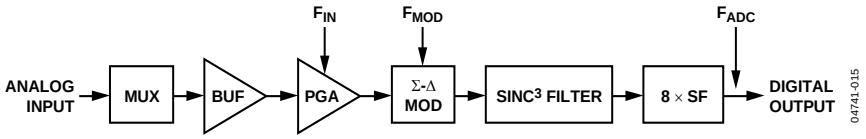

Figure 15. Block Diagram of ADC Input Channel with Chop Disabled

ADC Noise Performance with Chop Disabled ($\overline{CHOP}$ = 1)

Table 14 through Table 17 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. Note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution. Typically, the performance of the ADC with chop disabled shows a 0.5 LSB degradation over the performance with chop enabled.

Table 14. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
68	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 15. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	17	17	17.5	18
82	49.95	13	14	15	16	16.5	17.5	18	18
255	16.06	13.5	14.5	15.5	16.5	17.5	18.5	18.5	19

Table 16. ADuC848 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
69	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 17. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320mV	±640mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	16	16	16	16
82	49.95	13	14	15	16	16	16	16	16
255	16.06	13.5	14.5	15.5	16	16	16	16	16

that the internal calibration procedure for full-scale calibration automatically selects the reference in voltage at PGA = 1.

Therefore, the full-scale endpoint calibration automatically subtracts the offset calibration error, it is advisable to perform an offset calibration at the same gain range as that used for full-scale calibration. There is no penalty to the full-scale calibration in redoing the zero-scale calibration at the required PGA range because the full-scale calibration has very good matching at all the PGA ranges.

This procedure also applies when chop is disabled.

Note that for internal calibration to be effective, the AIN− pin should be held at a steady voltage, within the allowable common-mode range to keep it from floating during calibration.

System Calibration Example

With chop enabled, a system zero-scale or offset calibration should never be required. However, if a full-scale or gain calibration is required for any reason, use the following typical procedure for doing so.

1. Apply a differential voltage of 0 V to the selected analog inputs (AIN+ to AIN−) that are held at a common-mode voltage.

   Perform a system zero-scale or offset calibration by setting the MD2...0 bits in the ADCMODE register to 110B.

2. Apply a full-scale differential voltage across the ADC inputs again at the same common-mode voltage.

   Perform a system full-scale or gain calibration by setting the MD2...0 bits in the ADCMODE register to 111B.

Perform a system calibration at the required PGA range to be used since the ADC scales to the differential voltages that are applied to the ADC during the calibration routines.

In bipolar mode, the zero-scale calibration determines the mid-scale point of the ADC (800000H) or 0 V.

PROGRAMMABLE GAIN AMPLIFIER

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different ranges, which are programmed via the range bits (RN0 to RN2) in the ADC0CON1 register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V and 0 V to 2.56 V, while in bipolar mode the ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±64 0 mV, ±1.28 V, and ±2.56 V. These ranges should appear on the input to the on-chip PGA. The ADC range-matching specification of 2 µV (typical with chop enabled) means that calibration need only be carried out on a single range and need not be repeated when the ADC range is changed. This is a significant advantage compared to similar mixed-signal solutions available on the market. The auxiliary (ADuC845 only) ADC does not incorporate a PGA, and the gain is fixed at 0 V to 2.50 V in unipolar mode, and ±2.50 V in bipolar mode.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog inputs of the ADuC845/ADuC847/ADuC848 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the device can handle negative voltages with respect to system AGND, but rather with respect to the negative reference input. Unipolar and bipolar signals on the AIN(+) input on the ADC are referenced to the voltage on the respective AIN(−) input. AIN(+) and AIN(−) refer to the signals seen by the ADC.

For example, if AIN(−) is biased to 2.5 V (tied to the external reference voltage) and the ADC is configured for a unipolar analog input range of 0 mV to >20 mV, the input voltage range on AIN(+) is 2.5 V to 2.52 V. On the other hand, if AIN(−) is biased to 2.5 V (again the external reference voltage) and the ADC is configured for a bipolar analog input range of ±1.28 V, the analog input range on the AIN(+) is 1.22 V to 3.78 V, that is, 2.5 V ± 1.28 V.

The modes of operation for the ADC are fully differential mode or pseudo differential mode. In fully differential mode, AIN1 to AIN2 are one differential pair, and AIN3 to AIN4 are another pair (AIN5 to AIN6, AIN7 to AIN8, and AIN9 to AIN10 are the others). In differential mode, all AIN(−) pin names imply the negative analog input of the selected differential pair, that is, AIN2, AIN4, AIN6, AIN8, AIN10. The term AIN(+) implies the positive input of the selected differential pair, that is, AIN1, AIN3, AIN5, AIN7, AIN9. In pseudo differential mode, each analog input is paired with the AINCOM pin, which can be biased up or tied to AGND. In this mode, the AIN(−) implies AINCOM, and AIN(+) implies any one of the ten analog input channels.

The configuration of the inputs (unipolar vs. bipolar) is shown in Figure 17.

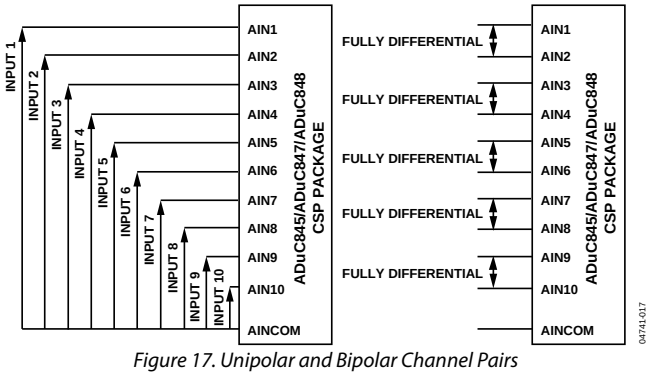

Figure 17. Unipolar and Bipolar Channel Pairs

ADCSTAT (ADC STATUS REGISTER)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including REFIN± reference detect and conversion overflow/underflow flags.

SFR Address: D8H
Power-On Default: 00H
Bit Addressable: Yes

Table 23. ADCSTAT SFR Bit Designation

Bit No.	Name	Description
7	RDY0	Ready Bit for the Primary ADC. Set by hardware on completion of conversion or calibration. Cleared directly by the user, or indirectly by a write to the mode bits, to start calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary (ADuC845 only) ADC. Same definition as RDY0 referred to the auxiliary ADC. Valid on the ADuC845 only.
5	CAL	Calibration Status Bit. Set by hardware on completion of calibration. Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration. Note that calibration with the temperature sensor selected (auxiliary ADC on the ADuC845 only) fails to complete.
4	NOXREF	No External Reference Bit (only active if primary or auxiliary (ADuC845 only) ADC is active). Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When set, conversion results are clamped to all 1s. Only detects invalid REFIN±, does not check REFIN2±. Cleared to indicate valid V_{REF}.
3	ERR0	Primary ADC Error Bit. Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC. Valid on the ADuC845 only.
1	–––	Not Implemented. Write Don't Care.
0	–––	Not Implemented. Write Don't Care.

ADC0CON2 (PRIMARY ADC CHANNEL SELECT REGISTER)

ADC0CON2 is used to select a reference source and channel for the primary ADC.

SFR Address: E6H
Power-On Default: 00H
Bit Addressable: No

Table 26. ADC0CON2 SFR Bit Designations

Bit No.	Name	Description
7, 6	XREF1, XREF0	Primary ADC External Reference Select Bit. Set by the user to enable the primary ADC to use the external reference via REFIN± or REFIN2±. Cleared by the user to enable the primary ADC to use the internal band gap reference (V_{REF} = 1.25 V). XREF1 XREF0 0 0 Internal 1.25 V Reference. 0 1 REFIN± Selected. 1 0 REFIN2± (AIN3/AIN4) Selected. 1 1 Reserved.
5	–––	Not Implemented. Write Don't Care.
4	–––	Not Implemented. Write Don't Care.
3, 2, 1, 0	CH3, CH2, CH1, CH0	Primary ADC Channel Select Bits. Written by the user to select the primary ADC channel as follows: CH3 CH2 CH1 CH0 Selected Primary ADC Input Channel. 0 0 0 0 AIN1–AINCOM 0 0 0 1 AIN2–AINCOM 0 0 1 0 AIN3–AINCOM 0 0 1 1 AIN4–AINCOM 0 1 0 0 AIN5–AINCOM 0 1 0 1 AIN6–AINCOM 0 1 1 0 AIN7–AINCOM 0 1 1 1 AIN8–AINCOM 1 0 0 0 AIN9–AINCOM (LFCSP package only; not a valid selection on the MQFP package) 1 0 0 1 AIN10–AINCOM (LFCSP package only; not a valid selection on the MQFP package) 1 0 1 0 AIN1–AIN2 1 0 1 1 AIN3–AIN4 1 1 0 0 AIN5–AIN6 1 1 0 1 AIN7–AIN8 1 1 1 0 AIN9–AIN10 (LFCSP package only; not a valid selection on the MQFP package) 1 1 1 1 AINCOM–AINCOM

Note that because the reference-detect does not operate on the REFIN2± pair, the REFIN2± pins can go below 1 V.

SPICON—SPI Control Register

SFR Address: F8H
Power-On Default: 05H
Bit Addressable: Yes

Table 41. SPICON SFR Bit Designations

Bit No.	Name	Description
7	ISPI	SPI Interrupt Bit. Set by the MicroConverter at the end of each SPI transfer. Cleared directly by user code or indirectly by reading the SPIDAT SFR.
6	WCOL	Write Collision Error Bit. Set by the MicroConverter if SPIDAT is written to while an SPI transfer is in progress. Cleared by user code.
5	SPE	SPI Interface Enable Bit. Set by user code to enable SPI functionality. Cleared by user code to enable standard Port 2 functionality.
4	SPIM	SPI Master/Slave Mode Select Bit. Set by user code to enable master mode operation (SCLOCK is an output). Cleared by user code to enable slave mode operation (SCLOCK is an input).
3	CPOL[1]	Clock Polarity Bit. Set by user code to enable SCLOCK idle high. Cleared by user code to enable SCLOCK idle low.
2	CPHA[1]	Clock Phase Select Bit. Set by user code if the leading SCLOCK edge is to transmit data. Cleared by user code if the trailing SCLOCK edge is to transmit data.
1, 0	SPR1, SPR0	SPI Bit-Rate Bits. SPR1 SPR0 Selected Bit Rate 0 0 $f_{core}/2$ 0 1 $f_{core}/4$ 1 0 $f_{core}/8$ 1 1 $f_{core}/16$

[1] The CPOL and CPHA bits should both contain the same values for master and slave devices.

Note that both SPI and I²C use the same ISR (Vector Address 3BH); therefore, when using SPI and I²C simultaneously, it is necessary to check the interfaces following an interrupt to determine which one caused the interrupt.

SPIDAT: SPI Data Register

SFR Address: 7FH
Power-On Default: 00H
Bit Addressable: No

P2.5 and P2.6 can also be used as PWM outputs, while P2.7 can act as an alternate PWM clock source. When selected as the PWM outputs, they overwrite anything written to P2.5 or P2.6.

Table 47. Port 2 Alternate Functions

Pin No.	Alternate Function
P2.0	SCLOCK for SPI
P2.1	MOSI for SPI
P2.2	MISO for SPI
P2.3	$\overline{SS}$ and T2 clock input
P2.4	T2EX alternate control for T2
P2.5	PWM0 output
P2.6	PWM1 output
P2.7	PWMCLK

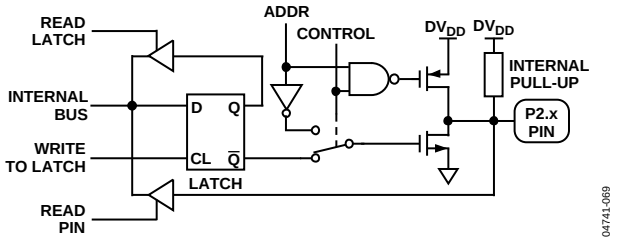

Figure 50. Port 2 Bit Latch and I/O Buffer

Port 3

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P3 SFR (B0H). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and, in that state, can be used as inputs. As inputs, Port 3 pins pulled externally low source current because of the internal pull-ups.

Port 3 pins with 0s written to them drive a logic low output voltage (V_{OL}) and are capable of sinking 4 mA. Port 3 pins also have various secondary functions as described in Table 48. The alternate functions of Port 3 pins can be activated only if the corresponding bit latch in the P3 SFR contains a 1. Otherwise, the port pin remains at 0.

Table 48. Port 3 Alternate Functions

Pin No.	Alternate Function
P3.0	RxD (UART input pin, or serial data I/O in Mode 0)
P3.1	TxD (UART output pin, or serial clock output in Mode 0)
P3.2	$\overline{INT0}$ (External Interrupt 0)
P3.3	$\overline{INT1}$ (External Interrupt 1)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

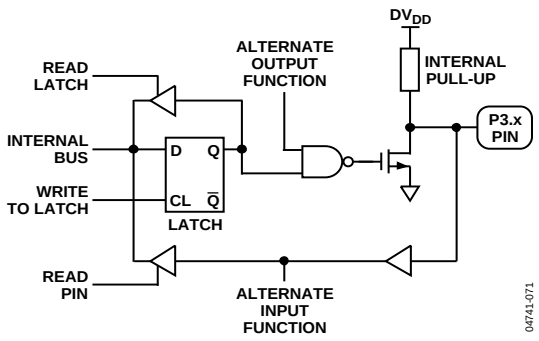

Figure 51. Port 3 Bit Latch and I/O Buffer

Read-Modify-Write Instructions

Some 8051 instructions read the latch while others read the pin. The instructions that read the latch rather than the pins are the ones that read a value, possibly change it, and rewrite it to the latch. These are called read-modify-write instructions, which are listed in Table 49. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 49. Read-Modify-Write Instructions

Instruction	Description
ANL	Logical AND, for example, ANL P1, A
ORL	Logical OR, for example, ORL P2, A
XRL	Logical EX-OR, for example, XRL P3, A
JBC	Jump if Bit = 1 and clear bit, for example, JBC P1.1, LABEL
CPL	Complement bit, for example, CPL P3.0
INC	Increment, for example, INC P2
DEC	Decrement, for example, DEC P2
DJNZ	Decrement and jump if not zero, for example, DJNZ P3, LABEL
MOV PX.Y, C[1]	Move Carry to Bit Y of Port X
CLR PX.Y[1]	Clear Bit Y of Port X
SETB PX.Y[1]	Set Bit Y of Port X

[1] These instructions read the port byte (all 8 bits), modify the addressed bit, and write the new byte back to the latch.

Read-modify-write instructions are directed to the latch rather than to the pin to avoid a possible misinterpretation of the voltage level of a pin. For example, a port pin might be used to drive the base of a transistor. When 1 is written to the bit, the transistor is turned on. If the CPU reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as Logic 0. Reading the latch rather than the pin returns the correct value of 1.

Timer/Counter 2 Operating Modes

The following sections describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table 53.

Table 53. T2CON Operating Modes

RCLK (or) TCLK	CAP2	TR2	Mode
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	Off

16-Bit Autoreload Mode

Autoreload mode has two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. Autoreload mode is shown in Figure 56.

16-Bit Capture Mode

Capture mode has two options that are selected by Bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter that, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into Registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes Bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is shown in Figure 57. The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore, Timer 2 interrupts do not occur, so they do not have to be disabled. In this mode, the EXF2 flag can, however, still cause interrupts, which can be used as a third external interrupt. Baud rate generation is described as part of the UART serial port operation in the following section.

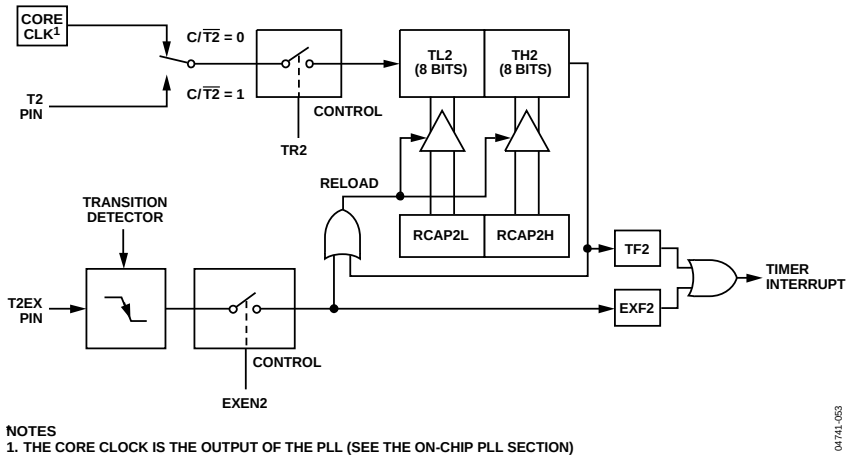

Figure 56. Timer/Counter 2, 16-Bit Autoreload Mode

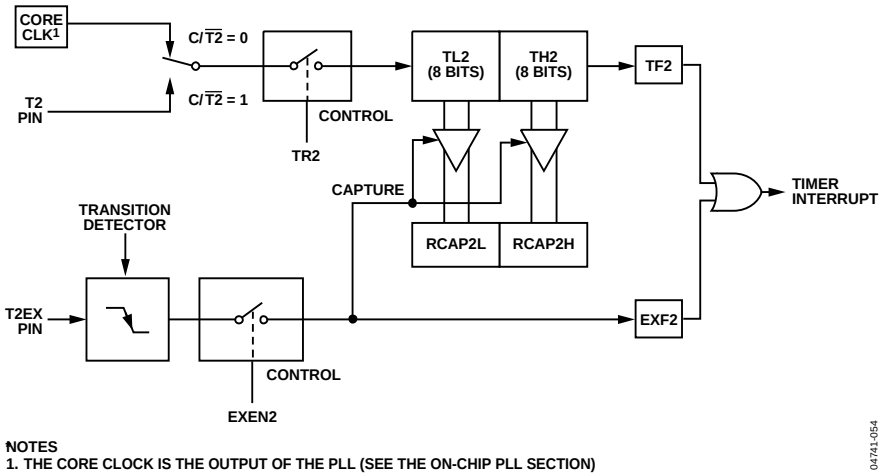

Figure 57. Timer/Counter 2, 16-Bit Capture Mode

Mode 0 (8-Bit Shift Register Mode)

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The 8 bits are transmitted with the least significant bit (LSB) first.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line, and the clock pulses are output from the TxD line as shown in Figure 58.

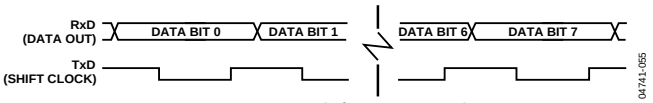

Figure 58. 8-Bit Shift Register Mode

Mode 1 (8-Bit UART, Variable Baud Rate)

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (0) and followed by a stop bit (1). Therefore, 10 bits are transmitted on TxD or are received on RxD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The write to SBUF signal also loads a 1 (stop bit) into the 9th bit position of the transmit shift register. The data is output bit-by-bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 59.

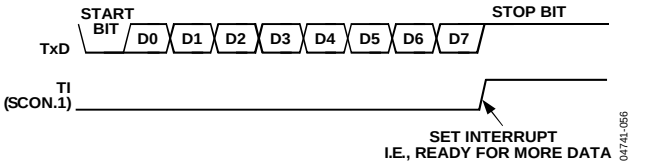

Figure 59. 8-Bit Variable Baud Rate

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming that a valid start bit is detected, character reception continues. The start bit is skipped and the 8 data bits are clocked into the serial port shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th bit (stop bit) is clocked into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is *not* met, the received frame is irretrievably lost, and RI is not set.

Mode 2 (9-Bit UART with Fixed Baud Rate)

Mode 2 is selected by setting SM0 and clearing SM1. In this mode, the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at Core_Clk/64 by default, although by setting the SMOD bit in PCON, the frequency can be doubled to Core_Clk/32. Eleven bits are transmitted or received: a start bit (0), 8 data bits, a programmable 9th bit, and a stop bit (1). The 9th bit is most often used as a parity bit, although it can be used for anything, including a ninth data bit if required.

To transmit, the 8 data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated, the 8 data bits (from SBUF) are loaded into the transmit shift register (LSB first). The contents of TB8 are loaded into the 9th bit position of the transmit shift register. The transmission starts at the next valid baud rate clock. The TI flag is set as soon as the stop bit appears on TxD.

Reception for Mode 2 is similar to that of Mode 1. The 8 data bytes are input at RxD (LSB first) and loaded onto the receive shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th data bit is latched into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART Serial Port Baud Rate Generation

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(\frac{CoreClockFrequency}{12}\right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Core\ Clock\ Frequency$$

Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or in both (one for transmit and the other for receive).

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{CoreClockFrequency}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{1}{16} \times Timer\ 2\ Overflow\ Rate$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 60.

In this case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{Core\ \ Clock\ \ Frequency}{(16 \times [65536\ - (RCAP\ 2H\ :RCAP\ 2L)])}$$

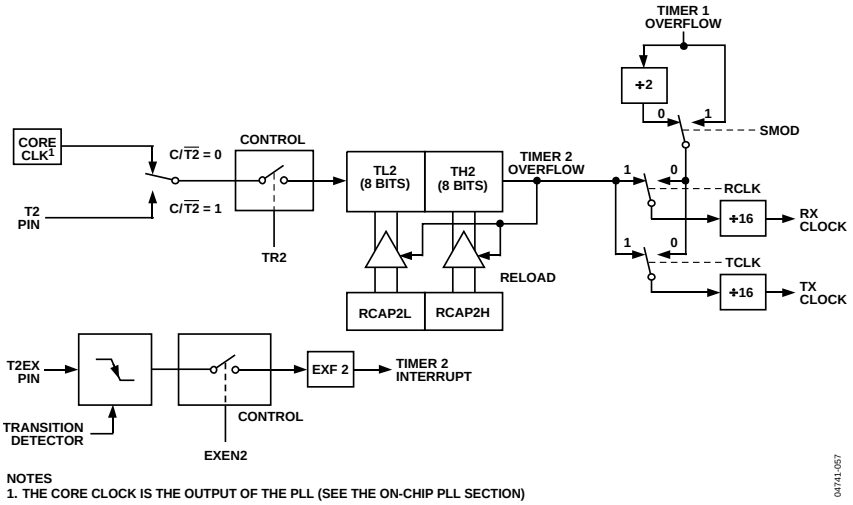

Figure 60. Timer 2, UART Baud Rates

Table 66. EXTERNAL DATA MEMORY WRITE CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{WLWH}	$\overline{WR}$ Pulse Width	65		130		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	65		135		ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low		130		260	ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	60		120		ns
t_{QVWH}	Data Setup Before $\overline{WR}$	120		250		ns
t_{WHQX}	Data and Address Hold After $\overline{WR}$	380		755		ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		125		ns

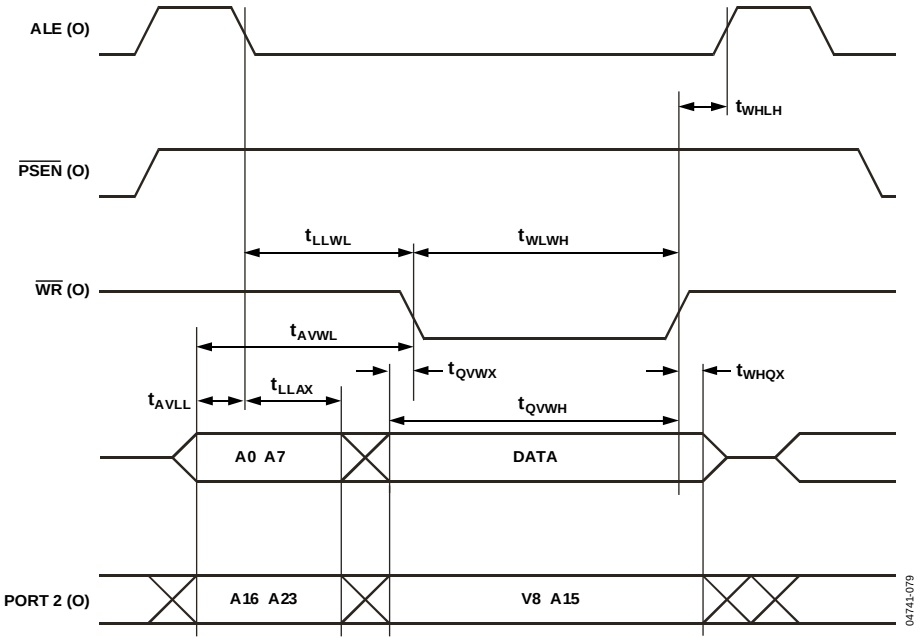

Figure 74. External Data Memory Write Cycle

Table 67. I²C-COMPATIBLE INTERFACE TIMING Parameter

Parameter		Min	Max	Unit
t_L	SCLCK Low Pulse Width	1.3		µs
t_H	SCLCK High Pulse Width	0.6		µs
t_{SHD}	Start Condition Hold Time	0.6		µs
t_{DSU}	Data Setup Time	100		µs
t_{DHD}	Data Hold Time		0.9	µs
t_{RSU}	Setup Time for Repeated Start	0.6		µs
t_{PSU}	Stop Condition Setup Time	0.6		µs
t_{BUF}	Bus Free Time Between a Stop Condition and a Start Condition	1.3		µs
t_R	Rise Time of Both SCLCK and SDATA		300	ns
t_F	Fall Time of Both SCLCK and SDATA		300	ns
t_{SUP}[1]	Pulse Width of Spike Suppressed		50	ns

[1] Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

Table 69. SPI MASTER MODE TIMING (CPHA = 0) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		635		ns
t_{SH}	SCLOCK High Pulse Width[1]		635		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DOSU}	Data Output Setup Before SCLOCK Edge			150	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 1.57 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

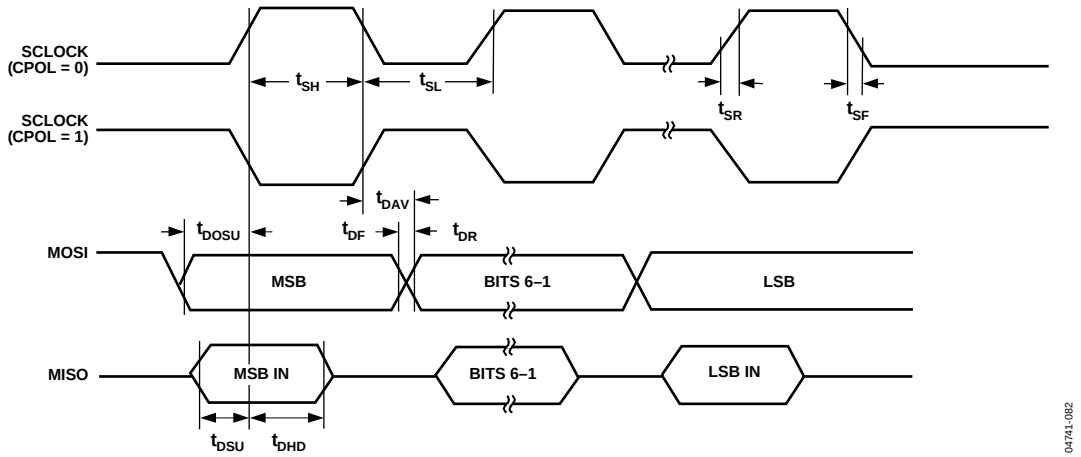

Figure 77. SPI Master Mode Timing (CHPA = 0)

Table 72. UART TIMING (SHIFT REGISTER MODE) Parameter

		12.58 MHz Core_Clk			Variable Core_Clk			
		Min	Typ	Max	Min	Typ	Max	Unit
TXLXL	Serial Port Clock Cycle Time		954			$12t_{core}$		ns
TQVXH	Output Data Setup to Clock	662						ns
TDVXH	Input Data Setup to Clock	292						ns
TXHDX	Input Data Hold After Clock	0						ns
TXHQX	Output Data Hold After Clock	22						ns

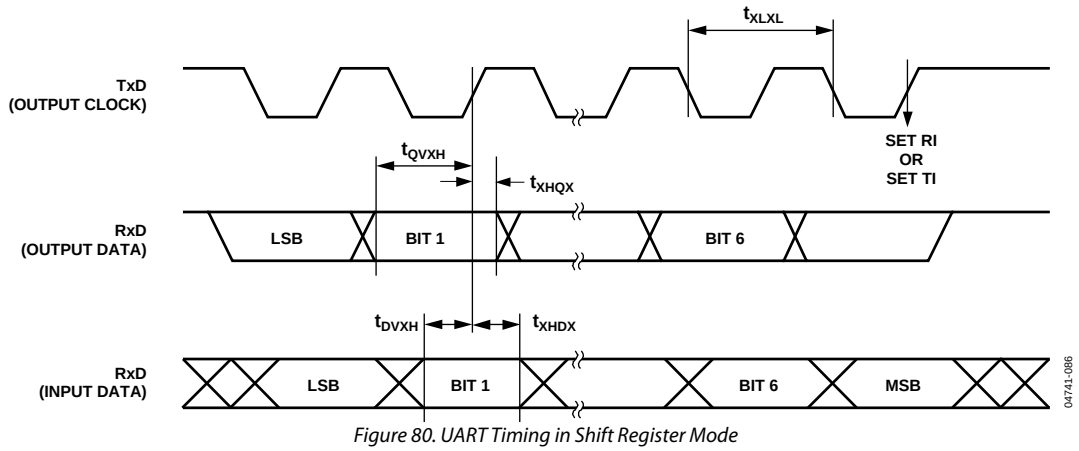

Figure 80. UART Timing in Shift Register Mode

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADuC845BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC845BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC845BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC845BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC845BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC845BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC847BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC847BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC847BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC847BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC847BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC847BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC847BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC847BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC847BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC847BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC848BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC848BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC848BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC848BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC848BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC848BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC848BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC848BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC848BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC848BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
EVAL-ADuC845QSZ		QuickStart Development System	
EVAL-ADuC845QSPZ		QuickStart-PLUS Development System	
EVAL-ADuC847QSZ		QuickStart Development System	
EVAL-ADUC-CABLE1Z		ADuC Serial Downloader Cable for UART	

[1] The -3 and -5 in the Model column indicate the DV_{DD} operating voltage.
[2] Z = RoHS Compliant Part.
[3] The QuickStart Plus system can only be ordered directly from Accutron. It can be purchased from the website http://www.accutron.com.

NOTES