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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 10x16b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc848bsz32-5

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Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AUXILIARY ADC ANALOG INPUTS (ADuC845 ONLY)					
Differential Input Voltage Ranges[5,6]					
Bipolar Mode (ADC1CON.5 = 0)		$\pm V_{REF}$		V	REFIN = REFIN(+) − REFIN(−) (or Int 1.25 V_{REF})
Unipolar Mode (ADC1CON.5 = 1)		0 − V_{REF}		V	REFIN = REFIN(+) − REFIN(−) (or Int 1.25 V_{REF})
Average Analog Input Current		125		nA/V	
Analog Input Current Drift		±2		pA/V/°C	
Absolute AIN/AINCOM Voltage Limits[2,7]	A_{GND} − 0.03		AV_{DD} + 0.03	V	
Normal Mode Rejection 50 Hz/60 Hz[2]					
On AIN and REFIN	75			dB	50 Hz/60 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on, REJ60 on
	100			dB	50 Hz ± 1 Hz, 16.6 Hz Fadc, SF = 52H, chop on
	67			dB	50 Hz/60 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off, REJ60 on
	100			dB	50 Hz ± 1 Hz, 50 Hz Fadc, SF = 52H, chop off
ADC SYSTEM CALIBRATION					
Full-Scale Calibration Limit			+1.05 × FS	V	
Zero-Scale Calibration Limit	−1.05 × FS			V	
Input Span	0.8 × FS		2.1 × FS	V	
DAC					
Voltage Range		0 − V_{REF}		V	DACCON.2 = 0
		0 − AV_{DD}		V	DACCON.2 = 1
Resistive Load		10		kΩ	From DAC output to AGND
Capactive Load		100		pF	From DAC output to AGND
Output Impedance		0.5		Ω	
I_{SINK}		50		µA	
DC Specifications[8]					
Resolution	12			Bits	
Relative Accuracy		±3		LSB	
Differential Nonlinearity			−1	LSB	Guaranteed 12-bit monotonic
Offset Error			±50	mV	
Gain Error			±1	%	AV_{DD} range
		±1		%	V_{REF} range
AC Specifications[2,8]					
Voltage Output Settling Time		15		µs	Settling time to 1 LSB of final value
Digital-to-Analog Glitch Energy		10		nVs	1 LSB change at major carry
INTERNAL REFERENCE					
ADC Reference					Chop enabled
Reference Voltage	1.25 − 1%	1.25	1.25 + 1%	V	Initial tolerance @ 25°C, V_{DD} = 5 V
Power Supply Rejection		45		dB	
Reference Tempco		100		ppm/°C	
DAC Reference					
Reference Voltage	2.5 − 1%	2.5	2.5 + 1%	±1% V	Initial tolerance @ 25°C, V_{DD} = 5 V
Power Supply Rejection		50		dB	
Reference Tempco		±100		ppm/°C	
TEMPERATURE SENSOR (ADuC845 ONLY)					
Accuracy		±2		°C	
Thermal Impedance		90		°C/W	MQFP
		52		°C/W	LFCSP

GENERAL DESCRIPTION

The ADuC845, ADuC847, and ADuC848 are single-cycle, 12.58 MIPs, 8052 core upgrades to the ADuC834 and ADuC836. They include additional analog inputs for applications requiring more ADC channels.

The ADuC845, ADuC847, and ADuC848 are complete smart transducer front ends. The family integrates high resolution Σ-Δ ADCs with flexible, up to 10-channel, input multiplexing, a fast 8-bit MCU, and program and data Flash/EE memory on a single chip.

The ADuC845 includes two (primary and auxiliary) 24-bit Σ-Δ ADCs with internal buffering and PGA on the primary ADC. The ADuC847 includes the same primary ADC as the ADuC845 (auxiliary ADC removed). The ADuC848 is a 16-bit ADC version of the ADuC847.

The ADCs incorporate flexible input multiplexing, a temperature sensor (ADuC845 only), and a PGA (primary ADC only) allowing direct measurement of low-level signals. The ADCs include on-chip digital filtering and programmable output data rates that are intended for measuring wide dynamic range and low frequency signals, such as those in weigh scale, strain gage, pressure transducer, or temperature measurement applications.

The devices operate from a 32 kHz crystal with an on-chip PLL generating a high frequency clock of 12.58 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an optimized single-cycle 8052 offering up to 12.58 MIPs performance while maintaining 8051 instruction set compatibility.

The available nonvolatile Flash/EE program memory options are 62 kbytes, 32 kbytes, and 8 kbytes. 4 kbytes of nonvolatile Flash/EE data memory and 2304 bytes of data RAM are also provided on-chip. The program memory can be configured as data memory to give up to 60 kbytes of NV data memory in data logging applications.

On-chip factory firmware supports in-circuit serial download and debug modes (via UART), as well as single-pin emulation mode via the $\overline{EA}$ pin. The ADuC845, ADuC847, and ADuC848 are supported by the QuickStart™ development system featuring low cost software and hardware development tools.

This offset is removed by performing a running average of 2. This average by 2 means that the settling time to any change in programming of the ADC is twice the normal conversion time, while an asynchronous step change on the analog input is not fully reflected until the third subsequent output. See Figure 13.

$$t_{SETTLE} = \frac{2}{f_{ADC}} = 2 \times t_{ADC}$$

The allowable range for SF (chop enabled) is 13 to 255 with a default of 69 (45H). The corresponding conversion rates, rms and peak-to-peak noise performances are shown in Table 10, Table 11, Table 12, and Table 13. The numbers are typical and generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. Note that the conversion time increases by 0.732 ms for each increment in SF.

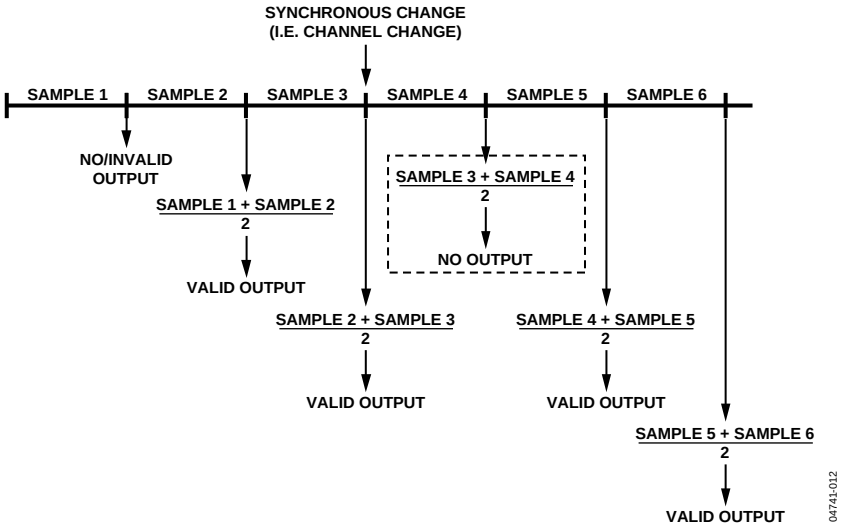

Figure 13. ADC Settling Time Following a Synchronous Change with Chop Enabled

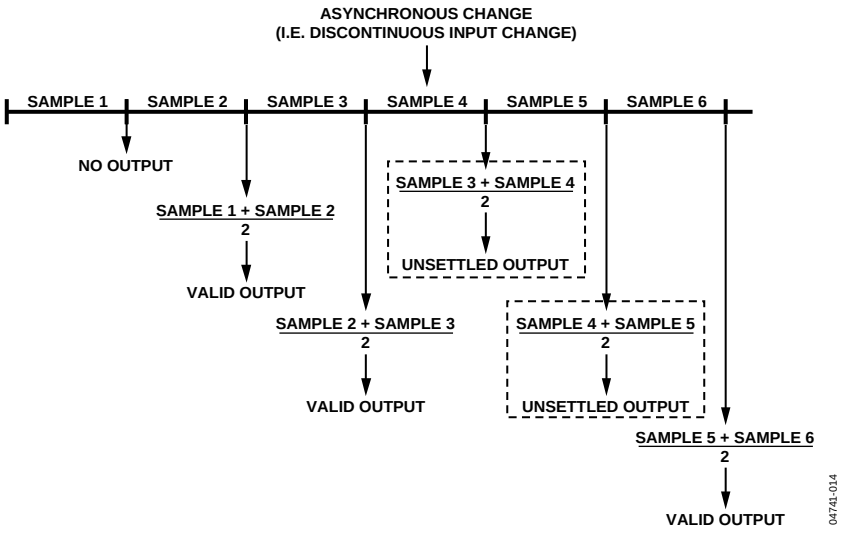

Figure 14. ADC Settling Time Following an Asynchronous Change with Chop Enabled

(see Table 30). These burnout current sources are also available only with buffering enabled via the BUF0/BUF1 bits in the ADC0CON1 SFR. Once the burnout currents are turned on, a current flows in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. When the resulting voltage measured is full scale, the transducer has gone open circuit. When the voltage measured is 0 V, this indicates that the transducer has gone short circuit. The current sources work over the normal absolute input voltage range specifications.

REFERENCE DETECT CIRCUIT

The main and auxiliary (ADuC845 only) ADCs can be configured to allow the use of the internal band gap reference or an external reference that is applied to the REFIN± pins by means of the XREF0/1 bit in the Control Registers AD0CON2 and AD1CON (ADuC845 only). A reference detection circuit is provided to detect whether a valid voltage is applied to the REFIN± pins. This feature arose in connection with strain-gage sensors in weigh scales where the reference and signal are provided via a cable from the remote sensor. It is desirable to detect whether the cable is disconnected. If either of the pins is floating or if the applied voltage is below a specified threshold, a flag (NOXREF) is set in the ADC status register (ADCSTAT), conversion results are clamped, and calibration registers are not updated if a calibration is in progress.

Note that the reference detect does not look at REFIN2± pins.

If, during either an offset or gain calibration, the NOEXREF bit becomes active, indicating an incorrect V_{REF}, updating the relevant calibration register is inhibited to avoid loading incorrect data into these registers, and the appropriate bits in ADCSTAT (ERR0 or ERR1) are set. If the user needs to verify that a valid reference is in place every time a calibration is performed, the status of the ERR0 and ERR1 bits should be checked at the end of every calibration cycle.

SINC FILTER REGISTER (SF)

The number entered into the SF register sets the decimation factor of the Sinc^3 filter for the ADC. See Table 28 and Table 29.

The range of operation of the SF word depends on whether ADC chop is on or off. With chop disabled, the minimum SF word is 3 and the maximum is 255. This gives an ADC throughput rate from 16.06 Hz to 1.365 kHz. With chop enabled, the minimum SF word is 13 (all values lower than 13 are clamped to 13) and the maximum is 255. This gives an ADC throughput rate of 5.4 Hz to 105 Hz. See the f_{ADC} equation in the ADC description preceding section.

An additional feature of the Sinc^3 filter is a second notch filter positioned in the frequency response at 60 Hz. This gives simultaneous 60 Hz rejection to whatever notch is defined by the SF filter. This 60 Hz filter is enabled via the REJ60 bit in the ADCMODE register (ADCMODE.6). The notch is valid only for SF words ≥ 68; otherwise, ADC errors occur, and, the notch is best used with an SF word of 82d giving simultaneous 50 Hz and 60 Hz rejection. This function is useful only with an ADC clock (modulator rate) of 32.768 kHz. During calibration, the current (user-written) value of the SF register is used.

Σ-Δ MODULATOR

A Σ-Δ ADC usually consists of two main blocks, an analog modulator, and a digital filter. For the ADuC845/ADuC847/ADuC848, the analog modulator consists of a difference amplifier, an integrator block, a comparator, and a feedback DAC as shown in Figure 16.

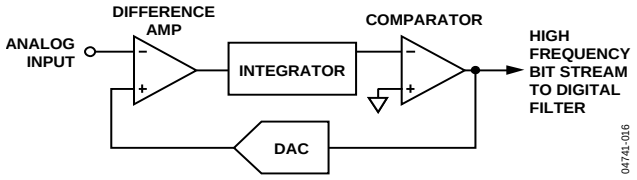

Figure 16. Σ-Δ Modulator Simplified Block Diagram

In operation, the analog signal is fed to the difference amplifier along with the output from the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output from the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data-word by using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (that results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency.

DIGITAL FILTER

The output of the ∑-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the device.

The ADuC845/ADuC847/ADuC848 filter is a low-pass, Sinc^3 or $[(SINx)/x]^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc filter) SFR as listed in Table 28 and Table 29.

Figure 22, Figure 23, Figure 24, and Figure 25 show the frequency response of the ADC, yielding an overall output rate of 16.6 Hz with chop enabled and 50 Hz with chop disabled. Also detailed in these plots is the effect of the fixed 60 Hz drop-in notch filter

DATA OUTPUT CODING

When the primary ADC is configured for unipolar operation, the output coding is natural (straight) binary with a zero differential input voltage resulting in a code of 000...000, a midscale voltage resulting in a code of 100...000, and a full-scale voltage resulting in a code of 111...111. The output code for any analog input voltage on the main ADC can be represented as follows:

$$Code - (AIN \times GAIN \times 2^N)/(1.024 \times V_{REF})$$

where:

AIN is the analog input voltage.
GAIN is the PGA gain setting, that is, 1 on the 2.56 V range and 128 on the 20 mV range, and $N = 24$ (16 on the ADuC848).

The output code for any analog input voltage on the auxiliary ADC can be represented as follows:

$$Code = (AIN \times 2^N)/(V_{REF})$$

with the same definitions as used for the primary ADC above.

When the primary ADC is configured for bipolar operation, the coding is offset binary with negative full-scale voltage resulting in a code of 000...000, a zero differential voltage resulting in a code of 800…000, and a positive full-scale voltage resulting in a code of 111...111. The output from the primary ADC for any analog input voltage can be represented as follows:

$$Code = 2^{N-1}[(AIN \times GAIN)/(1.024 \times V_{REF}) + 1]$$

where:

AIN is the analog input voltage.
GAIN is the PGA gain, that is, 1 on the ±2.56 V range and 128 on the ±20 mV range.
$N = 24$ (16 on the ADuC848).

The output from the auxiliary ADC in bipolar mode can be represented as follows:

$$Code = 2^{N-1}\ [(AIN/V_{REF}) + 1]$$

EXCITATION CURRENTS

The ADuC845/ADuC847/ADuC848 contain two matched, software-configurable 200 μA current sources. Both source current from AV_{DD}, which is directed to either or both of the IEXC1 (Pin 11 whose alternate functions are P1.6/AIN7) or IEXC2 (Pin 12, whose alternate functions are P1.7/AIN8) pins on the device. These currents are controlled via the lower four bits in the ICON register (Table 30). These bits not only enable the current sources but also allow the configuration of the currents such that 200 μA can be sourced individually from both pins or can be combined to give a 400 μA source from one or the other of the outputs. These sources can be used to excite external resistive bridge or RTD sensors (see Figure 71).

ADC POWER-ON

The ADC typically takes 0.5 ms to power up from an initial start-up sequence or following a power-down event.

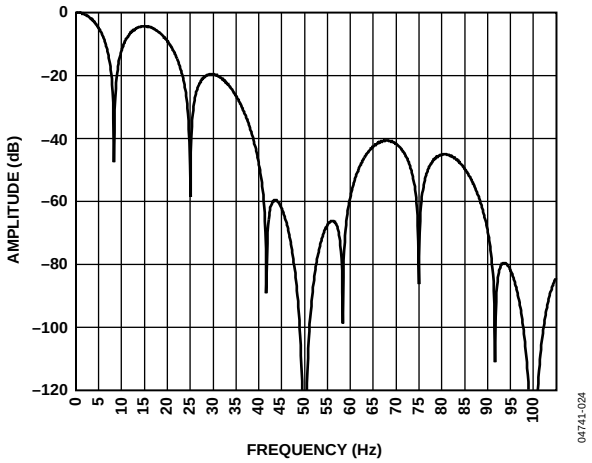

Figure 24. Chop On, Fadc = 16.6 Hz, SF = 52H

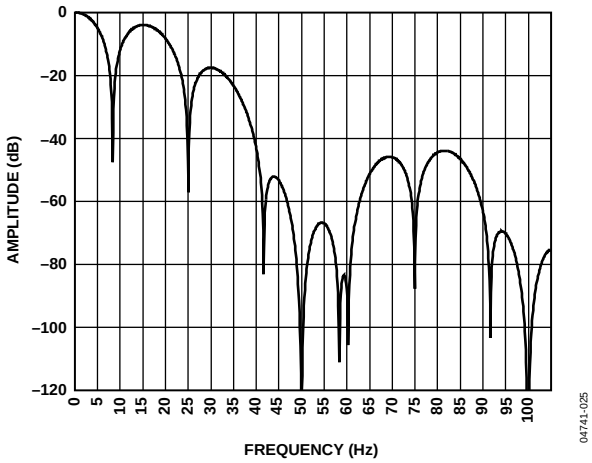

Figure 25. Chop On, Fadc = 16.6 Hz, SF = 52H, REJ60 Enabled

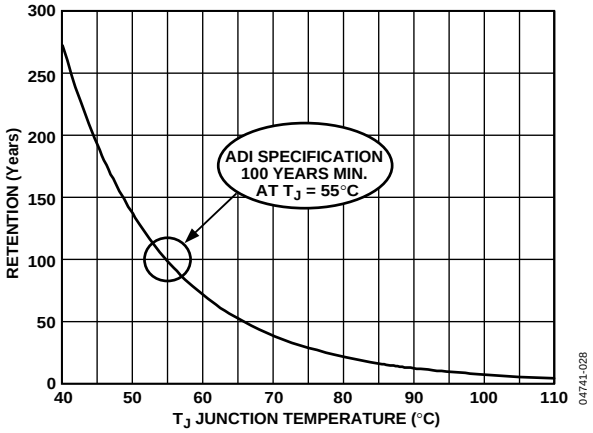

Figure 27. Flash/EE Memory Data Retention

FLASH/EE PROGRAM MEMORY

The ADuC845/ADuC847/ADuC848 contain a 64-kbyte array of Flash/EE program memory. The lower 62 kbytes of this program memory are available to the user for program storage or as additional NV data memory.

The upper 2 kbytes of this Flash/EE program memory array contain permanently embedded firmware, allowing in-circuit serial download, serial debug, and nonintrusive single-pin emulation. These 2 kbytes of embedded firmware also contain a power-on configuration routine that downloads factory calibrated coefficients to the various calibrated peripherals such as ADC, temperature sensor, current sources, band gap, and references.

These 2 kbytes of embedded firmware are hidden from the user code. Attempts to read this space read 0s; therefore, the embedded firmware appears as NOP instructions to user code.

In normal operating mode (power-on default), the 62 kbytes of user Flash/EE program memory appear as a single block. This block is used to store the user code as shown in Figure 28.

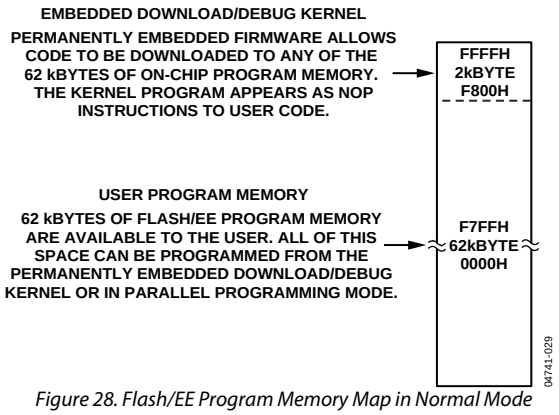

Figure 28. Flash/EE Program Memory Map in Normal Mode

In normal mode, the 62 kbytes of Flash/EE program memory can be programmed by serial downloading and by parallel programming.

Serial Downloading (In-Circuit Programming)

The ADuC845/ADuC847/ADuC848 facilitate code download via the standard UART serial port. The devices enter serial download mode after a reset or a power cycle if the $\overline{\text{PSEN}}$ pin is pulled low through an external 1 kΩ resistor. Once in serial download mode, the hidden embedded download kernel executes. This allows the user to download code to the full 62 kbytes of Flash/EE program memory while the device is in circuit in its target application hardware.

A PC serial download executable (WSD.EXE) is provided as part of the ADuC845/ADuC847/ADuC848 Quick Start development system. The AN-1074 Application Note fully describes the serial download protocol that is used by the embedded download kernel.

Parallel Programming

The parallel programming mode is fully compatible with conventional third-party flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 29. In this mode, Ports 0 and 2 operate as the external address bus interface, P3 operates as the external data bus interface, and P1.0 operates as the write enable strobe. P1.1, P1.2, P1.3, and P1.4 are used as general configuration ports that configure the device for various program and erase operations during parallel programming.

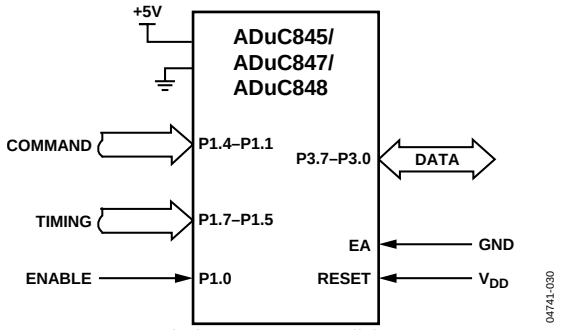

Figure 29. Flash/EE Memory Parallel Programming

The command words that are assigned to P1.1, P1.2, P1.3, and P1.4 are described in Table 31.

Table 31. Flash/EE Memory Parallel Programming Modes

Port 1 Pins				
P1.4	**P1.3**	**P1.2**	**P1.1**	**Programming Mode**
0	0	0	0	Erase Flash/EE Program, Data, and Security Mode
1	0	1	0	Program Code Byte
0	0	1	0	Program Data Byte
1	0	1	1	Read Code Byte
0	0	1	1	Read Data Byte
1	1	0	0	Program Security Modes
1	1	0	1	Read/Verify Security Modes
All other codes				Redundant

Table 36. PWM0L: PWM Pulse Width Low Byte

PWM0L.7	PWM0L.6	PWM0L.5	PWM0L.4	PWM0L.3	PWM0L.2	PWM0L.1	PWM0L.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Cycle Width High Byte (PWM1H)

SFR Address: B4H
Power-On Default: 00H
Bit Addressable: No

Table 37. PWM1H: PWM Cycle Width High Byte

PWM1H.7	PWM1H.6	PWM1H.5	PWM1H.4	PWM1H.3	PWM1H.2	PWM1H.1	PWM1H.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Cycle Width Low Byte (PWM1L)

SFR Address: B3H
Power-On Default: 00H
Bit Addressable: No

Table 38. PWM1L: PWM Cycle Width Low Byte

PWM1L.7	PWM1L.6	PWM1L.5	PWM1L.4	PWM1L.3	PWM1L.2	PWM1L.1	PWM1L.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Mode 0

In Mode 0, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal digital I/Os.

Mode 1 (Single-Variable Resolution PWM)

In Mode 1, both the pulse length and the cycle time (period) are programmable in user code, allowing the resolution of the PWM to be variable. PWM1H/L sets the period of the output waveform. Reducing PWM1H/L reduces the resolution of the PWM output but increases the maximum output rate of the PWM. For example, setting PWM1H/L to 65536 gives a 16-bit PWM with a maximum output rate of 192 Hz (12.583 MHz/65536). Setting PWM1H/L to 4096 gives a 12-bit PWM with a maximum output rate of 3072 Hz (12.583 MHz/4096).

PWM0H/L sets the duty cycle of the PWM output waveform as shown in Figure 39.

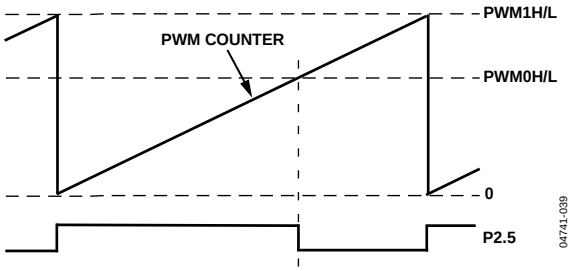

Figure 39. PWM in Mode 1

Mode 2 (Twin 8-Bit PWM)

In Mode 2, the duty cycle and the resolution of the PWM outputs are programmable. The maximum resolution of the PWM output is 8 bits.

PWM1L sets the period for both PWM outputs. Typically, this is set to 255 (FFH) to give an 8-bit PWM, although it is possible to reduce this as necessary. A value of 100 can be loaded here to give a percentage PWM, that is, the PWM is accurate to 1%.

Mode 5 (Dual 8-Bit PWM)

In Mode 5, the duty cycle and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

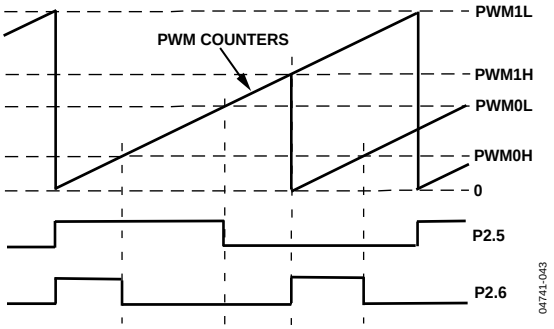

Figure 43. PWM Mode 5

Mode 6 (Dual RZ 16-Bit Σ-Δ DAC)

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4; however, the key difference is that Mode 6 provides return to zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. RZ mode ensures that any difference in the rise and fall times does not affect the Σ-Δ DAC INL. However, RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V– to AV_{DD} down to 0 V to $AV_{DD}/2$. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three full clocks (3 × 80 ns), high for one-half a clock (40 ns), and then low again for one-half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

The output resolution is set by the PWM1L and PWM1H SFRs for the P2.5 and P2.6 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P2.5 and P2.6, respectively. Both PWMs have the same clock source and clock divider.

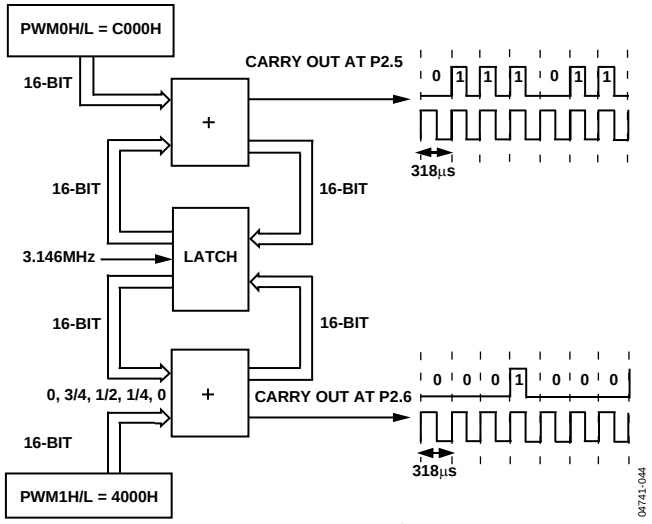

Figure 44. PWM Mode 6

Mode 7

In Mode 7, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal.

$\overline{SS}$ (Slave Select Input Pin)

Pin 31 (MQFP Package), Pin 33 (LFCSP Package)
The $\overline{SS}$ pin is used only when the ADuC845/ADuC847/ADuC848 are configured in SPI slave mode. This line is active low. Data is received or transmitted in slave mode only when the $\overline{SS}$ pin is low, allowing the devices to be used in single-master, multislave SPI configurations. If CPHA = 1, the $\overline{SS}$ input can be pulled low permanently. If CPHA = 0, the $\overline{SS}$ input must be driven low before the first bit in a byte-wide transmission or reception and must return high again after the last bit in that byte-wide transmission or reception. In SPI slave mode, the logic level on the external $\overline{SS}$ pin (Pin 31/Pin 33) can be read via the SPR0 bit in the SPICON SFR.

The SFR register in Table 41 is used to control the SPI interface.

TIME INTERVAL COUNTER (TIC)

A TIC is provided on-chip for counting longer intervals than the standard 8051-compatible timers can count. The TIC is capable of timeout intervals ranging from 1/128 second to 255 hours. Also, this counter is clocked by the external 32.768 kHz crystal rather than by the core clock, and it can remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required. Note that instructions to the TIC SFRs are also clocked at 32.768 kHz, so sufficient time must be allowed in user code for these instructions to execute.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled. If the device is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 45. Note also that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by user software. In effect, this facilitates the implementation of a real-time clock. A basic block diagram of the TIC is shown in Figure 47.

Because the TIC is clocked directly from a 32 kHz external crystal on the devices, instructions that access the TIC registers are also clocked at 32 kHz (not at the core frequency). The user must ensure that sufficient time is given for these instructions to execute.

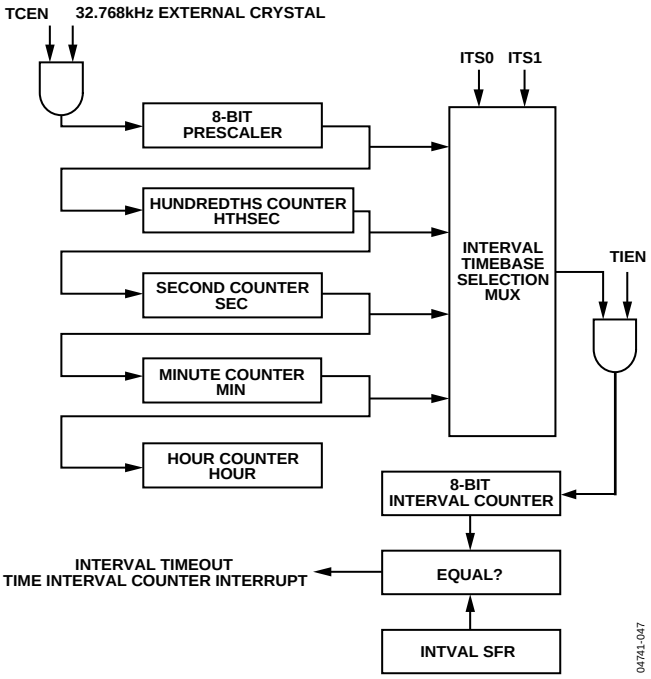

Figure 47. TIC Simplified Block Diagram

UART SERIAL INTERFACE

The serial port is full duplex, meaning that it can transmit and receive simultaneously. It is also receive buffered, meaning that it can begin receiving a second byte before a previously received byte is read from the receive register. However, if the first byte is still not read by the time reception of the second byte is complete, the first byte is lost. The physical interface to the serial data network is via Pins RxD(P3.0) and TxD(P3.1), while the SFR interface to the UART comprises SBUF and SCON, as described in this section.

SBUF SFR

Both the serial port receive and transmit registers are accessed through the SBUF SFR (SFR address = 99H). Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

SCON UART—Serial Port Control Register

SFR Address: 98H
Power-On Default: 00H
Bit Addressable: Yes

Table 54. SCON SFR Bit Designations

Bit No.	Name	Description
7, 6	SM0, SM1	UART Serial Mode Select Bits. These bits select the serial port operating mode as follows:
		SM0 SM1 Selected Operating Mode.
		0 0 Mode 0: Shift register, fixed baud rate (Core_Clk/2).
		0 1 Mode 1: 8-bit UART, variable baud rate.
		1 0 Mode 2: 9-bit UART, fixed baud rate (Core_Clk/32) or (Core_Clk/16).
		1 1 Mode 3: 9-bit UART, variable baud rate.
5	SM2	Multiprocessor Communication Enable Bit.
		Enables multiprocessor communication in Modes 2 and 3.
		In Mode 0, SM2 should be cleared.
		In Mode 1, if SM2 is set, RI is not activated if a valid stop bit was not received. If SM2 is cleared, RI is set as soon as the byte of data is received.
		In Modes 2 or 3, if SM2 is set, RI is not activated if the received ninth data bit in RB8 is 0.
		If SM2 is cleared, RI is set as soon as the byte of data is received.
4	REN	Serial Port Receive Enable Bit.
		Set by user software to enable serial port reception.
3	TB8	Serial Port Transmit (Bit 9).
		The data loaded into TB8 is the ninth data bit transmitted in Modes 2 and 3. Cleared by user software to disable serial port reception.
2	RB8	Serial Port Receiver Bit 9.
		The ninth data bit received in Modes 2 and 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.
1	TI	Serial Port Transmit Interrupt Flag.
		Set by hardware at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in Modes 1, 2, and 3. TI must be cleared by user software.
0	RI	Serial Port Receive Interrupt Flag.
		Set by hardware at the end of the eighth bit in Mode 0, or halfway through the stop bit in Modes 1, 2, and 3. RI must be cleared by software.

SBUF—UART Serial Port Data Register

SFR Address: 99H
Power-On Default: 00H
Bit Addressable: No

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART Serial Port Baud Rate Generation

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(\frac{CoreClockFrequency}{12}\right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Core\ Clock\ Frequency$$

Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or in both (one for transmit and the other for receive).

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{CoreClockFrequency}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{1}{16} \times Timer\ 2\ Overflow\ Rate$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 60.

In this case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{Core\ \ Clock\ \ Frequency}{(16 \times [65536\ - (RCAP\ 2H\ :RCAP\ 2L)])}$$

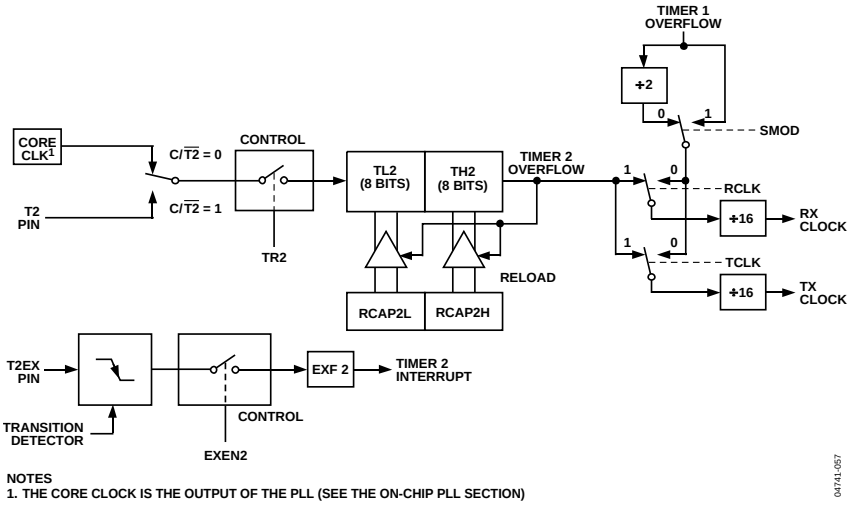

Figure 60. Timer 2, UART Baud Rates

Table 55. T3CON SFR Bit Designations

Bit No.	Name	Description			
7	T3BAUDEN	T3UARTBAUD Enable.			
		Set to enable Timer 3 to generate the baud rate. When set, PCON.7, T2CON.4, and T2CON.5 are ignored. Cleared to let the baud rate be generated as per a standard 8052.			
6		Not Implemented. Write Don't Care.			
5		Not Implemented. Write Don't Care.			
4		Not Implemented. Write Don't Care.			
3		Not Implemented. Write Don't Care.			
2, 1, 0	DIV2, DIV1, DIV0	Binary Divider			
		DIV2	DIV1	DIV0	
		0	0	0	Binary Divider 0. See Table 57.
		0	0	1	Binary Divider 1. See Table 57.
		0	1	0	Binary Divider 2. See Table 57.
		0	1	1	Binary Divider 3. See Table 57.
		1	0	0	Binary Divider 4. See Table 57.
		1	0	1	Binary Divider 5. See Table 57.
		1	1	0	Binary Divider 6. See Table 57.

T3FD—Timer 3 Fractional Divider Register

See Table 57 for values.

SFR Address: 9DH
Power-On Default: 00H
Bit Addressable: No

Table 56. T3FD SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	----	Not Implemented. Write Don't Care.
5	T3FD.5	Timer 3 Fractional Divider Bit 5.
4	T3FD.4	Timer 3 Fractional Divider Bit 4.
3	T3FD.3	Timer 3 Fractional Divider Bit 3.
2	T3FD.2	Timer 3 Fractional Divider Bit 2.
1	T3FD.1	Timer 3 Fractional Divider Bit 1.
0	T3FD.0	Timer 3 Fractional Divider Bit 0.

IEIP2—Secondary Interrupt Enable Register

SFR Address: A9H
Power-On Default: A0H
Bit Addressable: No

Table 60. IEIP2 Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	PTI	Time Interval Counter Interrupt Priority Setting (1 = High, 0 = Low).
5	PPSM	Power Supply Monitor Interrupt Priority Setting (1 = High, 0 = Low).
4	PSI	SPI/I²C Interrupt Priority Setting (1 = High, 0 = Low).
3	----	This bit must contain 0.
2	ETI	Set by the user to enable the time interval counter interrupt. Cleared by the user to disable the time interval counter interrupt.
1	EPSMI	Set by the user to enable the power supply monitor interrupt. Cleared by the user to disable the power supply monitor interrupt.
0	ESI	Set by the user to enable the SPI/I²C serial port interrupt. Cleared by the user to disable the SPI/I²C serial port interrupt.

INTERRUPT PRIORITY

The interrupt enable registers are written by the user to enable individual interrupt sources; the interrupt priority registers allow the user to select one of two priority levels for each interrupt. A high priority interrupt can interrupt the service routine of a low priority interrupt, and if two interrupts of different priorities occur at the same time, the higher level interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, the polling sequence, as shown in Table 61, is observed.

Table 61. Priority within Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt
WDS	2	Watchdog Timer Interrupt
IE0	2	External Interrupt 0
RDY0/RDY1	3	ADC Interrupt
TF0	4	Timer/Counter 0 Interrupt
IE1	5	External Interrupt 1
TF1	6	Timer/Counter 1 Interrupt
ISPI/I2CI	7	SPI/I²C Interrupt
RI/TI	8	UART Serial Port Interrupt
TF2/EXF2	9	Timer/Counter 2 Interrupt
TII	11 (Lowest)	Timer Interval Counter Interrupt

INTERRUPT VECTORS

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table 62.

Table 62. Interrupt Vector Addresses

Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH
RDY0/RDY1 (ADuC845 only)	0033H
ISPI/I2CI	003BH
PSMI	0043H
TII	0053H
WDS	005BH

Single-Pin Emulation Mode

Built into the ADuC845/ADuC847/ADuC848 is a dedicated controller for single-pin in-circuit emulation (ICE). In this mode, emulation access is gained by connection to a single pin, the $\overline{EA}$ pin. Normally on the 8051 standard, this pin is hardwired either high or low to select execution from internal or external program memory space. Note that external program memory or execution from external program memory is not allowed on the devices. To enable single-pin emulation mode, users need to pull the $\overline{EA}$ pin high through a 1 kΩ resistor as shown in Figure 70. The emulator then connects to the 2-pin header also shown in Figure 70. To be compatible with the standard connector that comes with the single-pin emulator available from Accutron Limited (www.accutron.com), use a 2-pin 0.1-inch pitch Friction Lock header from Molex (www.molex.com) such as part number 22-27-2021. Be sure to observe the polarity of this header. As shown in Figure 70, when the Friction Lock tab is at the right, the ground pin should be the lower of the two pins when viewed from the top.

Typical System Configuration

A typical ADuC845/ADuC847/ADuC848 configuration is shown in Figure 70. Figure 70 also includes connections for a typical analog measurement application of the devices, namely an interface to a resistive temperature device (RTD). The arrangement shown is commonly referred to as a 4-wire RTD configuration.

Here, the on-chip excitation current sources are enabled to excite the sensor. The excitation current flows directly through the RTD generating a voltage across the RTD proportional to its resistance. This differential voltage is routed directly to one set of the positive and negative inputs of the ADC (AIN1, AIN2, respectively in this case). The same current that excited the RTD also flows through a series resistance, R_{REF}, generating a ratiometric voltage reference, V_{REF}. The ratiometric voltage reference ensures that variations in the excitation current do not affect the measurement system since the input voltage from the RTD and reference voltage across R_{REF} vary ratiometrically with the excitation current. Resistor R_{REF} must, however, have a low temperature coefficient to avoid errors in the reference voltage overtemperature. R_{REF} must also be large enough to generate at least a 1 V voltage reference.

The preceding example shows just a single differential ADC connection using a single reference input pair. The ADuC845/ADuC847/ADuC848 have the capability of connecting to five differential inputs directly or ten single-ended inputs (LFCSP package only) as well as having a second reference input. This arrangement means that different sensors with different reference ranges can be connected to the device with the need for external multiplexing circuitry. This arrangement is shown in Figure 71. The bridge sensor shown can be a load cell or a pressure sensor. The RTD is shown using a reference voltage derived from the R_{REF} resistor via the REFIN± inputs, and the bridge sensor is shown using a divided down AV_{DD} reference via the REFIN2± inputs.

Table 66. EXTERNAL DATA MEMORY WRITE CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{WLWH}	$\overline{WR}$ Pulse Width	65		130		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	65		135		ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low		130		260	ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	60		120		ns
t_{QVWH}	Data Setup Before $\overline{WR}$	120		250		ns
t_{WHQX}	Data and Address Hold After $\overline{WR}$	380		755		ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		125		ns

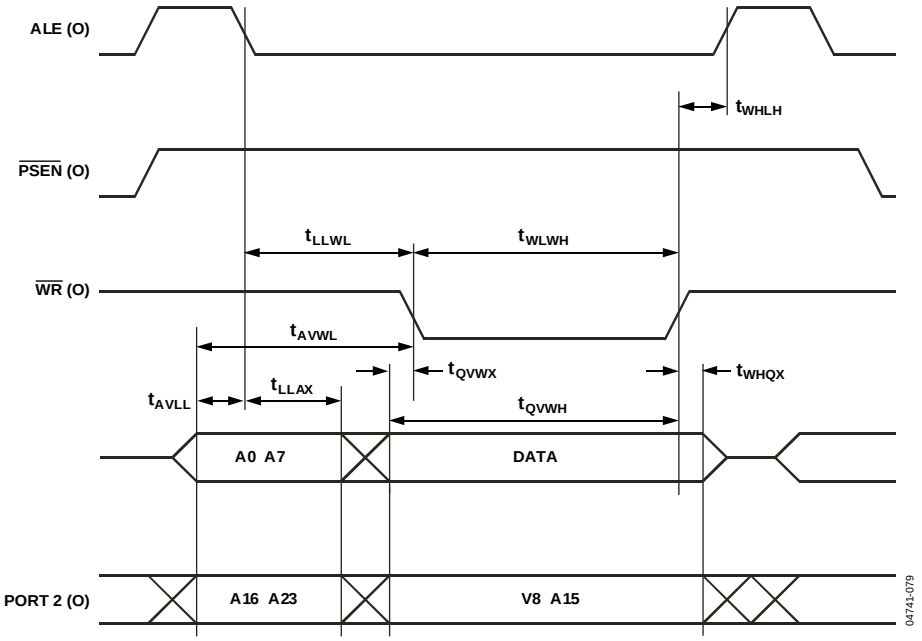

Figure 74. External Data Memory Write Cycle

Table 67. I²C-COMPATIBLE INTERFACE TIMING Parameter

Parameter		Min	Max	Unit
t_L	SCLCK Low Pulse Width	1.3		µs
t_H	SCLCK High Pulse Width	0.6		µs
t_{SHD}	Start Condition Hold Time	0.6		µs
t_{DSU}	Data Setup Time	100		µs
t_{DHD}	Data Hold Time		0.9	µs
t_{RSU}	Setup Time for Repeated Start	0.6		µs
t_{PSU}	Stop Condition Setup Time	0.6		µs
t_{BUF}	Bus Free Time Between a Stop Condition and a Start Condition	1.3		µs
t_R	Rise Time of Both SCLCK and SDATA		300	ns
t_F	Fall Time of Both SCLCK and SDATA		300	ns
t_{SUP}[1]	Pulse Width of Spike Suppressed		50	ns

[1] Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

Table 69. SPI MASTER MODE TIMING (CPHA = 0) Parameter

		Min	Typ	Max	Unit
t_{SL}	SCLOCK Low Pulse Width[1]		635		ns
t_{SH}	SCLOCK High Pulse Width[1]		635		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DOSU}	Data Output Setup Before SCLOCK Edge			150	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns

[1] Characterized under the following conditions:
a. Core clock divider bits CD2, CD1, and CD0 in PLLCON SFR set to 0, 1, and 1, respectively, that is, core clock frequency = 1.57 MHz.
b. SPI bit-rate selection bits SPR1 and SPR0 in SPICON SFR set to 0 and 0, respectively.

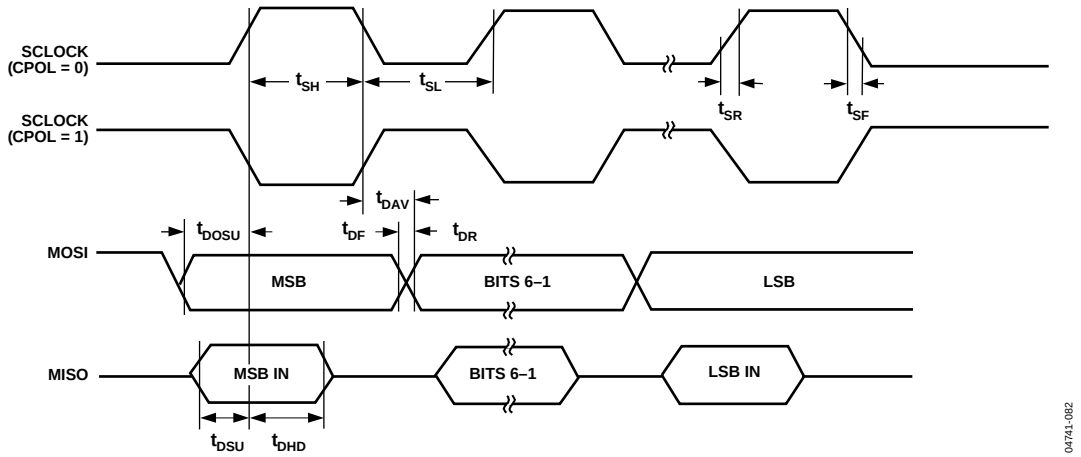

Figure 77. SPI Master Mode Timing (CHPA = 0)

NOTES