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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	62KB (62K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x16b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc848bsz62-3

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

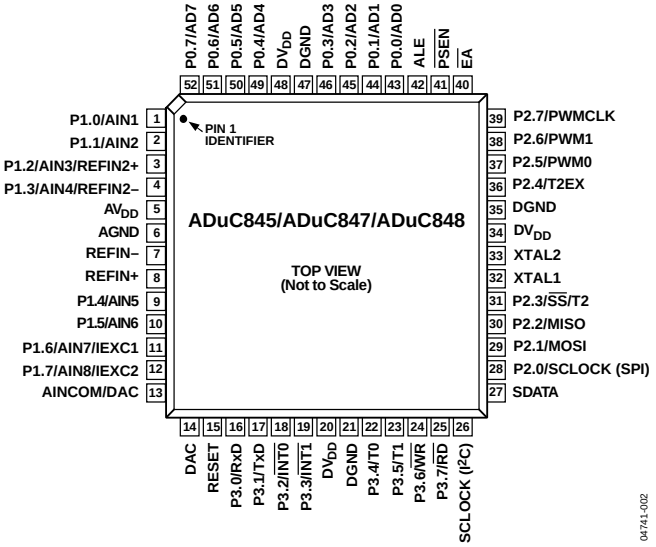

Figure 2. 52-Lead MQFP Pin Configuration

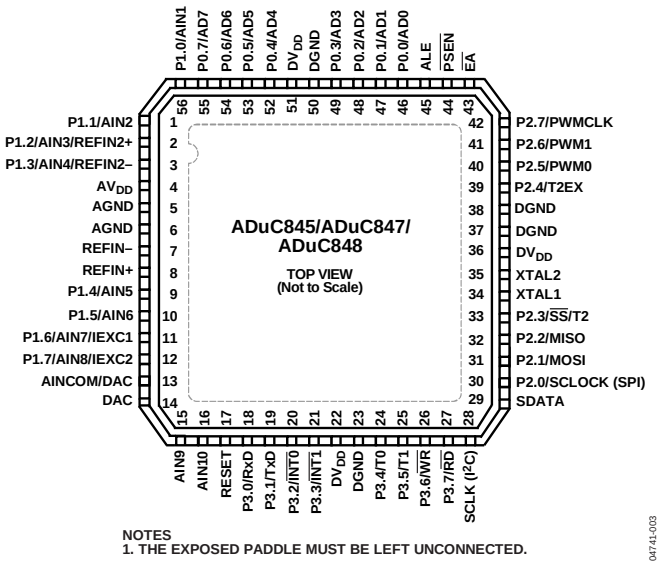

Figure 3. 56-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.				
52-MQFP	**56-LFCSP**	**Mnemonic**	**Type[1]**	**Description**
1	56	P1.0/AIN1	I	By power-on default, P1.0/AIN1 is configured as the AIN1 analog input. AIN1 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN2. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
2	1	P1.1/AIN2	I	On power-on default, P1.1/AIN2 is configured as the AIN2 analog input. AIN2 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN1. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
3	2	P1.2/AIN3/REFIN2+	I	On power-on default, P1.2/AIN3 is configured as the AIN3 analog input. AIN3 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN4. P1.2 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, positive terminal.
4	3	P1.3/AIN4/REFIN2–	I	On power-on default, P1.3/AIN4 is configured as the AIN4 analog input. AIN4 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN3. P1.3 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, negative terminal.
5	4	AV_{DD}	S	Analog Supply Voltage.
6	5	AGND	S	Analog Ground.
Not applicable	6	AGND	S	A second analog ground is provided with the LFCSP version only.
7	7	REFIN–	I	External Differential Reference Input, Negative Terminal.
8	8	REFIN+	I	External Differential Reference Input, Positive Terminal.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
9	9	P1.4/AIN5	I	On power-on default, P1.4/AIN5 is configured as the AIN5 analog input. AIN5 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN6. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
10	10	P1.5/AIN6	I	On power-on default, P1.5/AIN6 is configured as the AIN6 analog input. AIN6 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN5. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
11	11	P1.6/AIN7/IEXC1	I/O	On power-on default, P1.6/AIN7 is configured as the AIN7 analog input. AIN7 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN8. One or both current sources can also be configured at this pin. P1.6 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
12	12	P1.7/AIN8/IEXC2	I/O	On power-on default, P1.7/AIN8 is configured as the AIN8 analog input. AIN8 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN7. One or both current sources can also be configured at this pin. P1.7 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
13	13	AINCOM/DAC	I/O	All analog inputs can be referred to this pin, provided that a relevant pseudo differential input mode is selected. This pin also functions as an alternative pin out for the DAC.
14	14	DAC	O	The voltage output from the DAC, if enabled, appears at this pin.
Not applicable	15	AIN9	I	AIN9 can be used as a pseudo differential analog input when used with AINCOM or as the positive input of a fully differential pair when used with AIN10 (LFCSP version only).
Not applicable	16	AIN10	I	AIN10 can be used as a pseudo differential analog input when used with AINCOM or as the negative input of a fully differential pair when used with AIN9 (LFCSP version only).
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. This pin has an internal weak pull-down and a Schmitt trigger input stage.
16 to 19, 22 to 25	18 to 21, 24 to 27	P3.0 to P3.7	I/O	P3.0 to P3.7 are bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active for one core clock period of the instruction cycle. Port 3 pins also have the various secondary functions described in this table.
16	18	P3.0/RxD		Receiver Data for UART Serial Port.
17	19	P3.1/TxD		Transmitter Data for UART Serial Port.
18	20	P3.2/$\overline{\text{INT0}}$		External Interrupt 0. This pin can also be used as a gate control input to Timer 0.
19	21	P3.3/$\overline{\text{INT1}}$		External Interrupt 1. This pin can also be used as a gate control input to Timer 1.
22	24	P3.4/T0		Timer/Counter 0 External Input.
23	25	P3.5/T1		Timer/Counter 1 External Input.
24	26	P3.6/$\overline{\text{WR}}$		External Data Memory Write Strobe. This pin latches the data byte from Port 0 into an external data memory.
25	27	P3.7/$\overline{\text{RD}}$		External Data Memory Read Strobe. This pin enables the data from an external data memory to Port 0.

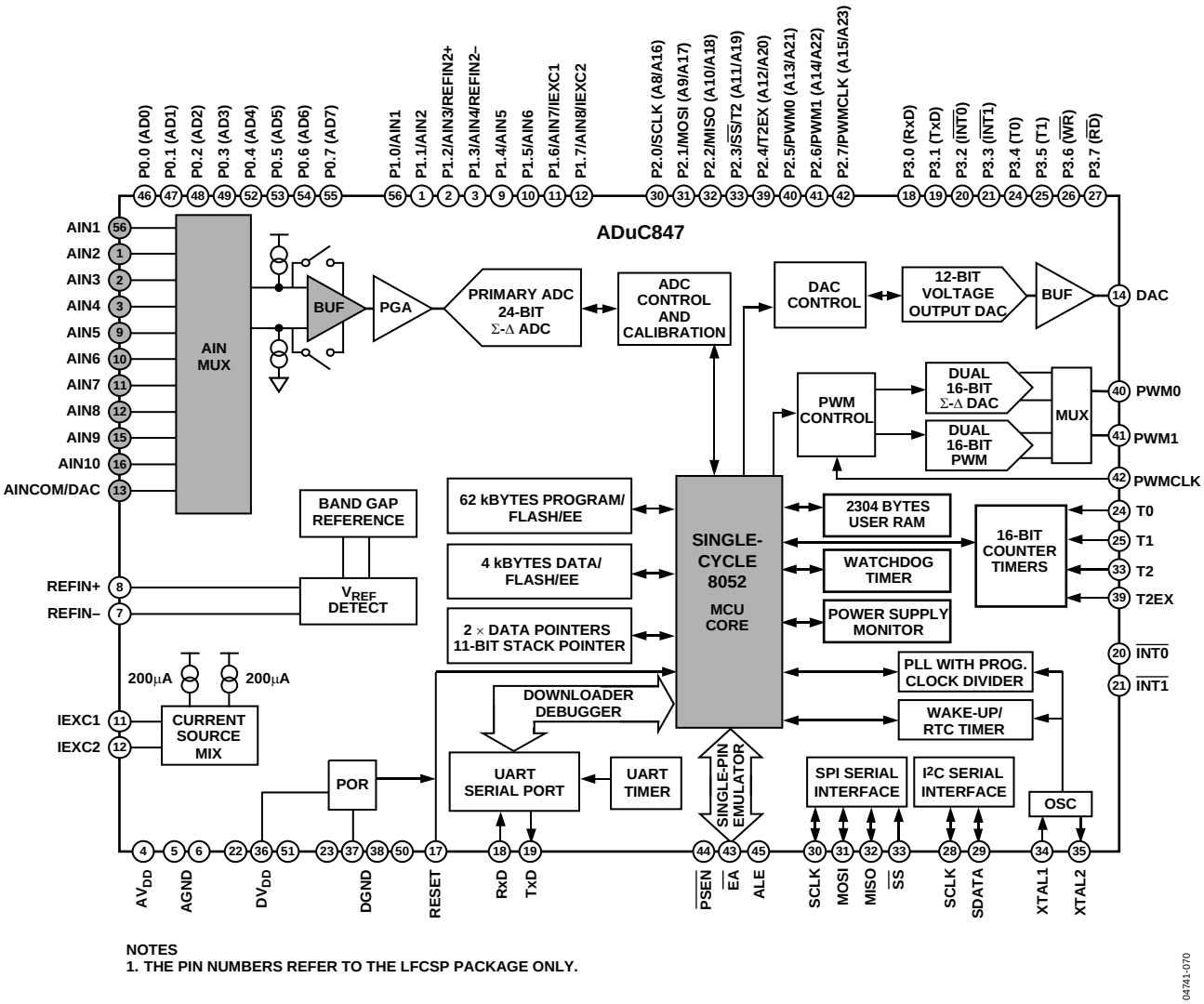

Figure 5. Detailed Block Diagram of the ADuC847

Mnemonic	Description	Bytes	Cycles[1]
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2
MOV dir,A	Move A to direct byte	2	2
MOV Rn, dir	Move register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,@Ri	Move indirect to direct memory	2	2
MOV @Ri,dir	Move direct to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A	1	4
MOVX[2] A,@Ri	Move external (A8) data to A	1	4
MOVX[2] A,@DPTR	Move external (A16) data to A	1	4
MOVX[2] @Ri,A	Move A to external data (A8)	1	4
MOVX[2] @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit	OR direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3

Power Control Register (PCON)

The PCON SFR contains bits for power-saving options and general-purpose status flags as listed in Table 6.

SFR Address: 87H
Power-On Default: 00H
Bit Addressable: No

Table 6. PCON SFR Bit Designations

Bit No.	Name	Description
7	SMOD	Double UART Baud Rate. 0 = Normal, 1 = Double Baud Rate.
6	SERIPD	Serial Power-Down Interrupt Enable. If this bit is set, a serial interrupt from either SPI or I^2C can terminate the power-down mode.
5	INT0PD	INT0 Power-Down Interrupt Enable. If this bit is set, either a level ($\overline{IT0}$ = 0) or a negative-going transition ($\overline{IT0}$ = 1) on the INT0 pin terminates power-down mode.
4	ALEOFF	If set to 1, the ALE output is disabled.
3	GF1	General-Purpose Flag Bit.
2	GF0	General-Purpose Flag Bit.
1	PD	Power-Down Mode Enable. If set to 1, the device enters power-down mode.
0	-----	Not Implemented. Write Don't Care.

ADuC845/ADuC847/ADuC848 Configuration Register (CFG845/CFG847/CFG848)

The CFG845/CFG847/CFG848 SFR contains the bits necessary to configure the internal XRAM and the extended SP. By default, it configures the user into 8051 mode, that is, extended SP, and the internal XRAM are disabled. When using in a program, use the device name only, that is, CFG845, CFG847, or CFG848.

SFR Address: AFH
Power-On Default: 00H
Bit Addressable: No

Table 7. CFG845/CFG847/CFG848 SFR Bit Designations

Bit No.	Name	Description
7	EXSP	Extended SP Enable. If this bit is set to 1, the stack rolls over from SPH/SP = 00FFH to 0100H. If this bit is cleared to 0, SPH SFR is disabled and the stack rolls over from SP = FFH to SP = 00H.
6	----	Not Implemented. Write Don't Care.
5	----	Not Implemented. Write Don't Care.
4	----	Not Implemented. Write Don't Care.
3	----	Not Implemented. Write Don't Care.
2	----	Not Implemented. Write Don't Care.
1	----	Not Implemented. Write Don't Care.
0	XRAMEN	If this bit is set to 1, the internal XRAM is mapped into the lower 2 kbytes of the external address space. If this bit is cleared to 0, the internal XRAM is accessible and up to 16 MB of external data memory become available. See Figure 8.

AUXILIARY ADC (ADUC845 ONLY)

Table 18. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Enabled

SF Word	Data Update Rate (Hz)	μV
13	105.03	17.46
23	59.36	3.13
27	50.56	4.56
69	19.79	2.66
255	5.35	1.13

Table 19. ADuC845 Typical Peak-to-Peak Resolution (Bits) vs. Update Rate[1] with Chop Enabled

SF Word	Data Update Rate (Hz)	Bits
13	105.03	15.5
23	59.36	18
27	50.56	17.5
69	19.79	18
255	5.35	19.5

[1] ADC converting in bipolar mode.

Table 20. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	μV
3	1365.33	1386.58
13	315.08	34.94
66	62.06	3.2
69	59.36	3.19
81	50.57	3.14
255	16.06	1.71

Table 21. ADuC845 Peak-to-Peak Resolution (Bits) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Bits
3	1365.33	9
13	315.08	14.5
66	62.06	18
69	59.36	18
81	50.57	18
255	16.06	19

REFERENCE INPUTS

The ADuC845/ADuC847/ADuC848 each have two separate differential reference inputs, REFIN± and REFIN2±. While both references are available for use with the primary ADC, only REFIN± is available for the auxiliary ADC (ADuC845 only). The common-mode range for these differential references is from AGND to AV_{DD}. The nominal external reference voltage is 2.5 V, with the primary and auxiliary (ADuC845 only) reference select bits configured from the ADC0CON2 and ADC1CON (ADuC845 only), respectively.

When an external reference voltage is used, the primary ADC sees this internally as a 2.56 V reference ($V_{REF} \times 1.024$). Therefore, any calculations of LSB size should account for this. For instance, with a 2.5 V external reference connected and using a gain of 1 on a unipolar range (2.56 V), the LSB size is $(2.56/2^{24}) = 152.6$ nV (if using the 24-bit ADC on the ADuC845 or ADuC847). If a bipolar gain of 4 is used (±640 mV), the LSB size is $(±640 \text{ mV})/2^{24}) = 76.3$ nV (again using the 24-bit ADC on the ADuC845 or ADuC847).

The ADuC845/ADuC847/ADuC848 can also be configured to use the on-chip band gap reference via the XREF0/1 bits in the ADC0CON2 SFR (for primary ADC) or the AXREF bit in ADC1CON (for auxiliary ADC (ADuC845 only)). In this mode of operation, the ADC sees the internal reference of 1.25 V, thereby halving all the input ranges. A consequence of using the internal band gap reference is a noticeable degradation in peak-to-peak resolution. For this reason, operation with an external reference is recommended.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference inputs for the device, the effect of any low frequency noise in the excitation source is removed because the application is ratiometric. If the devices are not used in a ratiometric configuration, use a low noise reference. Recommended reference voltage sources for the ADuC845/ADuC847/ADuC848 include the ADR421, REF43, and REF192.

The reference inputs provide a high impedance, dynamic load to external connections. Because the impedance of each reference input is dynamic, resistor/capacitor combinations on these pins can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources, such as those mentioned above, for example, the ADR421, typically have low output impedances, and, therefore, decoupling capacitors on the REFIN± or REFIN2± inputs would be recommended (typically 0.1 μF). Deriving the reference voltage from an external resistor configuration means that the reference input sees a significant external source impedance. External decoupling of the REFIN± and/or REFIN2± inputs is not recommended in this type of configuration.

BURNOUT CURRENT SOURCES

The primary ADC on the ADuC845 and the ADC on the ADuC847 and ADuC848 incorporate two 100 nA constant current generators that are used to detect a failure in a connected sensor. One sources current from the AV_{DD} to AIN(+), and one sinks current from AIN(−) to AGND. These currents are only configurable for use on AIN5/AIN6 and/or AIN7/AIN8 in differential mode only, from the ICON.6 bit in the ICON SFR

USING FLASH/EE DATA MEMORY

The 4 kbytes of Flash/EE data memory are configured as 1024 pages, each of 4 bytes. As with the other ADuC845/ADuC847/ADuC848 peripherals, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) holds the 4 bytes of data at each page. The page is addressed via the EADRH and EADRL registers. Finally, ECON is an 8-bit control register that can be written to with one of nine Flash/EE memory access commands to trigger various read, write, erase, and verify functions. A block diagram of the SFR interface to the Flash/EE data memory array is shown in Figure 32.

ECON—Flash/EE Memory Control SFR

Programming either Flash/EE data memory or Flash/EE program memory is done through the Flash/EE memory control SFR (ECON). This SFR allows the user to read, write, erase, or verify the 4 kbytes of Flash/EE data memory or the 56 kbytes of Flash/EE program memory.

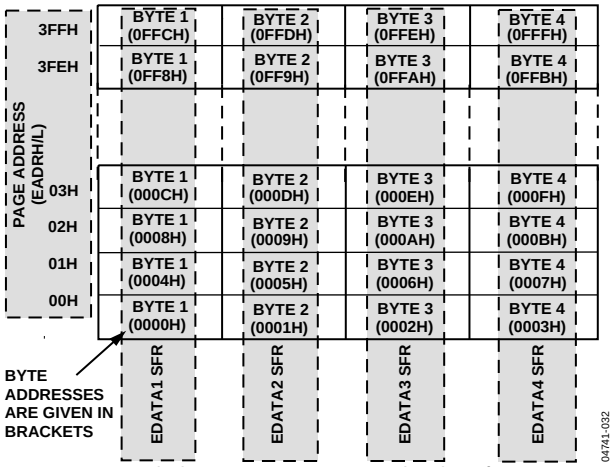

Figure 32. Flash/EE Data Memory Control and Configuration

Table 32. ECON—Flash/EE Memory Commands

ECON Value	Command Description (Normal Mode, Power-On Default)	Command Description (ULOAD Mode)
01H Read	4 bytes in the Flash/EE data memory, addressed by the page address EADRH/L, are read into EDATA1–4.	Not implemented. Use the MOVC instruction.
02H Write	Results in 4 bytes in EDATA1–4 being written to the Flash/EE data memory, at the page address given by EADRH (0 ≤ EADRH < 0400H). Note that the 4 bytes in the page being addressed must be pre-erased.	Bytes 0 to 255 of internal XRAM are written to the 256 bytes of Flash/EE program memory at the page address given by EADRH/L (0 ≤ EADRH/L < E0H). Note that the 256 bytes in the page being addressed must be pre-erased.
03H	Reserved.	Reserved.
04H Verify	Verifies that the data in EDATA1–4 is contained in the page address given by EADRH/L. A subsequent read of the ECON SFR results in a 0 being read if the verification is valid, or a nonzero value being read to indicate an invalid verification.	Not implemented. Use the MOVC and MOVX instructions to verify the Write in software.
05H Erase Page	4-byte page of Flash/EE data memory address is erased by the page address EADRH/L.	64-byte page of FLASH/EE program memory addressed by the byte address EADRH/L is erased. A new page starts when EADRL is equal to 00H, 80H, or C0H.
06H Erase All	4 kbytes of Flash/EE data memory are erased.	The entire 56 kbytes of ULOAD are erased.
81H ReadByte	The byte in the Flash/EE data memory, addressed by the byte address EADRH/L, is read into EDATA1 (0 ≤ EADRH/L ≤ 0FFFH).	Not implemented. Use the MOVC command.
82H WriteByte	The byte in EDATA1 is written into Flash/EE data memory at the byte address EADRH/L.	The byte in EDATA1 is written into Flash/EE program memory at the byte address EADRH/L (0 ≤ EADRH/L ≤ DFFFH).
0FH EXULOAD	Configures the ECON instructions (above) to operate on Flash/EE data memory.	Enters normal mode, directing subsequent ECON instructions to operate on the Flash/EE data memory.
F0H ULOAD	Enters ULOAD mode; subsequent ECON instructions operate on Flash/EE program memory.	Enables the ECON instructions to operate on the Flash/EE program memory. ULOAD entry mode.

DAC CIRCUIT INFORMATION

The ADuC845/ADuC847/ADuC848 incorporate a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF, and has two selectable ranges, 0 V to V_{REF} and 0 V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register, DACCON, and two data registers, DACH/L. The DAC output can be programmed to appear at Pin 14 (DAC) or Pin 13 (AINCOM).

In 12-bit mode, the DAC voltage output is updated as soon as the DACL data SFR is written; therefore, the DAC data registers should be updated as DACH first, followed by DACL. The 12-bit DAC data should be written into DACH/L right-justified such that DACL contains the lower 8 bits, and the lower nibble of DACH contains the upper 4 bits.

DACCON Control Register

SFR Address: FDH
Power-On Default: 00H
Bit Addressable: No

Table 33. DACCON—DAC Configuration Commands

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	–––	Not Implemented. Write Don't Care.
5	–––	Not Implemented. Write Don't Care.
4	DACPIN	DAC Output Pin Select. Set to 1 by the user to direct the DAC output to Pin 13 (AINCOM). Cleared to 0 by the user to direct the DAC output to Pin 14 (DAC).
3	DAC8	DAC 8-Bit Mode Bit. Set to 1 by the user to enable 8-bit DAC operation. In this mode, the 8 bits in DACL SFR are routed to the 8 MSBs of the DAC, and the 4 LSBs of the DAC are set to 0. Cleared to 0 by the user to enable 12-bit DAC operation. In this mode, the 8 LSBs of the result are routed to DACL, and the upper 4 MSB bits are routed to the lower 4 bits of DACH.
2	DACRN	DAC Output Range Bit. Set to 1 by the user to configure the DAC range of 0 V to AV_{DD}. Cleared to 0 by the user to configure the DAC range of 0 V to 2.5 V (V_{REF}).
1	DACCLR	DAC Clear Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to reset the DAC data registers DACL/H to 0.
0	DACEN	DAC Enable Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to power down the DAC.

DACH/DACL Data Registers

These DAC data registers are written to by the user to update the DAC output.

SFR Address: DACL (DAC data low byte)—FBH
DACH (DAC data high byte)—FCH
Power-On Default: 00H (both registers)
Bit Addressable: No (both registers)

Using the DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier, the functional equivalent of which is shown in Figure 33.

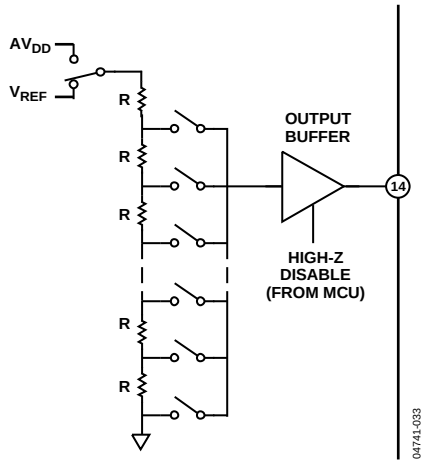

Figure 33. Resistor String DAC Functional Equivalent

Features of this architecture include inherent guaranteed monotonicity and excellent differential linearity. As shown in Figure 33, the reference source for the DAC is user-selectable in software. It can be either AV_{DD} or V_{REF}. In 0 V-to-AV_{DD} mode, the DAC output transfer function spans from 0 V to the voltage at the AV_{DD} pin. In 0 V-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal V_{REF} (2.5 V). The DAC output buffer amplifier features a true rail-to-rail output stage implementation. This means that, unloaded, each output is capable of swinging to within less than 100 mV of both AV_{DD} and ground. Moreover, the DAC's linearity specification (when driving a 10 kΩ resistive load to ground) is guaranteed through the full transfer function except Codes 0 to 48 in 0 V-to-V_{REF} mode; Codes 0 to 100; and Codes 3950 to 4095 in 0 V-to-V_{DD} mode.

Linearity degradation near ground and V_{DD} is caused by saturation of the output amplifier; a general representation of its effects (neglecting offset and gain error) is shown in Figure 34. The dotted line indicates the ideal transfer function, and the solid line represents what the transfer function might look like with endpoint nonlinearities due to saturation of the output amplifier.

Note that Figure 34 represents a transfer function in 0-to-V_{DD} mode only. In 0 V-to-V_{REF} mode (with $V_{REF} < V_{DD}$), the lower nonlinearity would be similar, but the upper portion of the transfer function would follow the ideal line to the end, showing no signs of the high-end endpoint linearity error.

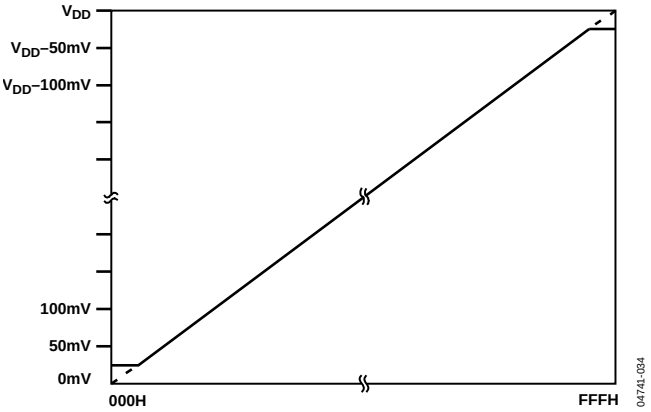

Figure 34. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities shown in Figure 34 become worse as a function of output loading. Most data sheet specifications assume a 10 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom, respectively, of Figure 34 become larger. With larger current demands, this can significantly limit output voltage swing. Figure 35 and Figure 36 illustrate this behavior. Note that the upper trace in each of these figures is valid only for an output range selection of 0 V to AV_{DD}. In 0 V-to-V_{REF} mode, DAC loading does not cause high-side voltage nonlinearities while the reference voltage remains below the upper trace in the corresponding figure. For example, if AV_{DD} = 3 V and V_{REF} = 2.5 V, the high-side voltage is not affected by loads of less than 5 mA. But around 7 mA, the upper curve in Figure 36 drops below 2.5 V (V_{REF}), indicating that at these higher currents, the output is not capable of reaching V_{REF}.

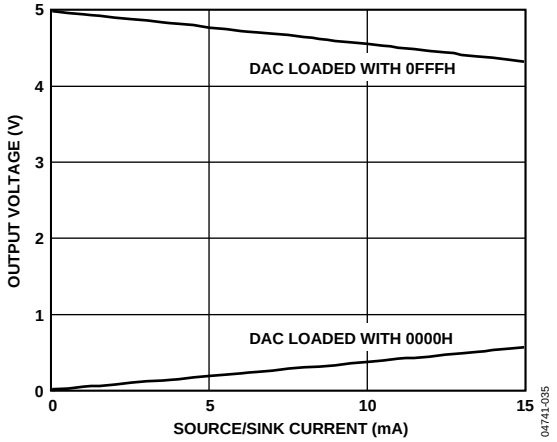

Figure 35. Source and Sink Current Capability with $V_{REF} = AV_{DD} = 5$ V

PWMCON PWM Control SFR

SFR Address: AEH
Power-On Default: 00H
Bit Addressable: No

Table 34. PWMCON PWM Control SFR

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6, 5, 4	PWM2, PWM1, PWM0	PMW Mode Selection. PWM2 PWM1 PWM0 0 0 0 Mode 0: PWM disabled. 0 0 1 Mode 1: Single 16-bit output with programmable pulse and cycle time. 0 1 0 Mode 2: Twin 8-bit outputs. 0 1 1 Mode 3: Twin 16-bit outputs. 1 0 0 Mode 4: Dual 16-bit pulse density outputs. 1 0 1 Mode 5: Dual 8-bit outputs. 1 1 0 Mode 6: Dual 16-bit pulse density RZ outputs. 1 1 1 Mode 7: PWM counter reset with outputs not used.
3, 2	PWS1, PWS0	PWM Clock Source Divider. PWS1 PWS0 0 0 Selected clock. 0 1 Selected clock divided by 4. 1 0 Selected clock divided by 16. 1 1 Selected clock divided by 64.
1, 0	PWC1, PWC0	PWM Clock Source Selection. PWC1 PWC0 0 0 F_{XTAL}/15 (2.184 kHz). 0 1 F_{XTAL} (32.768 kHz). 1 0 External input on P2.7. 1 1 F_{VCO} (12.58 MHz).

PWM Pulse Width High Byte (PWM0H)

SFR Address: B2H
Power-On Default: 00H
Bit Addressable: No

Table 35. PWM0H: PWM Pulse Width High Byte

PWM0H.7	PWM0H.6	PWM0H.5	PWM0H.4	PWM0H.3	PWM0H.2	PWM0H.1	PWM0H.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PWM Pulse Width Low Byte (PWM0L)

SFR Address: B1H
Power-On Default: 00H
Bit Addressable: No

The outputs of the PWM at P2.5 and P2.6 are shown in Figure 40. As can be seen, the output of PWM0 (P2.5) goes low when the PWM counter equals PWM0L. The output of PWM1 (P2.6) goes high when the PWM counter equals PWM1H and goes low again when the PWM counter equals PWM0H. Setting PWM1H to 0 ensures that both PWM outputs start simultaneously.

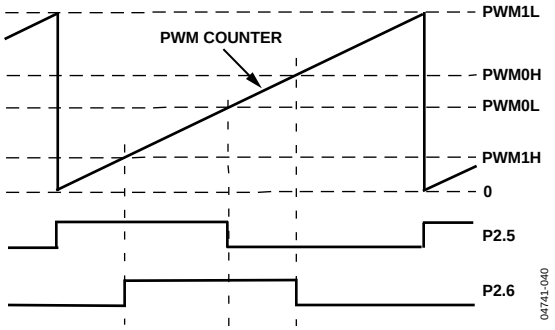

Figure 40. PWM Mode 2

Mode 3 (Twin 16-Bit PWM)

In Mode 3, the PWM counter is fixed to count from 0 to 65536, giving a fixed 16-bit PWM. Operating from the 12.58 MHz core clock results in a PWM output rate of 192 Hz. The duty cycle of the PWM outputs at P2.5 and P2.6 are independently programmable.

As shown in Figure 41, while the PWM counter is less than PWM0H/L, the output of PWM0 (P2.5) is high. Once the PWM counter equals PWM0H/L, PWM0 (P2.5) goes low and remains low until the PWM counter rolls over.

Similarly, while the PWM counter is less than PWM1H/L, the output of PWM1 (P2.6) is high. Once the PWM counter equals PWM1H/L, PWM1 (P2.6) goes low and remains low until the PWM counter rolls over.

In this mode, both PWM outputs are synchronized, that is, once the PWM counter rolls over to 0, both PWM0 (P2.5) and PWM1 (P2.6) go high.

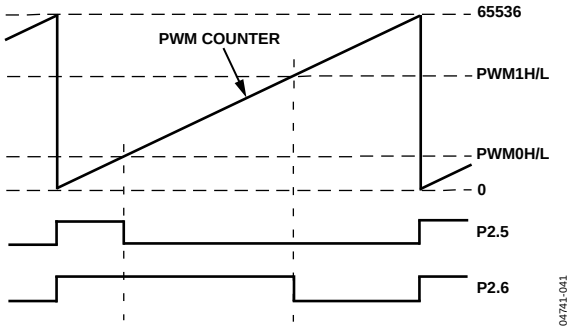

Figure 41. PWM Mode 3

Mode 4 (Dual NRZ 16-Bit Σ-Δ DAC)

Mode 4 provides a high speed PWM output similar to that of a Σ-Δ DAC. Typically, this mode is used with the PWM clock equal to 12.58 MHz.

In this mode, P2.5 and P2.6 are updated every PWM clock (80 ns in the case of 12.58 MHz). Over any 65536 cycles (16-bit PWM), PWM0 (P2.5) is high for PWM0H/L cycles and low for (65536 – PWM0H/L) cycles. Similarly, PWM1 (P2.6) is high for PWM1H/L cycles and low for (65536 – PWM1H/L) cycles.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three clocks and high for one clock (each clock is approximately 80 ns). Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale, by having a high cycle followed by only two low cycles.

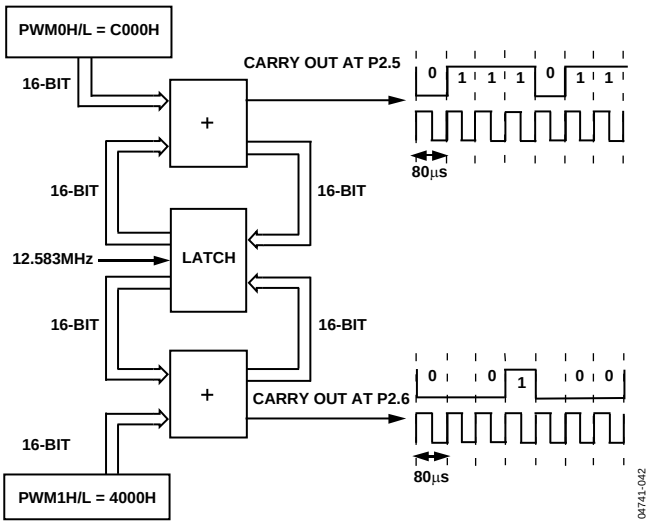

Figure 42. PWM Mode 4

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

Mode 5 (Dual 8-Bit PWM)

In Mode 5, the duty cycle and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

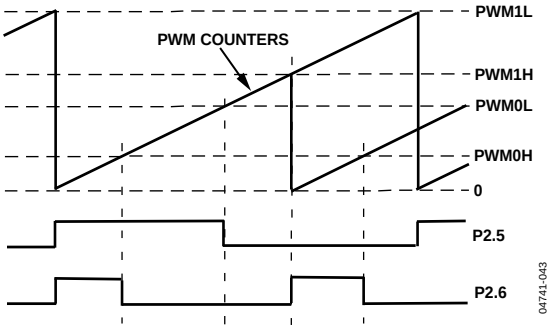

Figure 43. PWM Mode 5

Mode 6 (Dual RZ 16-Bit Σ-Δ DAC)

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4; however, the key difference is that Mode 6 provides return to zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. RZ mode ensures that any difference in the rise and fall times does not affect the Σ-Δ DAC INL. However, RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V– to AV_{DD} down to 0 V to $AV_{DD}/2$. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three full clocks (3 × 80 ns), high for one-half a clock (40 ns), and then low again for one-half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

The output resolution is set by the PWM1L and PWM1H SFRs for the P2.5 and P2.6 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P2.5 and P2.6, respectively. Both PWMs have the same clock source and clock divider.

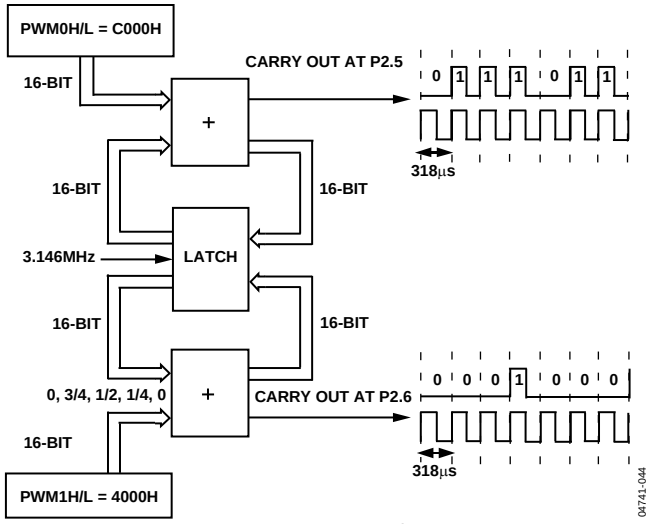

Figure 44. PWM Mode 6

Mode 7

In Mode 7, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal.

WATCHDOG TIMER

The watchdog timer generates a device reset or interrupt within a reasonable amount of time if the ADuC845/ADuC847/ADuC848 enters an erroneous state, possibly due to a programming error or electrical noise. The watchdog function can be disabled by clearing the WDE (watchdog enable) bit in the watchdog control (WDCON) SFR. When enabled, the watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the WDE bit within a predetermined amount of time (see the PRE3…0 bits in Table 44). The watchdog timer is clocked from the 32 kHz external crystal connected between the XTAL1 and XTAL2 pins. The WDCOM SFR can be written only by user software if the double write sequence described in WDWR is initiated on every write access to the WDCON SFR.

WDCON—Watchdog Control Register

SFR Address: C0H
Power-On Default: 10H
Bit Addressable: Yes

Table 44. WDCON SFR Bit Designations

Bit No.	Name	Description
7, 6, 5, 4	PRE3, PRE2, PRE1, PRE0	Watchdog Timer Prescale Bits. The watchdog timeout period is given by the equation $t_{WD} = (2^{PRE} \times (2^9/ f_{XTAL}))$ $(0 \le PRE \le 7; f_{XTAL} = 32.768\ kHz)$

PRE3	PRE2	PRE1	PRE0	Timeout Period (ms)	Action
0	0	0	0	15.6	Reset or interrupt
0	0	0	1	31.2	Reset or interrupt
0	0	1	0	62.5	Reset or interrupt
0	0	1	1	125	Reset or interrupt
0	1	0	0	250	Reset or interrupt
0	1	0	1	500	Reset or interrupt
0	1	1	0	1000	Reset or interrupt
0	1	1	1	2000	Reset or interrupt
1	0	0	0	0.0	Immediate reset
PRE3–PRE0 > 1000b					Reserved. Not a valid selection.

3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog generates an interrupt response instead of a system reset when the watchdog timeout period expires. This interrupt is not disabled by the CLR EA instruction, and it is also a fixed, high priority interrupt. If the watchdog timer is not being used to monitor the system, it can be used alternatively as a timer. The prescaler is used to set the timeout period in which an interrupt is generated.
2	WDS	Watchdog Status Bit. Set by the watchdog controller to indicate that a watchdog timeout has occurred. Cleared by writing a 0 or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit. Set by the user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog timer generates a reset or interrupt, depending on WDIR. Cleared under the following conditions: user writes 0; watchdog reset (WDIR = 0); hardware reset; PSM interrupt.

0	WDWR	Watchdog Write Enable Bit.
		Writing data to the WDCON SFR involves a double instruction sequence. Global interrupts must first be disabled. The WDWR bit is set with the very next instruction, a write to the WDCON SFR. For example:
		`CLR EA ;Disable Interrupts while configuring to WDT`
		`SETB WDWR ;Allow Write to WDCON`
		`MOV WDCON, #72H ;Enable WDT for 2.0s timeout`
		`SETB EA ;Enable Interrupts again (if required)`

TIMECON—TIC Control Register

SFR Address: A1H
Power-On Default: 00H
Bit Addressable: No

Table 45. TIMECON SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	TFH	Twenty-Four Hour Select Bit. Set by the user to enable the hour counter to count from 0 to 23. Cleared by the user to enable the hour counter to count from 0 to 255.
5, 4	ITS1, ITS0	Interval Timebase Selection Bits. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	ST1	Single Time Interval Bit. Set by the user to generate a single interval timeout. If set, a timeout clears the TIEN bit. Cleared by the user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by user software.
1	TIEN	Time Interval Enable Bit. Set by the user to enable the 8-bit time interval counter. Cleared by the user to disable the interval counter.
0	TCEN	Time Clock Enable Bit. Set by the user to enable the time clock to the time interval counters. Cleared by the user to disable the clock to the time interval counters and reset the time interval SFRs to the last value written to them by the user. The time registers (HTHSEC, SEC, MIN, and HOUR) can be written while TCEN is low.

TIMERS/COUNTERS

The ADuC845/ADuC847/ADuC848 have three 16-bit timer/counters: Timer 0, Timer 1, and Timer 2. The timer/counter hardware is included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each timer/counter consists of two 8-bit registers: THx and TLx (x = 0, 1, or 2). All three can be configured to operate either as timers or as event counters.

When functioning as a timer, the TLx register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Because a machine cycle on a single-cycle core consists of one core clock period, the maximum count rate is the core clock frequency.

When functioning as a counter, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin:

TMOD—Timer/Counter 0 and 1 Mode Register

SFR Address: 89H
Power-On Default: 00H
Bit Addressable: No

T0, T1, or T2. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. Because it takes two machine cycles (two core clock periods) to recognize a 1-to-0 transition, the maximum count rate is half the core clock frequency.

There are no restrictions on the duty cycle of the external input signal, but, to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. User configuration and control of all timer operating modes is achieved via three SFRs:

TMOD, TCON—Control and Configuration for Timers 0 and 1

T2CON—Control and Configuration for Timer 2.

Table 50. TMOD SFR Bit Designation

Bit No.	Name	Description
7	Gate	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only while the $\overline{INT1}$ pin is high and the TR1 control is set. Cleared by software to enable Timer 1 whenever the TR1control bit is set.
6	C/T	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from T1 pin). Cleared by software to select the timer operation (input from internal system clock).
5, 4	M1, M0	Timer 1 Mode Select Bits. M1 M0 Description 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH1 holds a value that is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. Cleared by software to enable Timer 0 whenever the TR0 control bit is set.
2	C/T	Timer 0 Timer or Counter Select Bit. Set by software to the select counter operation (input from T0 pin). Cleared by software to the select timer operation (input from internal system clock).
1, 0	M1, M0	Timer 0 Mode Select Bits. M1 M0 Description 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as a 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler. 1 0 8-Bit Autoreload Timer/Counter. TH0 holds a value that is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

Mode 0 (8-Bit Shift Register Mode)

Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RxD. TxD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RxD line. The 8 bits are transmitted with the least significant bit (LSB) first.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line, and the clock pulses are output from the TxD line as shown in Figure 58.

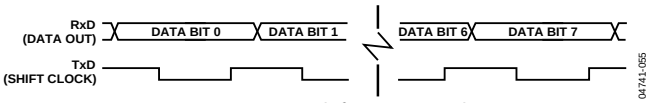

Figure 58. 8-Bit Shift Register Mode

Mode 1 (8-Bit UART, Variable Baud Rate)

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (0) and followed by a stop bit (1). Therefore, 10 bits are transmitted on TxD or are received on RxD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The write to SBUF signal also loads a 1 (stop bit) into the 9th bit position of the transmit shift register. The data is output bit-by-bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 59.

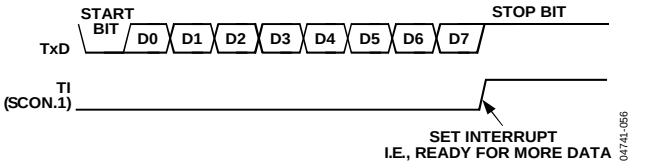

Figure 59. 8-Bit Variable Baud Rate

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming that a valid start bit is detected, character reception continues. The start bit is skipped and the 8 data bits are clocked into the serial port shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th bit (stop bit) is clocked into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is *not* met, the received frame is irretrievably lost, and RI is not set.

Mode 2 (9-Bit UART with Fixed Baud Rate)

Mode 2 is selected by setting SM0 and clearing SM1. In this mode, the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at Core_Clk/64 by default, although by setting the SMOD bit in PCON, the frequency can be doubled to Core_Clk/32. Eleven bits are transmitted or received: a start bit (0), 8 data bits, a programmable 9th bit, and a stop bit (1). The 9th bit is most often used as a parity bit, although it can be used for anything, including a ninth data bit if required.

To transmit, the 8 data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated, the 8 data bits (from SBUF) are loaded into the transmit shift register (LSB first). The contents of TB8 are loaded into the 9th bit position of the transmit shift register. The transmission starts at the next valid baud rate clock. The TI flag is set as soon as the stop bit appears on TxD.

Reception for Mode 2 is similar to that of Mode 1. The 8 data bytes are input at RxD (LSB first) and loaded onto the receive shift register. When all 8 bits have been clocked in, the following events occur:

- The 8 bits in the receive shift register are latched into SBUF.
- The 9th data bit is latched into RB8 in SCON.
- The receiver interrupt flag (RI) is set.

All of the following conditions must be met at the time the final shift pulse is generated:

- RI = 0
- Either SM2 = 0 or SM2 = 1
- Received stop bit = 1

If any of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

INTERRUPT SYSTEM

The ADuC845/ADuC847/ADuC848 provide nine interrupt sources with two priority levels. The control and configuration of the interrupt system is carried out through three interrupt-related SFRs:

IE Interrupt Enable Register
IP Interrupt Priority Register
IEIP2 Secondary Interrupt Enable Register

IE—Interrupt Enable Register

SFR Address: A8H
Power-On Default: 00H
Bit Addressable: Yes

Table 58. IE SFR Bit Designations

Bit No.	Name	Description
7	EA	Set by the user to enable all interrupt sources. Cleared by the user to disable all interrupt sources.
6	EADC	Set by the user to enable the ADC interrupt. Cleared by the user to disable the ADC interrupt.
5	ET2	Set by the user to enable the Timer 2 interrupt. Cleared by the user to disable the Timer 2 interrupt.
4	ES	Set by the user to enable the UART serial port interrupt. Cleared by the user to disable the UART serial port interrupt.
3	ET1	Set by the user to enable the Timer 1 interrupt. Cleared by the user to disable the Timer 1 interrupt.
2	EX1	Set by the user to enable External Interrupt 1 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 1 ($\overline{INT0}$).
1	ET0	Set by the user to enable the Timer 0 interrupt. Cleared by the user to disable the Timer 0 interrupt.
0	EX0	Set by the user to enable External Interrupt 0 ($\overline{INT0}$). Cleared by the user to disable External Interrupt 0 ($\overline{INT0}$).

IP—Interrupt Priority Register

SFR Address: B8H
Power-On Default: 00H
Bit Addressable: Yes

Table 59. IP SFR Bit Designations

Bit No.	Name	Description
7	-----	Not Implemented. Write Don't Care.
6	PADC	ADC Interrupt Priority (1 = High; 0 = Low).
5	PT2	Timer 2 Interrupt Priority (1 = High; 0 = Low).
4	PS	UART Serial Port Interrupt Priority (1 = High; 0 = Low).
3	PT1	Timer 1 Interrupt Priority (1 = High; 0 = Low).
2	PX1	$\overline{INT0}$ (External Interrupt 1) priority (1 = High; 0 = Low).
1	PT0	Timer 0 Interrupt Priority (1 = High; 0 = Low).
0	PX0	$\overline{INT0}$ (External Interrupt 0) Priority (1 = High; 0 = Low).

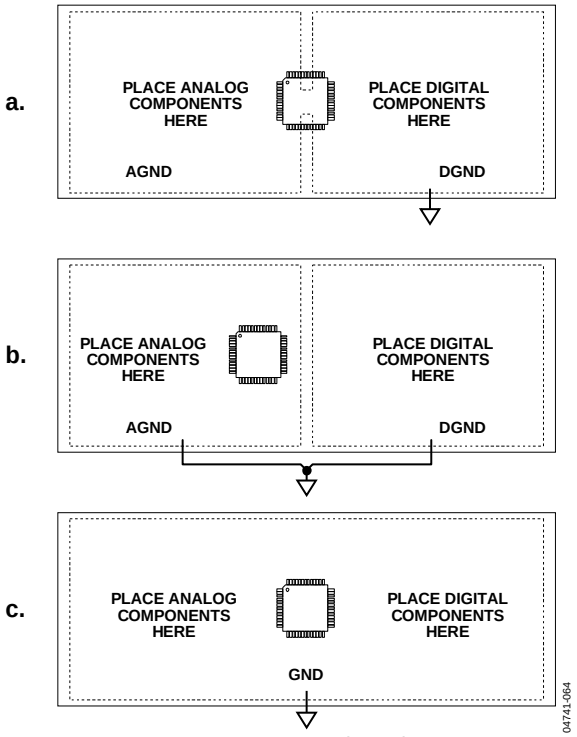

Figure 68. System Grounding Schemes

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the digital inputs of the ADuC845/ADuC847/ADuC848 add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the device. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the device and affecting the accuracy of ADC conversions.

When using the LFCSP package, it is recommended that the paddle underneath the chip be soldered to the board to provide maximum mechanical stability. However, it is recommended that this paddle not be grounded but left floating. All results and specifications contained in this data sheet are taken or recorded with the paddle floating.

System Self-Identification

In some hardware designs, it may be advantageous for the software to be able to identify the host MicroConverter.

The CHIPID SFR is a read-only register located at SFR address C2H. The upper nibble of this SFR designates the MicroConverter within the Σ-Δ ADC family. User software can read this SFR to identify the host MicroConverter and therefore execute slightly different code if required. The CHIPID SFR reads as follows for the Σ-Δ ADC family of MicroConverter products. Note that the ADuC845/ADuC847/ADuC848 are treated as one device as far as the CHIPID is concerned.

Table 63. CHIPID Values for Σ-Δ MicroConverter Products

Device	CHIPID
ADuC816	1xH
ADuC824	0xH
ADuC836	3xH
ADuC834	2xH
ADuC845/ADuC847/ADuC848	AxH

Clock Oscillator

As described earlier, the core clock frequency for the ADuC845/ADuC847/ADuC848 is generated from an on-chip PLL that locks onto a multiple (384 times) of 32.768 kHz. The latter is generated from an internal clock oscillator. To use the internal clock oscillator, connect a 32.768 kHz parallel resonant crystal between XTAL1 and XTAL2 as shown in Figure 69.

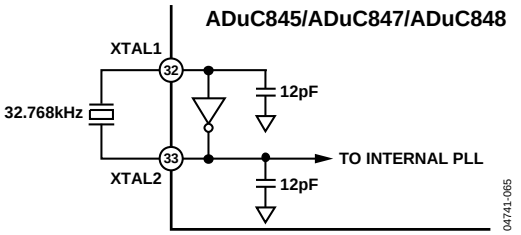

Figure 69. Crystal Connectivity to ADuC845/ADuC847/ADuC848

As shown in the typical external crystal connection diagram in Figure 69, two internal 12 pF capacitors are provided on-chip. These are connected internally, directly to the XTAL1 and XTAL2 pins. The total input capacitance at both pins is detailed in the Specifications table. Note that the total capacitance required for a particular crystal must be in accordance with the crystal manufacturer. However, in most cases, no additional external capacitance is required above that already supplied on-chip.

OTHER HARDWARE CONSIDERATIONS

In-Circuit Serial Download Access

Nearly all ADuC845/ADuC847/ADuC848 designs can take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the UART of the devices, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is shown in Figure 70 with a simple ADM3202-based circuit. If users would rather not include an RS-232 chip on the target board, refer to the uC006 Application Note, *A 4-Wire UART-to-PC Interface*, for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the device.

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADuC845BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC845BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC845BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-5-RL	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC845BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC845BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC845BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC845BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC845BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC847BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC847BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC847BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC847BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC847BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC847BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC847BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC847BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC847BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC847BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
ADuC848BSZ62-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 5 V	S-52-2
ADuC848BSZ62-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 62-kbyte, 3 V	S-52-2
ADuC848BSZ32-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 5 V	S-52-2
ADuC848BSZ32-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 32-kbyte, 3 V	S-52-2
ADuC848BSZ8-5	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 5 V	S-52-2
ADuC848BSZ8-3	−40°C to +125°C	52-Lead MQFP, Lead Free, 8-kbyte, 3 V	S-52-2
ADuC848BCPZ62-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 5 V	CP-56-11
ADuC848BCPZ62-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 62-kbyte, 3 V	CP-56-11
ADuC848BCPZ8-5	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 5 V	CP-56-11
ADuC848BCPZ8-3	−40°C to +85°C	56-Lead LFCSP, Lead Free, 8-kbyte, 3 V	CP-56-11
EVAL-ADuC845QSZ		QuickStart Development System	
EVAL-ADuC845QSPZ		QuickStart-PLUS Development System	
EVAL-ADuC847QSZ		QuickStart Development System	
EVAL-ADUC-CABLE1Z		ADuC Serial Downloader Cable for UART	

[1] The -3 and -5 in the Model column indicate the DV_{DD} operating voltage.
[2] Z = RoHS Compliant Part.
[3] The QuickStart Plus system can only be ordered directly from Accutron. It can be purchased from the website http://www.accutron.com.

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