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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x16b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc848bsz8-3

SPECIFICATIONS[1]

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V, REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz crystal; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Input buffer on for primary ADC, unless otherwise noted. Core speed = 1.57 MHz (default CD = 3), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY ADC					
Conversion Rate	5.4		105	Hz	Chop on (ADCMODE.3 = 0)
	16.06		1365	Hz	Chop off (ADCMODE.3 = 1)
No Missing Codes[2]	24			Bits	≤26.7 Hz update rate with chop enabled
	24			Bits	≤80.3 Hz update rate with chop disabled
Resolution (ADuC845/ADuC847)	See Table 11 and Table 15				
Resolution (ADuC848)	See Table 13 and Table 17				
Output Noise (ADuC845/ADuC847)	See Table 10 and Table 14			µV (rms)	Output noise varies with selected update rates, gain range, and chop status.
Output Noise (ADuC848)	See Table 12 and Table 16			µV (rms)	Output noise varies with selected update rates, gain range, and chop status.
Integral Nonlinearity			±15	ppm of FSR	1 LSB_{16}
Offset Error[3]		±3		µV	Chop on
					Chop off, offset error is in the order of the noise for the programmed gain and update rate following a calibration.
Offset Error Drift vs. Temperature[2]		±10		nV/°C	Chop on (ADCMODE.3 = 0)
		±200		nV/°C	Chop off (ADCMODE.3 = 1)
Full-Scale Error[4]					
ADuC845/ADuC847		±10		µV	±20 mV to ±2.56 V
ADuC848		±10		µV	±20 mV to ±640 mV
		±0.5		LSB_{16}	±1.28 V to ±2.56 V
Gain Error Drift vs. Temperature[4]		±0.5		ppm/°C	
Power Supply Rejection					
	80			dB	AIN = 1 V, ±2.56 V, chop enabled
		113		dB	AIN = 7.8 mV, ±20 mV, chop enabled
		80		dB	AIN = 1 V, ±2.56 V, chop disabled[2]
PRIMARY ADC ANALOG INPUTS					
Differential Input Voltage Ranges[5, 6]					Gain = 1 to 128
Bipolar Mode (ADC0CON1.5 = 0)		±1.024 × V_{REF}/GAIN		V	V_{REF} = REFIN(+) – REFIN(–) or REFIN2(+) – REFIN2(–) (or Int 1.25 V_{REF})
Unipolar Mode (ADC0CON1.5 = 1)		0 – 1.024 × V_{REF}/GAIN		V	V_{REF} = REFIN(+) – REFIN(–) or REFIN2(+) – REFIN2(–) (or Int 1.25 V_{REF})
ADC Range Matching		±2		µV	AIN = 18 mV, chop enabled
Common-Mode Rejection DC					Chop enabled, chop disabled
On AIN	95			dB	AIN = 7.8 mV, range = ±20 mV
		113		dB	AIN = 1 V, range = ±2.56 V
Common-Mode Rejection 50 Hz/60 Hz[2]					50 Hz/60 Hz ± 1 Hz, 16.6 Hz and 50 Hz update rate, chop enabled, REJ60 enabled
On AIN	95			dB	AIN = 7.8 mV, range = ±20 mV
	90			dB	AIN = 1 V, range = ±2.56 V

ABOSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
AV_{DD} to AGND	–0.3 V to +7 V
AV_{DD} to DGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
DV_{DD} to DGND	–0.3 V to +7 V
AGND to DGND[1]	–0.3 V to +0.3 V
AV_{DD} to DV_{DD}	–2 V to +5 V
Analog Input Voltage to AGND[2]	–0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	–0.3 V to AV_{DD} + 0.3 V
AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (MQFP)	90°C/W
θ_{JA} Thermal Impedance (LFCSP)	52°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] AGND and DGND are shorted internally on the ADuC845, ADuC847, and ADuC848.
[2] Applies to the P1.0 to P1.7 pins operating in analog or digital input modes.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin No.				
52-MQFP	56-LFCSP	Mnemonic	Type[1]	Description
9	9	P1.4/AIN5	I	On power-on default, P1.4/AIN5 is configured as the AIN5 analog input. AIN5 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN6. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
10	10	P1.5/AIN6	I	On power-on default, P1.5/AIN6 is configured as the AIN6 analog input. AIN6 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN5. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
11	11	P1.6/AIN7/IEXC1	I/O	On power-on default, P1.6/AIN7 is configured as the AIN7 analog input. AIN7 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN8. One or both current sources can also be configured at this pin. P1.6 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
12	12	P1.7/AIN8/IEXC2	I/O	On power-on default, P1.7/AIN8 is configured as the AIN8 analog input. AIN8 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN7. One or both current sources can also be configured at this pin. P1.7 has no digital output driver. It can, however, function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
13	13	AINCOM/DAC	I/O	All analog inputs can be referred to this pin, provided that a relevant pseudo differential input mode is selected. This pin also functions as an alternative pin out for the DAC.
14	14	DAC	O	The voltage output from the DAC, if enabled, appears at this pin.
Not applicable	15	AIN9	I	AIN9 can be used as a pseudo differential analog input when used with AINCOM or as the positive input of a fully differential pair when used with AIN10 (LFCSP version only).
Not applicable	16	AIN10	I	AIN10 can be used as a pseudo differential analog input when used with AINCOM or as the negative input of a fully differential pair when used with AIN9 (LFCSP version only).
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. This pin has an internal weak pull-down and a Schmitt trigger input stage.
16 to 19, 22 to 25	18 to 21, 24 to 27	P3.0 to P3.7	I/O	P3.0 to P3.7 are bidirectional port pins with internal pull-up resistors. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low source current because of the internal pull-up resistors. When driving a 0-to-1 output transition, a strong pull-up is active for one core clock period of the instruction cycle. Port 3 pins also have the various secondary functions described in this table.
16	18	P3.0/RxD		Receiver Data for UART Serial Port.
17	19	P3.1/TxD		Transmitter Data for UART Serial Port.
18	20	P3.2/$\overline{\text{INT0}}$		External Interrupt 0. This pin can also be used as a gate control input to Timer 0.
19	21	P3.3/$\overline{\text{INT1}}$		External Interrupt 1. This pin can also be used as a gate control input to Timer 1.
22	24	P3.4/T0		Timer/Counter 0 External Input.
23	25	P3.5/T1		Timer/Counter 1 External Input.
24	26	P3.6/$\overline{\text{WR}}$		External Data Memory Write Strobe. This pin latches the data byte from Port 0 into an external data memory.
25	27	P3.7/$\overline{\text{RD}}$		External Data Memory Read Strobe. This pin enables the data from an external data memory to Port 0.

Power Control Register (PCON)

The PCON SFR contains bits for power-saving options and general-purpose status flags as listed in Table 6.

SFR Address: 87H
Power-On Default: 00H
Bit Addressable: No

Table 6. PCON SFR Bit Designations

Bit No.	Name	Description
7	SMOD	Double UART Baud Rate. 0 = Normal, 1 = Double Baud Rate.
6	SERIPD	Serial Power-Down Interrupt Enable. If this bit is set, a serial interrupt from either SPI or I^2C can terminate the power-down mode.
5	INT0PD	INT0 Power-Down Interrupt Enable. If this bit is set, either a level ($\overline{IT0}$ = 0) or a negative-going transition ($\overline{IT0}$ = 1) on the INT0 pin terminates power-down mode.
4	ALEOFF	If set to 1, the ALE output is disabled.
3	GF1	General-Purpose Flag Bit.
2	GF0	General-Purpose Flag Bit.
1	PD	Power-Down Mode Enable. If set to 1, the device enters power-down mode.
0	-----	Not Implemented. Write Don't Care.

ADuC845/ADuC847/ADuC848 Configuration Register (CFG845/CFG847/CFG848)

The CFG845/CFG847/CFG848 SFR contains the bits necessary to configure the internal XRAM and the extended SP. By default, it configures the user into 8051 mode, that is, extended SP, and the internal XRAM are disabled. When using in a program, use the device name only, that is, CFG845, CFG847, or CFG848.

SFR Address: AFH
Power-On Default: 00H
Bit Addressable: No

Table 7. CFG845/CFG847/CFG848 SFR Bit Designations

Bit No.	Name	Description
7	EXSP	Extended SP Enable. If this bit is set to 1, the stack rolls over from SPH/SP = 00FFH to 0100H. If this bit is cleared to 0, SPH SFR is disabled and the stack rolls over from SP = FFH to SP = 00H.
6	----	Not Implemented. Write Don't Care.
5	----	Not Implemented. Write Don't Care.
4	----	Not Implemented. Write Don't Care.
3	----	Not Implemented. Write Don't Care.
2	----	Not Implemented. Write Don't Care.
1	----	Not Implemented. Write Don't Care.
0	XRAMEN	If this bit is set to 1, the internal XRAM is mapped into the lower 2 kbytes of the external address space. If this bit is cleared to 0, the internal XRAM is accessible and up to 16 MB of external data memory become available. See Figure 8.

Signal Chain Overview with Chop Disabled ($\overline{CHOP}$ = 1)

With $\overline{CHOP}$ = 1, chop is disabled and the available output rates vary from 16.06 Hz to 1.365 kHz. The range of applicable SF words is from 3 to 255. When switching between channels with chop disabled, the channel throughput rate is higher than when chop is enabled. The drawback with chop disabled is that the drift performance is degraded and offset calibration is required following a gain range change or significant temperature change. A block diagram of the ADC input channel with chop disabled is shown in Figure 15.

The signal chain includes a multiplex or buffer, PGA, Σ-Δ modulator, and digital filter. The modulator bit stream is applied to a Sinc^3 filter. Programming the Sinc^3 decimation factor is restricted to an 8-bit register SF; the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) is therefore

$$f_{ADC} = \frac{1}{8 \times SF} \times f_{MOD}$$

where:
f_{ADC} is the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register, valid range is from 3 to 255.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The settling time to a step input is governed by the digital filter. A synchronized step change requires a settling time of three times the programmed update rate; a channel change can be treated as a synchronized step change. This is one conversion longer than the case for chop enabled. However, because the ADC throughput is three times faster with chop disabled than it is with chop enabled, the actual time to a settled ADC output is significantly less also. This means that following a synchronized step change, the ADC requires three conversions (note: data is not output following a synchronized ADC change until data has settled) before the result accurately reflects the new input voltage.

$$t_{SETTLE} = \frac{3}{f_{ADC}} = 3 \times t_{ADC}$$

An unsynchronized step change requires four conversions to accurately reflect the new analog input at its output. Note that with an unsynchronized change the ADC continues to output data and so the user must take unsettled outputs into account. Again, this is one conversion longer than with chop enabled, but because the ADC throughput with chop disabled is faster than with chop enabled, the actual time taken to obtain a settled ADC output is less.

The allowable range for SF is 3 to 255 with a default of 69 (45H). The corresponding conversion rates, rms, and peak-to-peak noise performances are shown in Table 14, Table 15, Table 16, and Table 17. Note that the conversion time increases by 0.244 ms for each increment in SF.

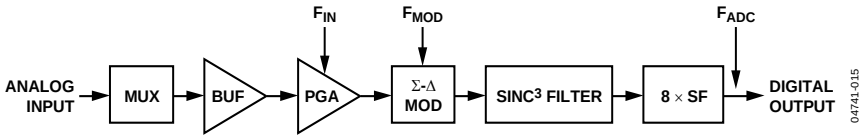

Figure 15. Block Diagram of ADC Input Channel with Chop Disabled

AUXILIARY ADC (ADUC845 ONLY)

Table 18. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Enabled

SF Word	Data Update Rate (Hz)	μV
13	105.03	17.46
23	59.36	3.13
27	50.56	4.56
69	19.79	2.66
255	5.35	1.13

Table 19. ADuC845 Typical Peak-to-Peak Resolution (Bits) vs. Update Rate[1] with Chop Enabled

SF Word	Data Update Rate (Hz)	Bits
13	105.03	15.5
23	59.36	18
27	50.56	17.5
69	19.79	18
255	5.35	19.5

[1] ADC converting in bipolar mode.

Table 20. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	μV
3	1365.33	1386.58
13	315.08	34.94
66	62.06	3.2
69	59.36	3.19
81	50.57	3.14
255	16.06	1.71

Table 21. ADuC845 Peak-to-Peak Resolution (Bits) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Bits
3	1365.33	9
13	315.08	14.5
66	62.06	18
69	59.36	18
81	50.57	18
255	16.06	19

REFERENCE INPUTS

The ADuC845/ADuC847/ADuC848 each have two separate differential reference inputs, REFIN± and REFIN2±. While both references are available for use with the primary ADC, only REFIN± is available for the auxiliary ADC (ADuC845 only). The common-mode range for these differential references is from AGND to AV_{DD}. The nominal external reference voltage is 2.5 V, with the primary and auxiliary (ADuC845 only) reference select bits configured from the ADC0CON2 and ADC1CON (ADuC845 only), respectively.

When an external reference voltage is used, the primary ADC sees this internally as a 2.56 V reference ($V_{REF} \times 1.024$). Therefore, any calculations of LSB size should account for this. For instance, with a 2.5 V external reference connected and using a gain of 1 on a unipolar range (2.56 V), the LSB size is $(2.56/2^{24}) = 152.6$ nV (if using the 24-bit ADC on the ADuC845 or ADuC847). If a bipolar gain of 4 is used (±640 mV), the LSB size is $(±640 \text{ mV})/2^{24}) = 76.3$ nV (again using the 24-bit ADC on the ADuC845 or ADuC847).

The ADuC845/ADuC847/ADuC848 can also be configured to use the on-chip band gap reference via the XREF0/1 bits in the ADC0CON2 SFR (for primary ADC) or the AXREF bit in ADC1CON (for auxiliary ADC (ADuC845 only)). In this mode of operation, the ADC sees the internal reference of 1.25 V, thereby halving all the input ranges. A consequence of using the internal band gap reference is a noticeable degradation in peak-to-peak resolution. For this reason, operation with an external reference is recommended.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference inputs for the device, the effect of any low frequency noise in the excitation source is removed because the application is ratiometric. If the devices are not used in a ratiometric configuration, use a low noise reference. Recommended reference voltage sources for the ADuC845/ADuC847/ADuC848 include the ADR421, REF43, and REF192.

The reference inputs provide a high impedance, dynamic load to external connections. Because the impedance of each reference input is dynamic, resistor/capacitor combinations on these pins can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources, such as those mentioned above, for example, the ADR421, typically have low output impedances, and, therefore, decoupling capacitors on the REFIN± or REFIN2± inputs would be recommended (typically 0.1 μF). Deriving the reference voltage from an external resistor configuration means that the reference input sees a significant external source impedance. External decoupling of the REFIN± and/or REFIN2± inputs is not recommended in this type of configuration.

BURNOUT CURRENT SOURCES

The primary ADC on the ADuC845 and the ADC on the ADuC847 and ADuC848 incorporate two 100 nA constant current generators that are used to detect a failure in a connected sensor. One sources current from the AV_{DD} to AIN(+), and one sinks current from AIN(−) to AGND. These currents are only configurable for use on AIN5/AIN6 and/or AIN7/AIN8 in differential mode only, from the ICON.6 bit in the ICON SFR

TYPICAL PERFORMANCE CHARACTERISTICS

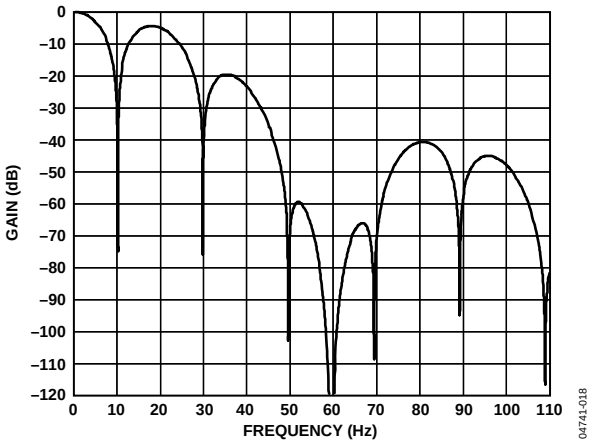

Figure 18. Filter Response, Chop On, SF = 69 Decimal

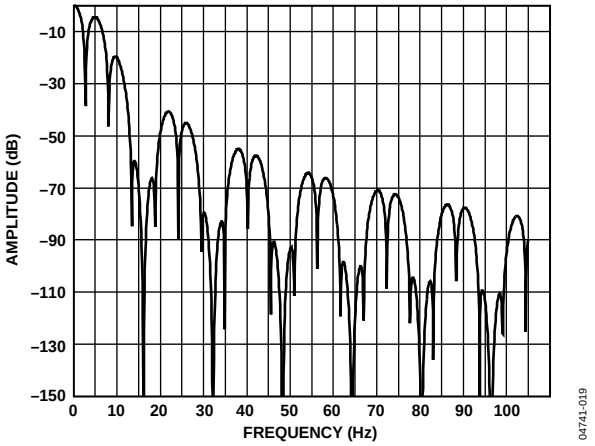

Figure 19. Filter Response, Chop On, SF = 255 Decimal

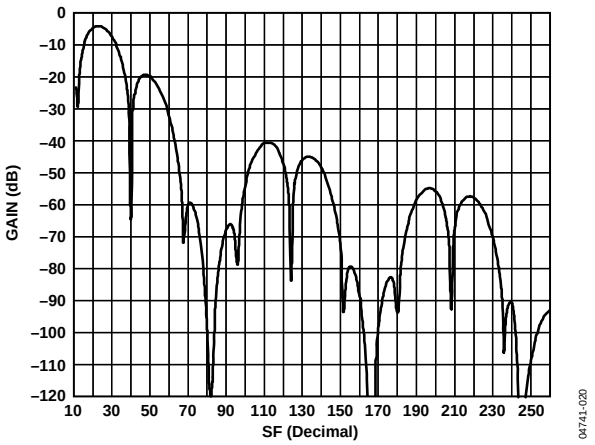

Figure 20. 50 Hz Normal Mode Rejection vs. SF Word, Chop On

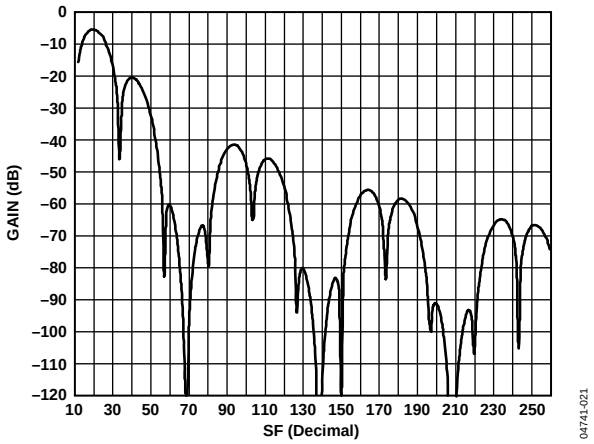

Figure 21. 60 Hz Normal Mode Rejection vs. SF, Chop On

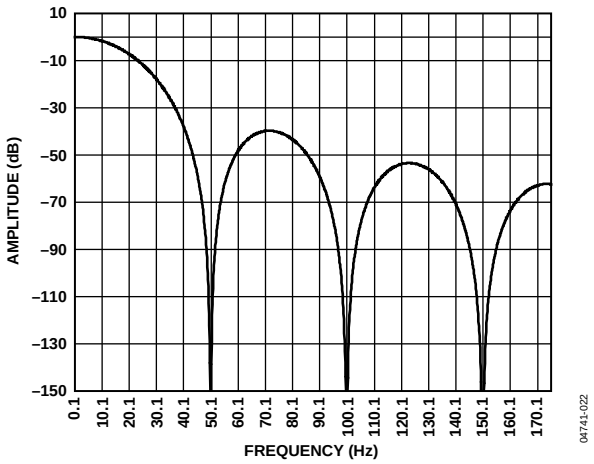

Figure 22. Chop Off, Fadc = 50 Hz, SF = 52H

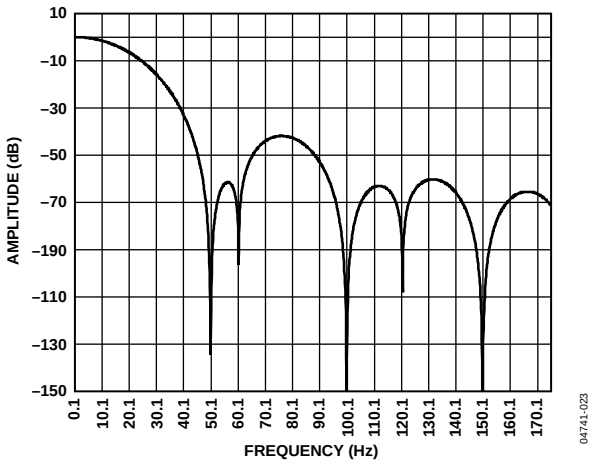

Figure 23. Chop Off, SF = 52H, REJ60 Enabled

ADCSTAT (ADC STATUS REGISTER)

This SFR reflects the status of both ADCs including data ready, calibration, and various (ADC-related) error and warning conditions including REFIN± reference detect and conversion overflow/underflow flags.

SFR Address: D8H
Power-On Default: 00H
Bit Addressable: Yes

Table 23. ADCSTAT SFR Bit Designation

Bit No.	Name	Description
7	RDY0	Ready Bit for the Primary ADC. Set by hardware on completion of conversion or calibration. Cleared directly by the user, or indirectly by a write to the mode bits, to start calibration. The primary ADC is inhibited from writing further results to its data or calibration registers until the RDY0 bit is cleared.
6	RDY1	Ready Bit for Auxiliary (ADuC845 only) ADC. Same definition as RDY0 referred to the auxiliary ADC. Valid on the ADuC845 only.
5	CAL	Calibration Status Bit. Set by hardware on completion of calibration. Cleared indirectly by a write to the mode bits to start another ADC conversion or calibration. Note that calibration with the temperature sensor selected (auxiliary ADC on the ADuC845 only) fails to complete.
4	NOXREF	No External Reference Bit (only active if primary or auxiliary (ADuC845 only) ADC is active). Set to indicate that one or both of the REFIN pins is floating or the applied voltage is below a specified threshold. When set, conversion results are clamped to all 1s. Only detects invalid REFIN±, does not check REFIN2±. Cleared to indicate valid V_{REF}.
3	ERR0	Primary ADC Error Bit. Set by hardware to indicate that the result written to the primary ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Cleared by a write to the mode bits to initiate a conversion or calibration.
2	ERR1	Auxiliary ADC Error Bit. Same definition as ERR0 referred to the auxiliary ADC. Valid on the ADuC845 only.
1	–––	Not Implemented. Write Don't Care.
0	–––	Not Implemented. Write Don't Care.

ADCMODE (ADC MODE REGISTER)

Used to control the operational mode of both ADCs.

SFR Address: D1H
Power-On Default: 08H
Bit Addressable: No

Table 24. ADCMODE SFR Bit Designations

Bit No.	Name	Description
7	---	Not Implemented. Write Don't Care.
6	REJ60	Automatic 60 Hz Notch Select Bit. Setting this bit places a notch in the frequency response at 60 Hz, allowing simultaneous 50 Hz and 60 Hz rejection at an SF word of 82 decimal. This 60 Hz notch can be set only if SF ≥68 decimal, that is, the regular filter notch must be ≤60 Hz. This second notch is placed at 60 Hz only if the device clock is at 32.768 kHz.
5	ADC0EN	Primary ADC Enable. Set by the user to enable the primary ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the primary ADC into power-down mode.
4	ADC1EN (ADuC845 only)	Auxiliary (ADuC845 only) ADC Enable. Set by the user to enable the auxiliary (ADuC845 only) ADC and place it in the mode selected in MD2–MD0. Cleared by the user to place the auxiliary (ADuC845 only) ADC in power-down mode.
3	$\overline{\text{CHOP}}$	Chop Mode Disable. Set by the user to disable chop mode on both the primary and auxiliary (ADuC845 only) ADC allowing a three times higher ADC data throughput. SF values as low as 3 are allowed with this bit set, giving up to 1.3 kHz ADC update rates. Cleared by the user to enable chop mode on both the primary and auxiliary (ADuC845 only) ADC.
2, 1, 0	MD2, MD1, MD0	Primary and Auxiliary (ADuC845 only) ADC Mode Bits. These bits select the operational mode of the enabled ADC as follows: MD2 MD1 MD0 0 0 0 ADC Power-Down Mode (Power-On Default). 0 0 1 Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided. 0 1 0 Single Conversion Mode. In single conversion mode, a single conversion is performed on the enabled ADC. Upon completion of a conversion, the ADC data registers (ADC0H/M/L and/or ADC1H/M/L (ADuC845 only)) are updated. The relevant flags in the ADCSTAT SFR are written, and power-down is re-entered with the MD2–MD0 accordingly being written to 000. Note that ADC0L is not available on the ADuC848. 0 1 1 Continuous Conversion. In continuous conversion mode, the ADC data registers are regularly updated at the selected update rate (see the Sinc Filter SFR Bit Designations in Table 28). 1 0 0 Internal Zero-Scale Calibration. Internal short automatically connected to the enabled ADC input(s). 1 0 1 Internal Full-Scale Calibration. Internal or external REFIN± or REFIN2± V_{REF} (as determined by XREF bits in ADC0CON2 and/or AXREF (ADuC845 only) in ADC1CON (ADuC845 only) is automatically connected to the enabled ADC input(s) for this calibration. 1 1 0 System Zero-Scale Calibration. User should connect system zero-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers. 1 1 1 System Full-Scale Calibration. User should connect system full-scale input to the enabled ADC input(s) as selected by CH3–CH0 and ACH3–ACH0 bits in the ADC0CON2 and ADC1CON (ADuC845 only) registers.

DAC CIRCUIT INFORMATION

The ADuC845/ADuC847/ADuC848 incorporate a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF, and has two selectable ranges, 0 V to V_{REF} and 0 V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register, DACCON, and two data registers, DACH/L. The DAC output can be programmed to appear at Pin 14 (DAC) or Pin 13 (AINCOM).

In 12-bit mode, the DAC voltage output is updated as soon as the DACL data SFR is written; therefore, the DAC data registers should be updated as DACH first, followed by DACL. The 12-bit DAC data should be written into DACH/L right-justified such that DACL contains the lower 8 bits, and the lower nibble of DACH contains the upper 4 bits.

DACCON Control Register

SFR Address: FDH
Power-On Default: 00H
Bit Addressable: No

Table 33. DACCON—DAC Configuration Commands

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	–––	Not Implemented. Write Don't Care.
5	–––	Not Implemented. Write Don't Care.
4	DACPIN	DAC Output Pin Select. Set to 1 by the user to direct the DAC output to Pin 13 (AINCOM). Cleared to 0 by the user to direct the DAC output to Pin 14 (DAC).
3	DAC8	DAC 8-Bit Mode Bit. Set to 1 by the user to enable 8-bit DAC operation. In this mode, the 8 bits in DACL SFR are routed to the 8 MSBs of the DAC, and the 4 LSBs of the DAC are set to 0. Cleared to 0 by the user to enable 12-bit DAC operation. In this mode, the 8 LSBs of the result are routed to DACL, and the upper 4 MSB bits are routed to the lower 4 bits of DACH.
2	DACRN	DAC Output Range Bit. Set to 1 by the user to configure the DAC range of 0 V to AV_{DD}. Cleared to 0 by the user to configure the DAC range of 0 V to 2.5 V (V_{REF}).
1	DACCLR	DAC Clear Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to reset the DAC data registers DACL/H to 0.
0	DACEN	DAC Enable Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to power down the DAC.

DACH/DACL Data Registers

These DAC data registers are written to by the user to update the DAC output.

SFR Address: DACL (DAC data low byte)—FBH
DACH (DAC data high byte)—FCH
Power-On Default: 00H (both registers)
Bit Addressable: No (both registers)

Mode 5 (Dual 8-Bit PWM)

In Mode 5, the duty cycle and the resolution of the PWM outputs are individually programmable. The maximum resolution of the PWM output is 8 bits.

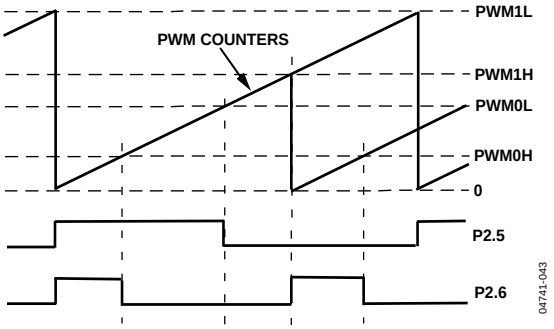

Figure 43. PWM Mode 5

Mode 6 (Dual RZ 16-Bit Σ-Δ DAC)

Mode 6 provides a high speed PWM output similar to that of a Σ-Δ DAC. Mode 6 operates very similarly to Mode 4; however, the key difference is that Mode 6 provides return to zero (RZ) Σ-Δ DAC output. Mode 4 provides non-return-to-zero Σ-Δ DAC outputs. RZ mode ensures that any difference in the rise and fall times does not affect the Σ-Δ DAC INL. However, RZ mode halves the dynamic range of the Σ-Δ DAC outputs from 0 V– to AV_{DD} down to 0 V to $AV_{DD}/2$. For best results, this mode should be used with a PWM clock divider of 4.

If PWM1H is set to 4010H (slightly above one-quarter of FS), typically P2.6 is low for three full clocks (3 × 80 ns), high for one-half a clock (40 ns), and then low again for one-half a clock (40 ns) before repeating itself. Over every 65536 clocks, the PWM compromises for the fact that the output should be slightly above one-quarter of full scale by leaving the output high for two half clocks in four every so often.

For faster DAC outputs (at lower resolution), write 0s to the LSBs that are not required with a 1 in the LSB position. If, for example, only 12-bit performance is required, write 0001 to the 4 LSBs. This means that a 12-bit accurate Σ-Δ DAC output can occur at 3 kHz. Similarly, writing 00000001 to the 8 LSBs gives an 8-bit accurate Σ-Δ DAC output at 49 kHz.

The output resolution is set by the PWM1L and PWM1H SFRs for the P2.5 and P2.6 outputs, respectively. PWM0L and PWM0H set the duty cycles of the PWM outputs at P2.5 and P2.6, respectively. Both PWMs have the same clock source and clock divider.

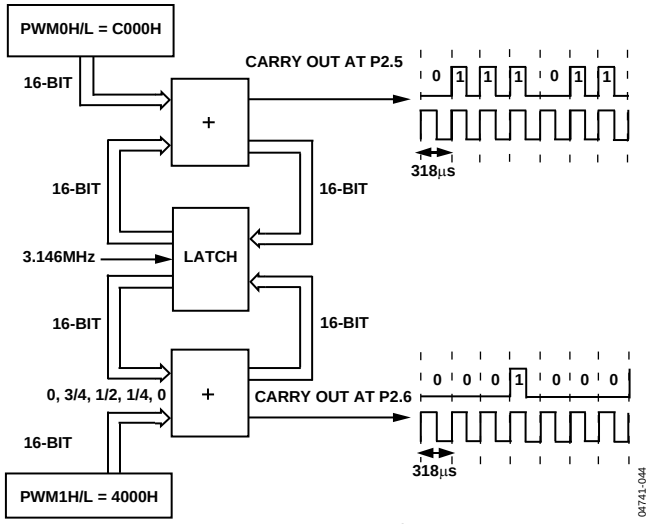

Figure 44. PWM Mode 6

Mode 7

In Mode 7, the PWM is disabled, allowing P2.5 and P2.6 to be used as normal.

I2CADD—I²C Address Register 1

Function:	Holds one of the I²C peripheral addresses for the device. It may be overwritten by user code. The uC001 Application Note describes the format of the I²C standard 7-bit address.
SFR Address:	9BH
Power-On Default:	55H
Bit Addressable:	No

I2CADD1—I²C Address Register 2

Function:	Same as the I2CADD.
SFR Address:	F2H
Power-On Default:	7FH
Bit Addressable:	No

I2CDAT—I²C Data Register

Function:	The I2CDAT SFR is written to by user code to transmit data, or read by user code to read data just received by the I²C interface. Accessing I2CDAT automatically clears any pending I²C interrupt and the I2CI bit in the I2CCON SFR. User code should access I2CDAT only once per interrupt cycle.
SFR Address:	9AH
Power-On Default:	00H
Bit Addressable:	No

The main features of the MicroConverter I²C interface are

- Only two bus lines are required: a serial data line (SDATA) and a serial clock line (SCLOCK).
- An I²C master can communicate with multiple slave devices. Because each slave device has a unique 7-bit address, single master/slave relationships can exist at all times even in a multislave environment.
- The ability to respond to two separate addresses when operating in slave mode.
- On-chip filtering rejects <50 ns spikes on the SDATA and the SCLOCK lines to preserve data integrity.

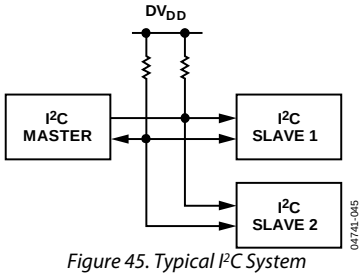

Figure 45. Typical I²C System

Software Master Mode

The ADuC845/ADuC847/ADuC848 can be used as an I²C master device by configuring the I²C peripheral in master mode and writing software to output the data bit-by-bit. This is referred to as a software master. Master mode is enabled by setting the I2CM bit in the I2CCON register.

To transmit data on the SDATA line, MDE must be set to enable the output driver on the SDATA pin. If MDE is set, the SDATA pin is pulled high or low depending on whether the MDO bit is set or cleared. MCO controls the SCLOCK pin and is always configured as an output in master mode. In master mode, the SCLOCK pin is pulled high or low depending on the whether MCO is set or cleared.

To receive data, MDE must be cleared to disable the output driver on SDATA. Software must provide the clocks by toggling the MCO bit and reading the SDATA pin via the MDI bit. If MDE is cleared, MDI can be used to read the SDATA pin. The value of the SDATA pin is latched into MDI on a rising edge of SCLOCK. MDI is set if the SDATA pin is high on the last rising edge of SCLOCK. MDI is cleared if the SDATA pin is low on the last rising edge of SCLOCK.

Software must control MDO, MCO, and MDE appropriately to generate the start condition, slave address, acknowledge bits, data bytes, and stop conditions. These functions are described in the uC001 Application Note.

TIMECON—TIC Control Register

SFR Address: A1H
Power-On Default: 00H
Bit Addressable: No

Table 45. TIMECON SFR Bit Designations

Bit No.	Name	Description
7	----	Not Implemented. Write Don't Care.
6	TFH	Twenty-Four Hour Select Bit. Set by the user to enable the hour counter to count from 0 to 23. Cleared by the user to enable the hour counter to count from 0 to 255.
5, 4	ITS1, ITS0	Interval Timebase Selection Bits. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	ST1	Single Time Interval Bit. Set by the user to generate a single interval timeout. If set, a timeout clears the TIEN bit. Cleared by the user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. Set when the 8-bit interval counter matches the value in the INTVAL SFR. Cleared by user software.
1	TIEN	Time Interval Enable Bit. Set by the user to enable the 8-bit time interval counter. Cleared by the user to disable the interval counter.
0	TCEN	Time Clock Enable Bit. Set by the user to enable the time clock to the time interval counters. Cleared by the user to disable the clock to the time interval counters and reset the time interval SFRs to the last value written to them by the user. The time registers (HTHSEC, SEC, MIN, and HOUR) can be written while TCEN is low.

Timer/Counter 0 and 1 Operating Modes

This section describes the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 52 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

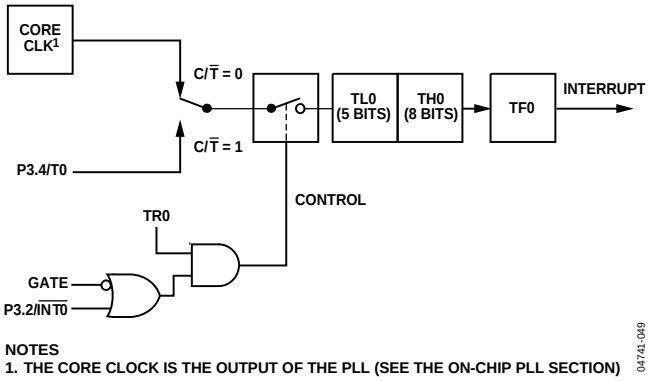

Figure 52. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 53.

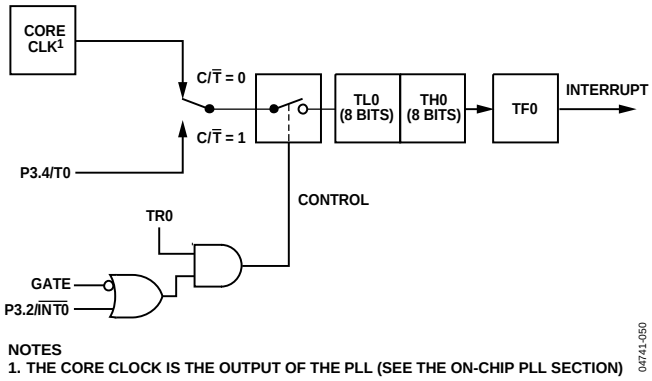

Figure 53. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload as shown in Figure 54. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

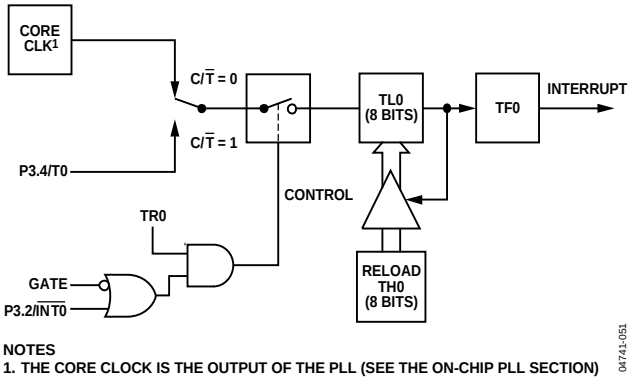

Figure 54. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 55. TL0 uses the Timer 0 Control Bits C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 then controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

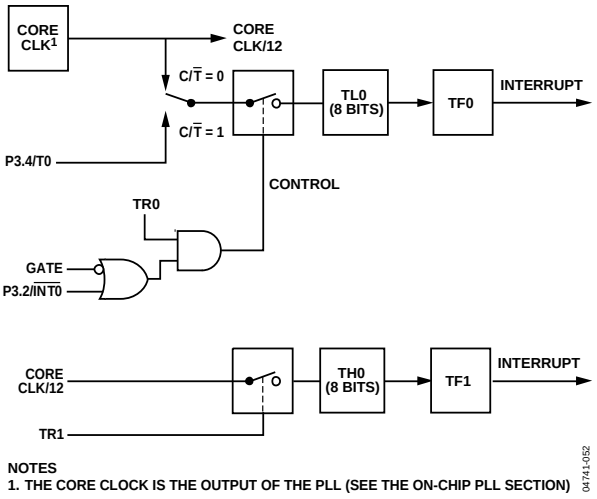

Figure 55. Timer/Counter 0, Mode 3

T2CON—Timer/Counter 2 Control Register

SFR Address: C8H
Power-On Default: 00H
Bit Addressable: Yes

Table 52. T2CON SFR Bit Designations

Bit No.	Name	Description
7	TF2	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	EXF2	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. Cleared by user software.
5	RCLK	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. Set by the user to select the counter function (input from external T2 pin). Cleared by the user to select the timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and as timer capture/reload registers.

TH2 and TL2—Timer 2 data high byte and low byte.
SFR Address: CDH and CCH respectively.
Power-On Default: 00H and 00H, respectively.

RCAP2H and RCAP2L—Timer 2 capture/reload byte and low byte.
SFR Address: CBH and CAH, respectively.
Power-On Default: 00H and 00H, respectively.

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART Serial Port Baud Rate Generation

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(\frac{CoreClockFrequency}{12}\right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Core\ Clock\ Frequency$$

Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or in both (one for transmit and the other for receive).

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{CoreClockFrequency}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{1}{16} \times Timer\ 2\ Overflow\ Rate$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 60.

In this case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{Core\ \ Clock\ \ Frequency}{(16 \times [65536\ - (RCAP\ 2H\ :RCAP\ 2L)])}$$

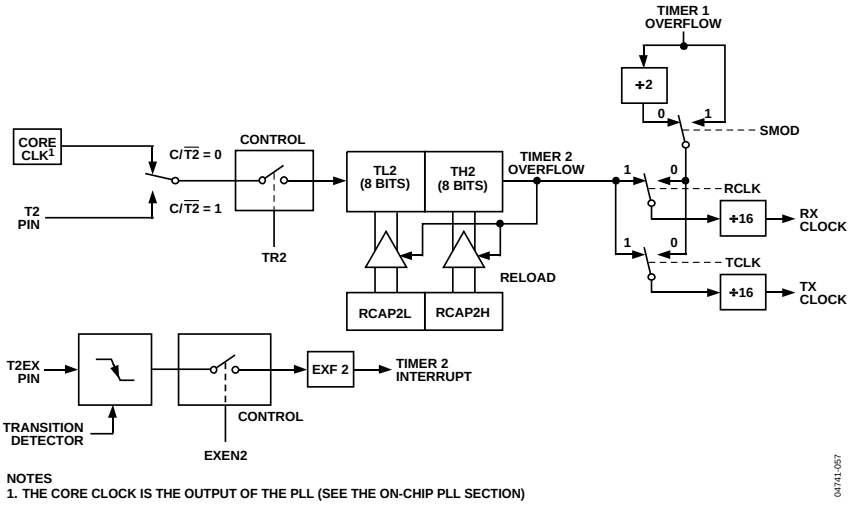

Figure 60. Timer 2, UART Baud Rates

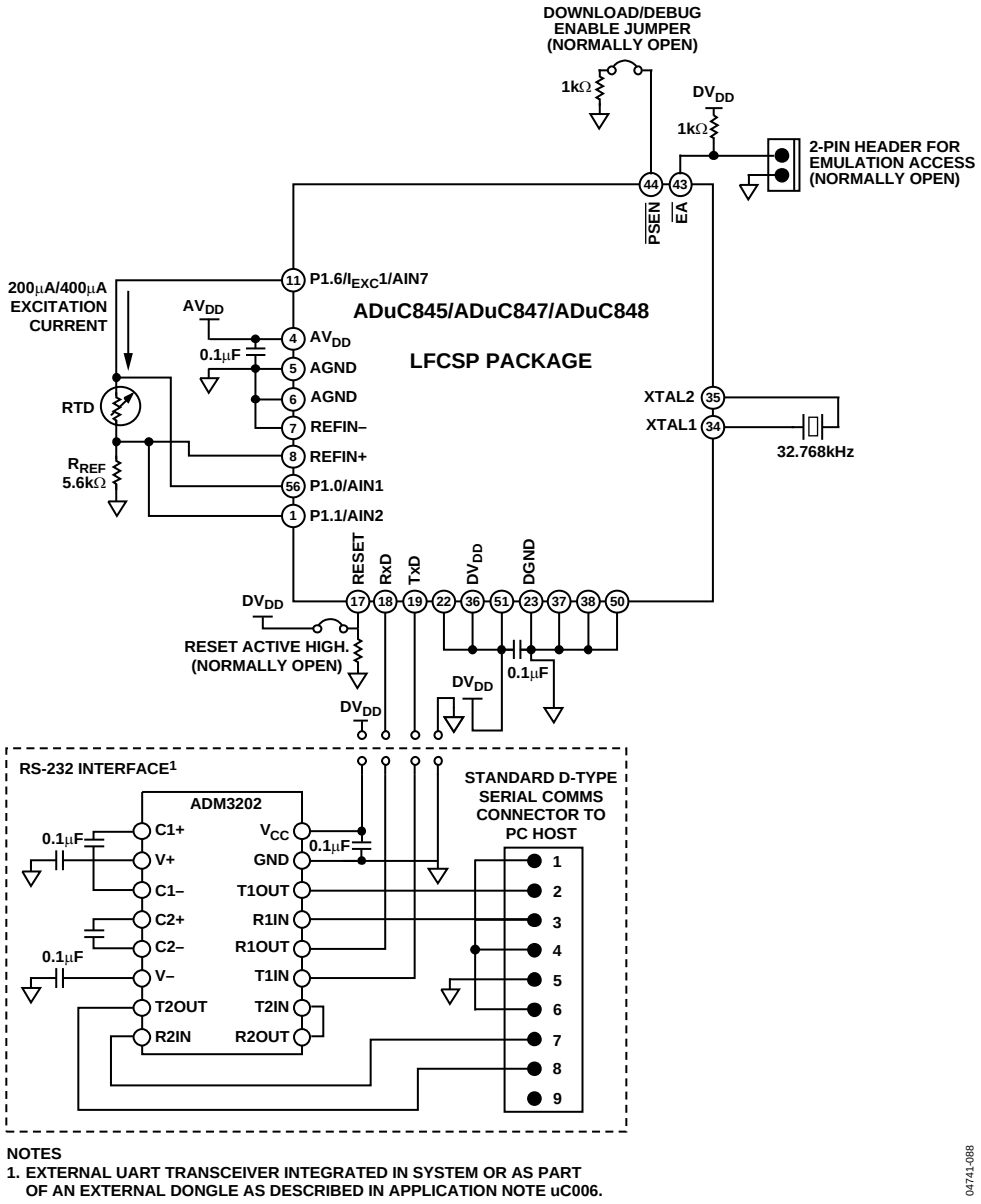

Figure 70. UART Connectivity in Typical System

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 70. To get the devices into download mode, connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it is ready to receive a new program serially. With the jumper removed, the device powers on in normal mode (and runs the program) whenever power is cycled or RESET is toggled. Note that $\overline{\text{PSEN}}$ is normally an output and that it is sampled as an input only on the falling edge of RESET, that is, at power-on or upon an external manual reset. Note also that if any external circuitry unintentionally pulls $\overline{\text{PSEN}}$ low during power-on or reset events, it may cause the chip to enter download mode and fail to begin user code execution. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself or the method of download entry in use during a reset or power-cycle condition.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described previously. In fact, both serial download and serial port debug modes are essentially one mode of operation used in two different ways.

The serial port debugger is fully contained on the device, unlike ROM monitor type debuggers, and, therefore, no external memory is needed to enable in-system debug sessions.

TIMING SPECIFICATIONS

AC inputs during testing are driven at DV_{DD} – 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements are made at V_{IH} min for Logic 1 and V_{IL} max for Logic 0 as shown in Figure 72.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 72.

C_{LOAD} for all outputs = 80 pF, unless otherwise noted.

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 64. CLOCK INPUT (External Clock Driven XTAL1) Parameter

		32.768 kHz External Crystal			
		Min	Typ	Max	Unit
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		6.26		µs
t_{CKH}	XTAL1 Width High		6.26		µs
t_{CKR}	XTAL1 Rise Time		9		ns
t_{CKF}	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	Core Clock Frequency[1]	0.098	1.57	12.58	MHz
t_{CORE}	Core Clock Period[2]		0.636		µs
t_{CYC}	Machine Cycle Time[3]	10.2	0.636	0.08	µs

[1] ADuC845/ADuC847/ADuC848 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 12.58 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[2] This number is measured at the default Core_Clk operating frequency of 1.57 MHz.
[3] ADuC845/ADuC847/ADuC848 machine cycle time is nominally defined as 1/Core_Clk.

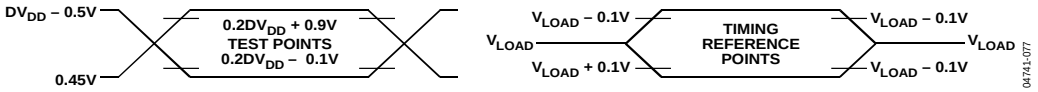

Figure 72. Timing Waveform Characteristics

Table 70. SPI SLAVE MODE TIMING (CPHA = 1) Parameter

		Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns
t_{SL}	SCLOCK Low Pulse Width		330		ns
t_{SH}	SCLOCK High Pulse Width		330		ns
t_{DAV}	Data Output Valid After SCLOCK Edge			50	ns
t_{DSU}	Data Input Setup Time Before SCLOCK Edge	100			ns
t_{DHD}	Data Input Hold Time After SCLOCK Edge	100			ns
t_{DF}	Data Output Fall Time		10	25	ns
t_{DR}	Data Output Rise Time		10	25	ns
t_{SR}	SCLOCK Rise Time		10	25	ns
t_{SF}	SCLOCK Fall Time		10	25	ns
t_{SFS}	$\overline{SS}$ High After SCLOCK Edge	0			ns

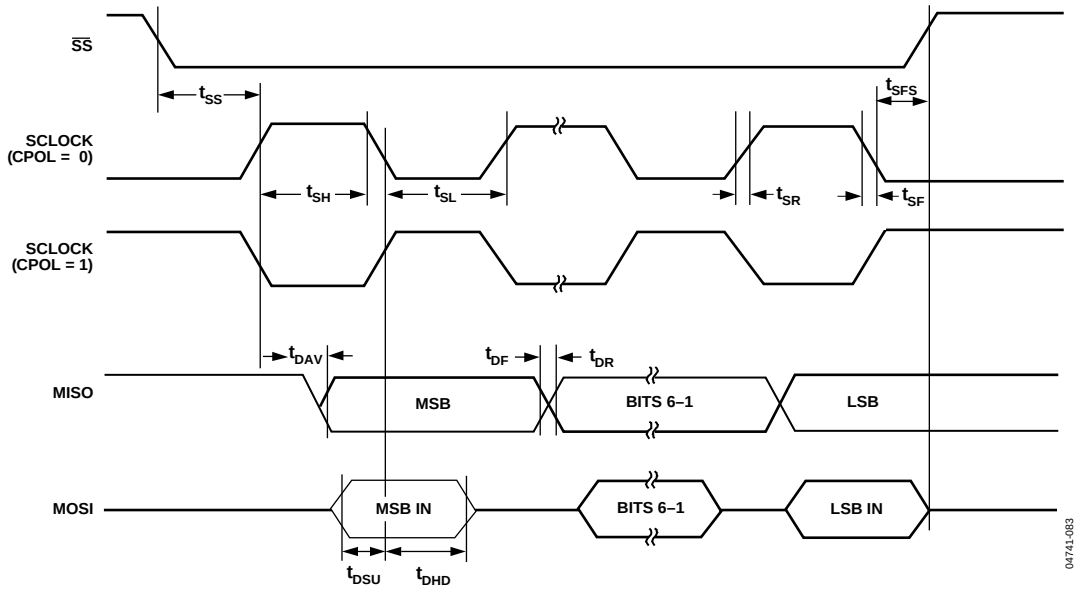

Figure 78. SPI Slave Mode Timing (CHPA = 1)

Table 72. UART TIMING (SHIFT REGISTER MODE) Parameter

		12.58 MHz Core_Clk			Variable Core_Clk			
		Min	Typ	Max	Min	Typ	Max	Unit
TXLXL	Serial Port Clock Cycle Time		954			$12t_{core}$		ns
TQVXH	Output Data Setup to Clock	662						ns
TDVXH	Input Data Setup to Clock	292						ns
TXHDX	Input Data Hold After Clock	0						ns
TXHQX	Output Data Hold After Clock	22						ns

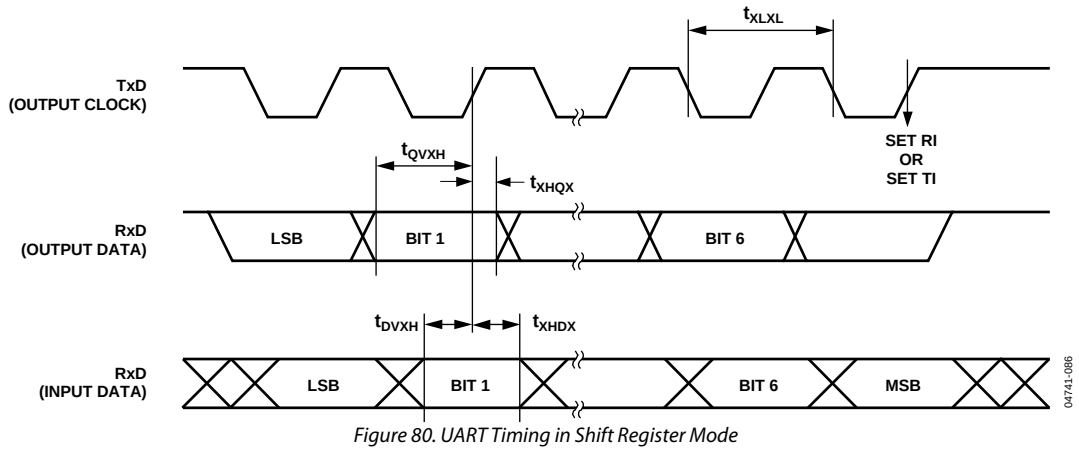

Figure 80. UART Timing in Shift Register Mode