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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PSM, PWM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.25K x 8
Voltage - Supply (Vcc/Vdd)	4.75V ~ 5.25V
Data Converters	A/D 10x16b; D/A 1x12b, 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc848bsz8-5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PWM					
–Fxtal		3		µA	
–Fvco		0.5		mA	
TIC		1		µA	
3 V Power Consumption					2.7 V < DV_{DD} < 3.6 V, AV_{DD} = 3.6 V
Normal Mode[11, 12]					
DV_{DD} Current			4.8	mA	Core clock = 1.57 MHz
		9	11	mA	Core clock = 6.29 MHz (CD = 1)
AV_{DD} Current			180	µA	ADC not enabled
Power-Down Mode[11, 12]					
DV_{DD} Current		20	26	µA	T_{MAX} = 85°C; OSC on; TIC on
		29		µA	T_{MAX} = 125°C; OSC on; TIC on
		14	20	µA	T_{MAX} = 85°C; OSC off
		21		µA	T_{MAX} = 125°C; OSC off
AV_{DD} Current			1	µA	T_{MAX} = 85°C; OSC on or off
			3	µA	T_{MAX} = 125°C; OSC on or off

[1] Temperature range is for ADuC845BS; for the ADuC847BS and ADuC848BS (MQFP package), the range is –40°C to +125°C. Temperature range for ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) is –40°C to +85°C.
[2] These numbers are not production tested but are guaranteed by design and/or characterization data on production release.
[3] System zero-scale calibration can remove this error.
[4] Gain error drift is a span drift. To calculate full-scale error drift, add the offset error drift to the gain error drift times the full-scale input.
[5] In general terms, the bipolar input voltage range to the primary ADC is given by the ADC range = ±(V_{REF} 2^{RN})/1.25, where: V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected. RN = decimal equivalent of RN2, RN1, RN0. For example, if V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0, respectively, then the ADC range = ±1.28 V. In unipolar mode, the effective range is 0 V to 1.28 V in this example.
[6] 1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0/XREF1 or AXREF bits in ADC0CON2 and ADC1CON, respectively. (AXREF is available only on the ADuC845.)
[7] In bipolar mode, the auxiliary ADC can be driven only to a minimum of AGND – 30 mV as indicated by the auxiliary ADC absolute AIN voltage limits. The bipolar range is still –V_{REF} to +V_{REF}.
[8] DAC linearity and ac specifications are calculated using a reduced code range of 48 to 4095, 0 V to V_{REF}, reduced code range of 100 to 3950, 0 V to V_{DD}.
[9] Endurance is qualified to 100 kcycle per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, +85°C, and +125°C. Typical endurance at 25°C is 700 kcycles.
[10] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.
[11] Power supply current consumption is measured in normal mode following the power-on sequence, and in power-down modes under the following conditions: Normal mode: reset = 0.4 V, digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, core executing internal software loop. Power-down mode: reset = 0.4 V, all P0 pins and P1.2 to P1.7 pins = 0.4 V. All other digital I/O pins are open circuit, core Clk changed via CD bits in PLLCON, PCON.1 = 1, core execution suspended in power-down mode, OSC turned on or off via OSC_PD bit (PLLCON.7) in PLLCON SFR.
[12] DV_{DD} power supply current increases typically by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

General Notes about Specifications

- DAC gain error is a measure of the span error of the DAC.
- The ADuC845BCP, ADuC847BCP, and ADuC848BCP (LFCSP package) have been qualified and tested with the base of the LFCSP package floating. The base of the LFCSP package should be soldered to the board, but left floating electrically, to ensure good mechanical stability.
- Flash/EE memory reliability characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

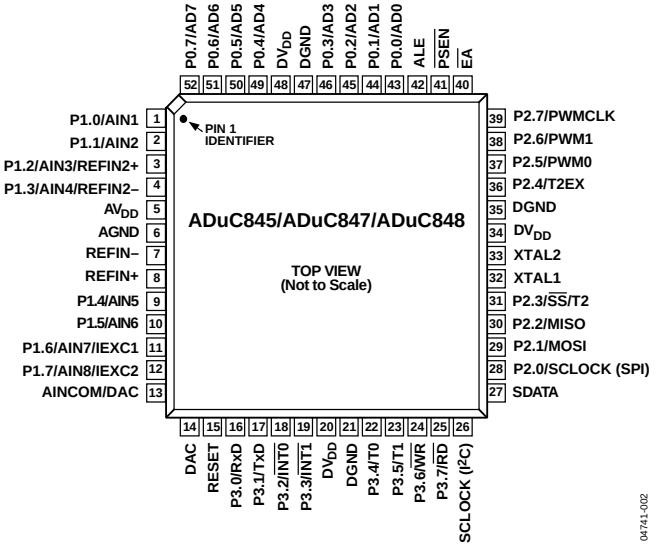

Figure 2. 52-Lead MQFP Pin Configuration

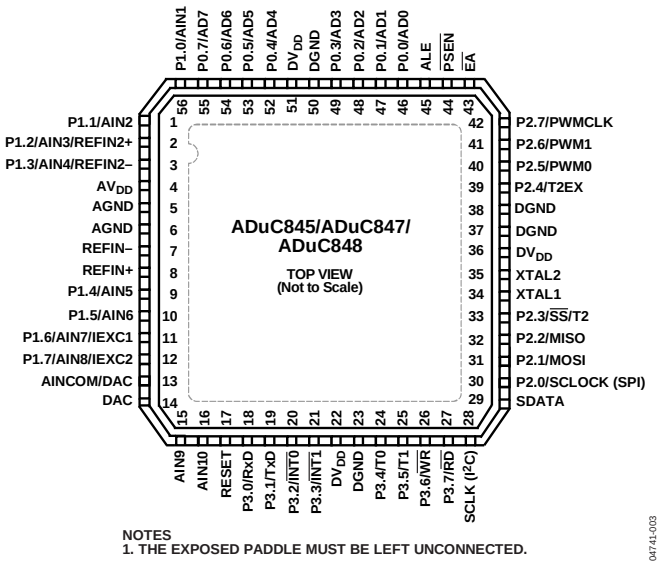

Figure 3. 56-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.				
52-MQFP	**56-LFCSP**	**Mnemonic**	**Type[1]**	**Description**
1	56	P1.0/AIN1	I	By power-on default, P1.0/AIN1 is configured as the AIN1 analog input. AIN1 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN2. P1.0 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
2	1	P1.1/AIN2	I	On power-on default, P1.1/AIN2 is configured as the AIN2 analog input. AIN2 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN1. P1.1 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally.
3	2	P1.2/AIN3/REFIN2+	I	On power-on default, P1.2/AIN3 is configured as the AIN3 analog input. AIN3 can be used as a pseudo differential input when used with AINCOM or as the positive input of a fully differential pair when used with AIN4. P1.2 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, positive terminal.
4	3	P1.3/AIN4/REFIN2–	I	On power-on default, P1.3/AIN4 is configured as the AIN4 analog input. AIN4 can be used as a pseudo differential input when used with AINCOM or as the negative input of a fully differential pair when used with AIN3. P1.3 has no digital output driver. It can function as a digital input for which 0 must be written to the port bit. As a digital input, this pin must be driven high or low externally. This pin also functions as a second external differential reference input, negative terminal.
5	4	AV_{DD}	S	Analog Supply Voltage.
6	5	AGND	S	Analog Ground.
Not applicable	6	AGND	S	A second analog ground is provided with the LFCSP version only.
7	7	REFIN–	I	External Differential Reference Input, Negative Terminal.
8	8	REFIN+	I	External Differential Reference Input, Positive Terminal.

Mnemonic	Description	Bytes	Cycles[1]
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A,Rn	Move register to A	1	1
MOV A,@Ri	Move indirect memory to A	1	2
MOV Rn,A	Move A to register	1	1
MOV @Ri,A	Move A to indirect memory	1	2
MOV A,dir	Move direct byte to A	2	2
MOV A,#data	Move immediate to A	2	2
MOV Rn,#data	Move register to immediate	2	2
MOV dir,A	Move A to direct byte	2	2
MOV Rn, dir	Move register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri,#data	Move immediate to indirect memory	2	2
MOV dir,@Ri	Move indirect to direct memory	2	2
MOV @Ri,dir	Move direct to indirect memory	2	2
MOV dir,dir	Move direct byte to direct byte	3	3
MOV dir,#data	Move immediate to direct byte	3	3
MOV DPTR,#data	Move immediate to data pointer	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A,@A+PC	Move code byte relative PC to A	1	4
MOVX[2] A,@Ri	Move external (A8) data to A	1	4
MOVX[2] A,@DPTR	Move external (A16) data to A	1	4
MOVX[2] @Ri,A	Move A to external data (A8)	1	4
MOVX[2] @DPTR,A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A,Rn	Exchange A and register	1	1
XCH A,@Ri	Exchange A and indirect memory	1	2
XCHD A,@Ri	Exchange A and indirect memory nibble	1	2
XCH A,dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit and carry	2	2
ANL C,/bit	AND direct bit inverse to carry	2	2
ORL C,bit	OR direct bit and carry	2	2
ORL C,/bit	OR direct bit inverse to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3

Power Control Register (PCON)

The PCON SFR contains bits for power-saving options and general-purpose status flags as listed in Table 6.

SFR Address: 87H
Power-On Default: 00H
Bit Addressable: No

Table 6. PCON SFR Bit Designations

Bit No.	Name	Description
7	SMOD	Double UART Baud Rate. 0 = Normal, 1 = Double Baud Rate.
6	SERIPD	Serial Power-Down Interrupt Enable. If this bit is set, a serial interrupt from either SPI or I^2C can terminate the power-down mode.
5	INT0PD	INT0 Power-Down Interrupt Enable. If this bit is set, either a level ($\overline{IT0}$ = 0) or a negative-going transition ($\overline{IT0}$ = 1) on the INT0 pin terminates power-down mode.
4	ALEOFF	If set to 1, the ALE output is disabled.
3	GF1	General-Purpose Flag Bit.
2	GF0	General-Purpose Flag Bit.
1	PD	Power-Down Mode Enable. If set to 1, the device enters power-down mode.
0	-----	Not Implemented. Write Don't Care.

ADuC845/ADuC847/ADuC848 Configuration Register (CFG845/CFG847/CFG848)

The CFG845/CFG847/CFG848 SFR contains the bits necessary to configure the internal XRAM and the extended SP. By default, it configures the user into 8051 mode, that is, extended SP, and the internal XRAM are disabled. When using in a program, use the device name only, that is, CFG845, CFG847, or CFG848.

SFR Address: AFH
Power-On Default: 00H
Bit Addressable: No

Table 7. CFG845/CFG847/CFG848 SFR Bit Designations

Bit No.	Name	Description
7	EXSP	Extended SP Enable. If this bit is set to 1, the stack rolls over from SPH/SP = 00FFH to 0100H. If this bit is cleared to 0, SPH SFR is disabled and the stack rolls over from SP = FFH to SP = 00H.
6	----	Not Implemented. Write Don't Care.
5	----	Not Implemented. Write Don't Care.
4	----	Not Implemented. Write Don't Care.
3	----	Not Implemented. Write Don't Care.
2	----	Not Implemented. Write Don't Care.
1	----	Not Implemented. Write Don't Care.
0	XRAMEN	If this bit is set to 1, the internal XRAM is mapped into the lower 2 kbytes of the external address space. If this bit is cleared to 0, the internal XRAM is accessible and up to 16 MB of external data memory become available. See Figure 8.

Signal Chain Overview with Chop Disabled ($\overline{CHOP}$ = 1)

With $\overline{CHOP}$ = 1, chop is disabled and the available output rates vary from 16.06 Hz to 1.365 kHz. The range of applicable SF words is from 3 to 255. When switching between channels with chop disabled, the channel throughput rate is higher than when chop is enabled. The drawback with chop disabled is that the drift performance is degraded and offset calibration is required following a gain range change or significant temperature change. A block diagram of the ADC input channel with chop disabled is shown in Figure 15.

The signal chain includes a multiplex or buffer, PGA, Σ-Δ modulator, and digital filter. The modulator bit stream is applied to a Sinc^3 filter. Programming the Sinc^3 decimation factor is restricted to an 8-bit register SF; the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) is therefore

$$f_{ADC} = \frac{1}{8 \times SF} \times f_{MOD}$$

where:
f_{ADC} is the ADC conversion rate.
SF is the decimal equivalent of the word loaded to the filter register, valid range is from 3 to 255.
f_{MOD} is the modulator sampling rate of 32.768 kHz.

The settling time to a step input is governed by the digital filter. A synchronized step change requires a settling time of three times the programmed update rate; a channel change can be treated as a synchronized step change. This is one conversion longer than the case for chop enabled. However, because the ADC throughput is three times faster with chop disabled than it is with chop enabled, the actual time to a settled ADC output is significantly less also. This means that following a synchronized step change, the ADC requires three conversions (note: data is not output following a synchronized ADC change until data has settled) before the result accurately reflects the new input voltage.

$$t_{SETTLE} = \frac{3}{f_{ADC}} = 3 \times t_{ADC}$$

An unsynchronized step change requires four conversions to accurately reflect the new analog input at its output. Note that with an unsynchronized change the ADC continues to output data and so the user must take unsettled outputs into account. Again, this is one conversion longer than with chop enabled, but because the ADC throughput with chop disabled is faster than with chop enabled, the actual time taken to obtain a settled ADC output is less.

The allowable range for SF is 3 to 255 with a default of 69 (45H). The corresponding conversion rates, rms, and peak-to-peak noise performances are shown in Table 14, Table 15, Table 16, and Table 17. Note that the conversion time increases by 0.244 ms for each increment in SF.

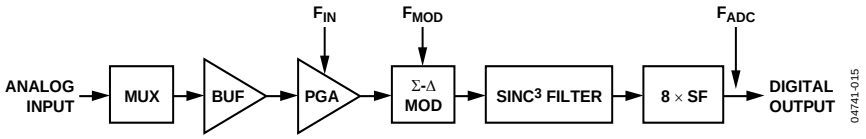

Figure 15. Block Diagram of ADC Input Channel with Chop Disabled

ADC Noise Performance with Chop Disabled ($\overline{CHOP}$ = 1)

Table 14 through Table 17 show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for some typical output update rates. The numbers are typical and are generated at a differential input voltage of 0 V and a common-mode voltage of 2.5 V. The output update rate is selected via the SF7 to SF0 bits in the SF filter register. Note that the peak-to-peak resolution figures represent the resolution for which there is no code flicker within a 6-sigma limit.

The output noise comes from two sources. The first source is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second source is quantization noise, which is added when the analog input is converted to the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is based on half the signal range, which effectively means losing 1 bit of resolution. Typically, the performance of the ADC with chop disabled shows a 0.5 LSB degradation over the performance with chop enabled.

Table 14. ADuC845 and ADuC847 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
68	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 15. ADuC845 and ADuC847 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	17	17	17.5	18
82	49.95	13	14	15	16	16.5	17.5	18	18
255	16.06	13.5	14.5	15.5	16.5	17.5	18.5	18.5	19

Table 16. ADuC848 Typical Output RMS Noise (μV) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
3	1365.33	30.64	24.5	56.18	100.47	248.39	468.65	774.36	1739.5
13	315.08	2.07	1.95	2.28	3.24	8.22	13.9	20.98	49.26
69	59.36	0.85	0.79	1.01	0.99	0.79	1.29	2.3	3.7
82	49.95	0.83	0.77	0.85	0.77	0.91	1.12	1.59	3.2
255	16.06	0.52	0.58	0.59	0.48	0.52	0.57	1.16	1.68

Table 17. ADuC848 Typical Peak-to-Peak Resolution (Bits) vs. Input Range and Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320mV	±640mV	±1.28 V	±2.56 V
3	1365.33	7.5	9	9	9	9	9	9	9
13	315.08	11.5	12.5	13.5	14	13.5	14	14	14
68	59.36	13	14	14.5	15.5	16	16	16	16
82	49.95	13	14	15	16	16	16	16	16
255	16.06	13.5	14.5	15.5	16	16	16	16	16

AUXILIARY ADC (ADUC845 ONLY)

Table 18. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Enabled

SF Word	Data Update Rate (Hz)	μV
13	105.03	17.46
23	59.36	3.13
27	50.56	4.56
69	19.79	2.66
255	5.35	1.13

Table 19. ADuC845 Typical Peak-to-Peak Resolution (Bits) vs. Update Rate[1] with Chop Enabled

SF Word	Data Update Rate (Hz)	Bits
13	105.03	15.5
23	59.36	18
27	50.56	17.5
69	19.79	18
255	5.35	19.5

[1] ADC converting in bipolar mode.

Table 20. ADuC845 Typical Output RMS Noise (μV) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	μV
3	1365.33	1386.58
13	315.08	34.94
66	62.06	3.2
69	59.36	3.19
81	50.57	3.14
255	16.06	1.71

Table 21. ADuC845 Peak-to-Peak Resolution (Bits) vs. Update Rate with Chop Disabled

SF Word	Data Update Rate (Hz)	Bits
3	1365.33	9
13	315.08	14.5
66	62.06	18
69	59.36	18
81	50.57	18
255	16.06	19

REFERENCE INPUTS

The ADuC845/ADuC847/ADuC848 each have two separate differential reference inputs, REFIN± and REFIN2±. While both references are available for use with the primary ADC, only REFIN± is available for the auxiliary ADC (ADuC845 only). The common-mode range for these differential references is from AGND to AV_{DD}. The nominal external reference voltage is 2.5 V, with the primary and auxiliary (ADuC845 only) reference select bits configured from the ADC0CON2 and ADC1CON (ADuC845 only), respectively.

When an external reference voltage is used, the primary ADC sees this internally as a 2.56 V reference ($V_{REF} \times 1.024$). Therefore, any calculations of LSB size should account for this. For instance, with a 2.5 V external reference connected and using a gain of 1 on a unipolar range (2.56 V), the LSB size is $(2.56/2^{24}) = 152.6$ nV (if using the 24-bit ADC on the ADuC845 or ADuC847). If a bipolar gain of 4 is used (±640 mV), the LSB size is $(±640 \text{ mV})/2^{24}) = 76.3$ nV (again using the 24-bit ADC on the ADuC845 or ADuC847).

The ADuC845/ADuC847/ADuC848 can also be configured to use the on-chip band gap reference via the XREF0/1 bits in the ADC0CON2 SFR (for primary ADC) or the AXREF bit in ADC1CON (for auxiliary ADC (ADuC845 only)). In this mode of operation, the ADC sees the internal reference of 1.25 V, thereby halving all the input ranges. A consequence of using the internal band gap reference is a noticeable degradation in peak-to-peak resolution. For this reason, operation with an external reference is recommended.

In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference inputs for the device, the effect of any low frequency noise in the excitation source is removed because the application is ratiometric. If the devices are not used in a ratiometric configuration, use a low noise reference. Recommended reference voltage sources for the ADuC845/ADuC847/ADuC848 include the ADR421, REF43, and REF192.

The reference inputs provide a high impedance, dynamic load to external connections. Because the impedance of each reference input is dynamic, resistor/capacitor combinations on these pins can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources, such as those mentioned above, for example, the ADR421, typically have low output impedances, and, therefore, decoupling capacitors on the REFIN± or REFIN2± inputs would be recommended (typically 0.1 μF). Deriving the reference voltage from an external resistor configuration means that the reference input sees a significant external source impedance. External decoupling of the REFIN± and/or REFIN2± inputs is not recommended in this type of configuration.

BURNOUT CURRENT SOURCES

The primary ADC on the ADuC845 and the ADC on the ADuC847 and ADuC848 incorporate two 100 nA constant current generators that are used to detect a failure in a connected sensor. One sources current from the AV_{DD} to AIN(+), and one sinks current from AIN(−) to AGND. These currents are only configurable for use on AIN5/AIN6 and/or AIN7/AIN8 in differential mode only, from the ICON.6 bit in the ICON SFR

that the internal calibration procedure for full-scale calibration automatically selects the reference in voltage at PGA = 1.

Therefore, the full-scale endpoint calibration automatically subtracts the offset calibration error, it is advisable to perform an offset calibration at the same gain range as that used for full-scale calibration. There is no penalty to the full-scale calibration in redoing the zero-scale calibration at the required PGA range because the full-scale calibration has very good matching at all the PGA ranges.

This procedure also applies when chop is disabled.

Note that for internal calibration to be effective, the AIN− pin should be held at a steady voltage, within the allowable common-mode range to keep it from floating during calibration.

System Calibration Example

With chop enabled, a system zero-scale or offset calibration should never be required. However, if a full-scale or gain calibration is required for any reason, use the following typical procedure for doing so.

1. Apply a differential voltage of 0 V to the selected analog inputs (AIN+ to AIN−) that are held at a common-mode voltage.

   Perform a system zero-scale or offset calibration by setting the MD2...0 bits in the ADCMODE register to 110B.

2. Apply a full-scale differential voltage across the ADC inputs again at the same common-mode voltage.

   Perform a system full-scale or gain calibration by setting the MD2...0 bits in the ADCMODE register to 111B.

Perform a system calibration at the required PGA range to be used since the ADC scales to the differential voltages that are applied to the ADC during the calibration routines.

In bipolar mode, the zero-scale calibration determines the mid-scale point of the ADC (800000H) or 0 V.

PROGRAMMABLE GAIN AMPLIFIER

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different ranges, which are programmed via the range bits (RN0 to RN2) in the ADC0CON1 register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V and 0 V to 2.56 V, while in bipolar mode the ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±64 0 mV, ±1.28 V, and ±2.56 V. These ranges should appear on the input to the on-chip PGA. The ADC range-matching specification of 2 µV (typical with chop enabled) means that calibration need only be carried out on a single range and need not be repeated when the ADC range is changed. This is a significant advantage compared to similar mixed-signal solutions available on the market. The auxiliary (ADuC845 only) ADC does not incorporate a PGA, and the gain is fixed at 0 V to 2.50 V in unipolar mode, and ±2.50 V in bipolar mode.

BIPOLAR/UNIPOLAR CONFIGURATION

The analog inputs of the ADuC845/ADuC847/ADuC848 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the device can handle negative voltages with respect to system AGND, but rather with respect to the negative reference input. Unipolar and bipolar signals on the AIN(+) input on the ADC are referenced to the voltage on the respective AIN(−) input. AIN(+) and AIN(−) refer to the signals seen by the ADC.

For example, if AIN(−) is biased to 2.5 V (tied to the external reference voltage) and the ADC is configured for a unipolar analog input range of 0 mV to >20 mV, the input voltage range on AIN(+) is 2.5 V to 2.52 V. On the other hand, if AIN(−) is biased to 2.5 V (again the external reference voltage) and the ADC is configured for a bipolar analog input range of ±1.28 V, the analog input range on the AIN(+) is 1.22 V to 3.78 V, that is, 2.5 V ± 1.28 V.

The modes of operation for the ADC are fully differential mode or pseudo differential mode. In fully differential mode, AIN1 to AIN2 are one differential pair, and AIN3 to AIN4 are another pair (AIN5 to AIN6, AIN7 to AIN8, and AIN9 to AIN10 are the others). In differential mode, all AIN(−) pin names imply the negative analog input of the selected differential pair, that is, AIN2, AIN4, AIN6, AIN8, AIN10. The term AIN(+) implies the positive input of the selected differential pair, that is, AIN1, AIN3, AIN5, AIN7, AIN9. In pseudo differential mode, each analog input is paired with the AINCOM pin, which can be biased up or tied to AGND. In this mode, the AIN(−) implies AINCOM, and AIN(+) implies any one of the ten analog input channels.

The configuration of the inputs (unipolar vs. bipolar) is shown in Figure 17.

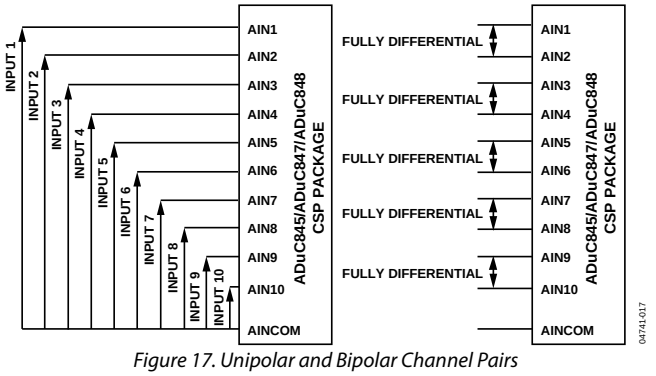

Figure 17. Unipolar and Bipolar Channel Pairs

SF (ADC SINC FILTER CONTROL REGISTER)

The SF register is used to configure the decimation factor for the ADC, and therefore, has a direct influence on the ADC throughput rate.

SFR Address: D4H
Power-On Default: 45H
Bit Addressable: No

Table 28. Sinc Filter SFR Bit Designations

SF.7	SF.6	SF.5	SF.4	SF.3	SF.2	SF.1	SF.0
0	1	0	0	0	1	0	1

The bits in this register set the decimation factor of the ADC. This has a direct bearing on the throughput rate of the ADC along with the chop setting. The equations used to determine the ADC throughput rate are

$$Fadc\ (Chop\ On) = \frac{1}{3 \times 8 \times SFword} \times 32.768\ \text{kHz}$$

where *SFword* is in decimal.

$$Fadc\ (Chop\ Off) = \frac{1}{8 \times SFword} \times 32.768\ \text{kHz}$$

where *SFword* is in decimal.

Table 29. SF SFR Bit Examples

Chop Enabled (ADCMODE.3 = 0)

SF (Decimal)	SF (Hexadecimal)	Fadc (Hz)	Tadc (ms)	Tsettle (ms)
13[1]	0D	105.3	9.52	19.04
69	45	19.79	50.53	101.1
82	52	16.65	60.06	120.1
255	FF	5.35	186.77	373.54

Chop Disabled (ADCMODE.3 = 1)

SF (Decimal)	SF (Hexadecimal)	Fadc (Hz)	Tadc (ms)	Tsettle (ms)
3	03	1365.3	0.73	2.2
69	45	59.36	16.84	50.52
82	52	49.95	20.02	60.06
255	FF	16.06	62.25	186.8

[1] With chop enabled, if an SF word smaller than 13 is written to this SF register, the filter automatically defaults to 13.

During ADC calibration, the user-programmed value of SF word is used. The SF word does not default to the maximum setting (255) as it did on previous MicroConverter® products. However, for optimum calibration results, it is recommended that the maximum SF word be set.

DAC CIRCUIT INFORMATION

The ADuC845/ADuC847/ADuC848 incorporate a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF, and has two selectable ranges, 0 V to V_{REF} and 0 V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register, DACCON, and two data registers, DACH/L. The DAC output can be programmed to appear at Pin 14 (DAC) or Pin 13 (AINCOM).

In 12-bit mode, the DAC voltage output is updated as soon as the DACL data SFR is written; therefore, the DAC data registers should be updated as DACH first, followed by DACL. The 12-bit DAC data should be written into DACH/L right-justified such that DACL contains the lower 8 bits, and the lower nibble of DACH contains the upper 4 bits.

DACCON Control Register

SFR Address: FDH
Power-On Default: 00H
Bit Addressable: No

Table 33. DACCON—DAC Configuration Commands

Bit No.	Name	Description
7	–––	Not Implemented. Write Don't Care.
6	–––	Not Implemented. Write Don't Care.
5	–––	Not Implemented. Write Don't Care.
4	DACPIN	DAC Output Pin Select. Set to 1 by the user to direct the DAC output to Pin 13 (AINCOM). Cleared to 0 by the user to direct the DAC output to Pin 14 (DAC).
3	DAC8	DAC 8-Bit Mode Bit. Set to 1 by the user to enable 8-bit DAC operation. In this mode, the 8 bits in DACL SFR are routed to the 8 MSBs of the DAC, and the 4 LSBs of the DAC are set to 0. Cleared to 0 by the user to enable 12-bit DAC operation. In this mode, the 8 LSBs of the result are routed to DACL, and the upper 4 MSB bits are routed to the lower 4 bits of DACH.
2	DACRN	DAC Output Range Bit. Set to 1 by the user to configure the DAC range of 0 V to AV_{DD}. Cleared to 0 by the user to configure the DAC range of 0 V to 2.5 V (V_{REF}).
1	DACCLR	DAC Clear Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to reset the DAC data registers DACL/H to 0.
0	DACEN	DAC Enable Bit. Set to 1 by the user to enable normal DAC operation. Cleared to 0 by the user to power down the DAC.

DACH/DACL Data Registers

These DAC data registers are written to by the user to update the DAC output.

SFR Address: DACL (DAC data low byte)—FBH
DACH (DAC data high byte)—FCH
Power-On Default: 00H (both registers)
Bit Addressable: No (both registers)

Hardware Slave Mode

After reset, the ADuC845/ADuC847/ADuC848 default to hardware slave mode. Slave mode is enabled by clearing the I2CM bit in I2CCON. The devices have a full hardware slave. In slave mode, the I²C address is stored in the I2CADD register. Data received or to be transmitted is stored in the I2CDAT register.

Once enabled in I²C slave mode, the slave controller waits for a start condition. If the parts detect a valid start condition, followed by a valid address, followed by the R/W bit, then the I2CI interrupt bit is automatically set by hardware. The I²C peripheral generates a core interrupt only if the user has pre-configured the I²C interrupt enable bit in the IEIP2 SFR as well as the global interrupt bit, EA, in the IE SFR. Therefore,

```
MOV IEIP2, #01h    ;Enable I²C Interrupt
SETB EA
```

An autoclear of the I2CI bit is implemented on the devices so that this bit is cleared automatically upon read or write access to the I2CDAT SFR.

```
MOV I2CDAT, A      ;I2CI auto-cleared
MOV A, I2CDAT      ;I2CI auto-cleared
```

If for any reason the user tries to clear the interrupt more than once, that is, access the data SFR more than once per interrupt, the I²C controller stops. The interface then must be reset by using the I2CRS bit.

The user can choose to poll the I2CI bit or to enable the interrupt. In the case of the interrupt, the PC counter vectors to 003BH at the end of each complete byte. For the first byte, when the user gets to the I2CI ISR, the 7-bit address and the R/W bit appear in the I2CDAT SFR.

The I2CTX bit contains the R/W bit sent from the master. If I2CTX is set, the master is ready to receive a byte; therefore the slave transmits data by writing to the I2CDAT register. If I2CTX is cleared, the master is ready to transmit a byte; therefore the slave receives a serial byte. Software can interrogate the state of I2CTX to determine whether it should write to or read from I2CDAT.

Once the device has received a valid address, hardware holds SCLOCK low until the I2CI bit is cleared by software. This allows the master to wait for the slave to be ready before transmitting the clocks for the next byte.

The I2CI interrupt bit is set every time a complete data byte is received or transmitted, provided that it is followed by a valid ACK. If the byte is followed by a NACK, an interrupt is not generated.

The device continues to issue interrupts for each complete data byte transferred until a stop condition is received or the interface is reset.

When a stop condition is received, the interface resets to a state in which it is waiting to be addressed (idle). Similarly, if the interface receives a NACK at the end of a sequence, it also returns to the default idle state. The I2CRS bit can be used to reset the I²C interface. This bit can be used to force the interface back to the default idle state.

SPI SERIAL INTERFACE

The ADuC845/ADuC847/ADuC848 integrate a complete hardware serial peripheral interface (SPI) interface on-chip. SPI is an industry-standard synchronous serial interface that allows 8 bits of data to be synchronously transmitted and received simultaneously, that is, full duplex. Note that the SPI pins are multiplexed with the Port 2 pins, P2.0, P2.1, P2.2, and P2.3. These pins have SPI functionality only if SPE is set. Otherwise, with SPE cleared, standard Port 2 functionality is maintained. SPI can be configured for master or slave operation and typically consists of Pins SCLOCK, MISO, MOSI, and $\overline{SS}$.

SCLOCK (Serial Clock I/O Pin)

Pin 28 (MQFP Package), Pin 30 (LFCSP Package)
The master clock (SCLOCK) is used to synchronize the data transmitted and received through the MOSI and MISO data lines.

A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode, the bit rate, polarity, and phase of the clock are controlled by the CPOL, CPHA, SPR0, and SPR1 bits in the SPICON SFR (see Table 41). In slave mode, the SPICON register must be configured with the same phase and polarity (CPHA and CPOL) as the master. The data is transmitted on one edge of the SCLOCK signal and sampled on the other.

MISO (Master In, Slave Out Pin)

Pin 30 (MQFP Package), Pin 32 (LFCSP Package)
The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

Pin 29 (MQFP Package), Pin31 (LFCSP Package)
The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

TIME INTERVAL COUNTER (TIC)

A TIC is provided on-chip for counting longer intervals than the standard 8051-compatible timers can count. The TIC is capable of timeout intervals ranging from 1/128 second to 255 hours. Also, this counter is clocked by the external 32.768 kHz crystal rather than by the core clock, and it can remain active in power-down mode and time long power-down intervals. This has obvious applications for remote battery-powered sensors where regular widely spaced readings are required. Note that instructions to the TIC SFRs are also clocked at 32.768 kHz, so sufficient time must be allowed in user code for these instructions to execute.

Six SFRs are associated with the time interval counter, TIMECON being its control register. Depending on the configuration of the IT0 and IT1 bits in TIMECON, the selected time counter register overflow clocks the interval counter. When this counter is equal to the time interval value loaded in the INTVAL SFR, the TII bit (TIMECON.2) is set and generates an interrupt, if enabled. If the device is in power-down mode, again with TIC interrupt enabled, the TII bit wakes up the device and resumes code execution by vectoring directly to the TIC interrupt service vector address at 0053H. The TIC-related SFRs are described in Table 45. Note also that the time based SFRs can be written initially with the current time; the TIC can then be controlled and accessed by user software. In effect, this facilitates the implementation of a real-time clock. A basic block diagram of the TIC is shown in Figure 47.

Because the TIC is clocked directly from a 32 kHz external crystal on the devices, instructions that access the TIC registers are also clocked at 32 kHz (not at the core frequency). The user must ensure that sufficient time is given for these instructions to execute.

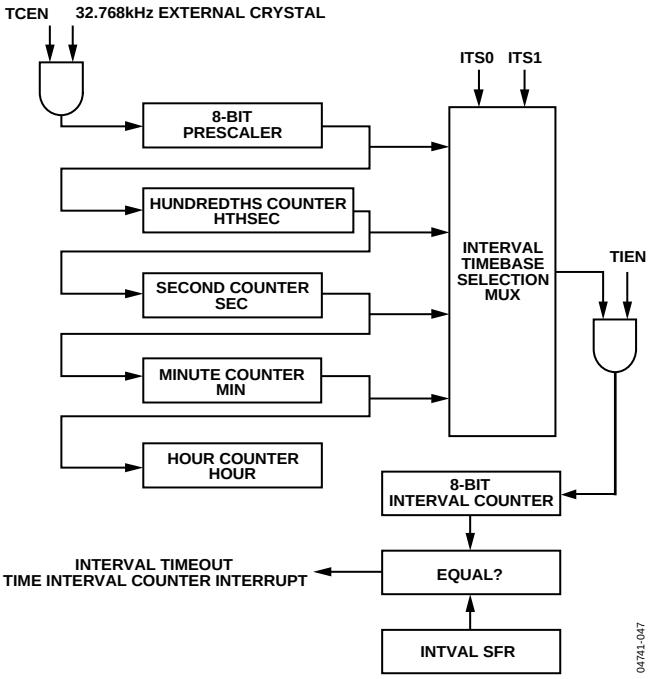

Figure 47. TIC Simplified Block Diagram

Timer/Counter 0 and 1 Operating Modes

This section describes the operating modes for Timer/Counters 0 and 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 52 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single-cycle core.

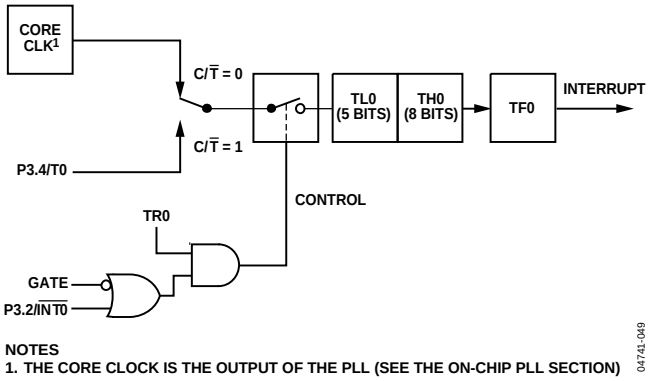

Figure 52. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate = 0 or $\overline{INT0}$ = 1. Setting Gate = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse-width measurements. TR0 is a control bit in the special function register TCON; Gate is in TMOD. The 13-bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 53.

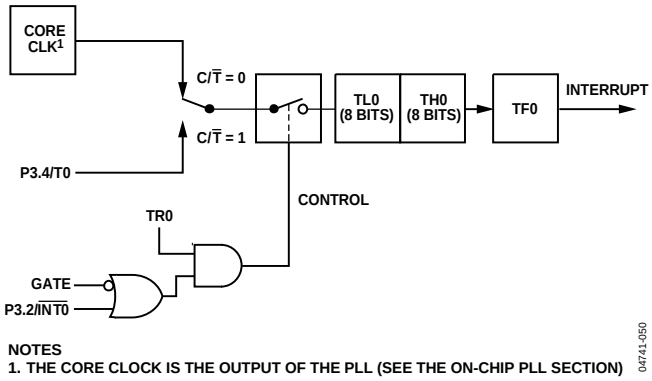

Figure 53. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload as shown in Figure 54. Overflow from TL0 not only sets TF0, but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

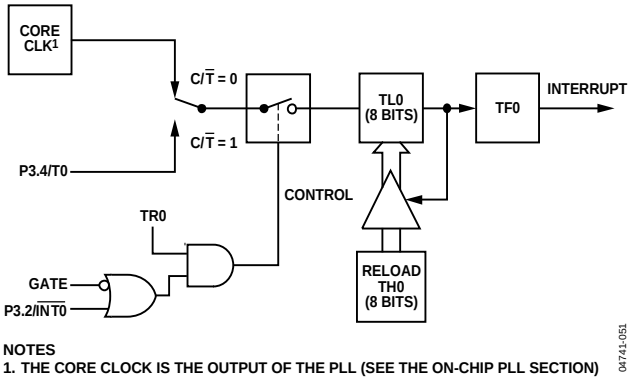

Figure 54. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 55. TL0 uses the Timer 0 Control Bits C/$\overline{T}$, Gate, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 then controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can still be used by the serial interface as a baud rate generator. In fact, it can be used in any application not requiring an interrupt from Timer 1 itself.

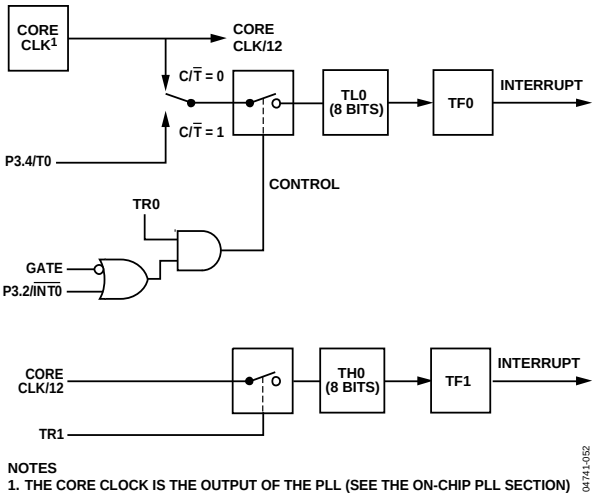

Figure 55. Timer/Counter 0, Mode 3

Timer/Counter 2 Operating Modes

The following sections describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table 53.

Table 53. T2CON Operating Modes

RCLK (or) TCLK	CAP2	TR2	Mode
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	Off

16-Bit Autoreload Mode

Autoreload mode has two options that are selected by bit EXEN2 in T2CON. If EXEN2 = 0, when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX also triggers the 16-bit reload and sets EXF2. Autoreload mode is shown in Figure 56.

16-Bit Capture Mode

Capture mode has two options that are selected by Bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter that, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into Registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes Bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is shown in Figure 57. The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore, Timer 2 interrupts do not occur, so they do not have to be disabled. In this mode, the EXF2 flag can, however, still cause interrupts, which can be used as a third external interrupt. Baud rate generation is described as part of the UART serial port operation in the following section.

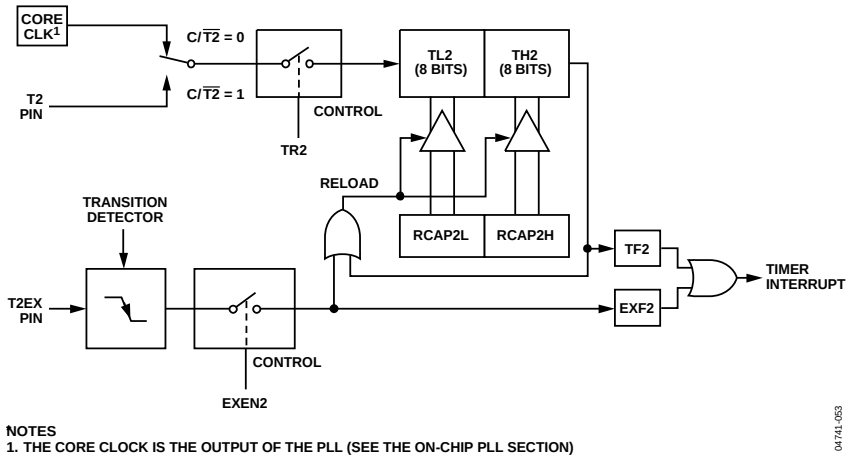

Figure 56. Timer/Counter 2, 16-Bit Autoreload Mode

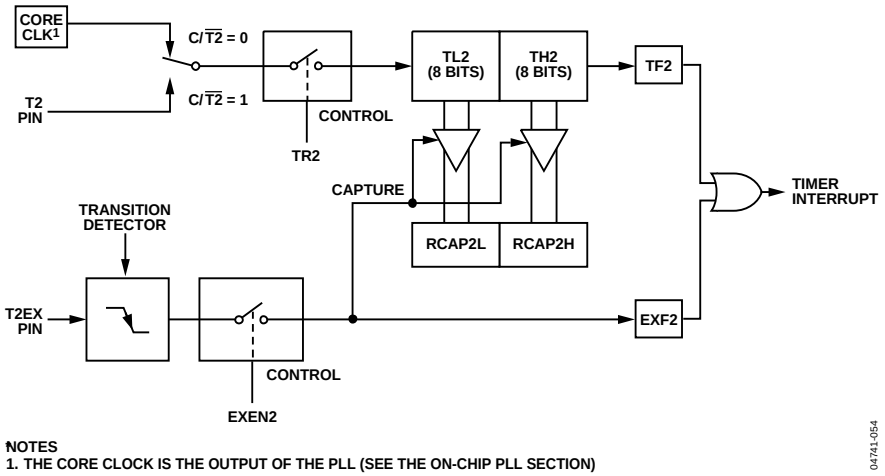

Figure 57. Timer/Counter 2, 16-Bit Capture Mode

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART Serial Port Baud Rate Generation

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed:

$$Mode\ 0\ Baud\ Rate = \left(\frac{CoreClockFrequency}{12}\right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock:

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Core\ Clock\ Frequency$$

Modes 1 and 3 Baud Rate Generation

The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or in both (one for transmit and the other for receive).

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, and in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{CoreClockFrequency}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{1}{16} \times Timer\ 2\ Overflow\ Rate$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible.

Timer 2 is selected as the baud rate generator by setting the TCLK and/or RCLK in T2CON. The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode as shown in Figure 60.

In this case, the baud rate is given by the formula

$$Modes\ 1\ and\ 3\ Baud\ Rate = \frac{Core\ \ Clock\ \ Frequency}{(16 \times [65536\ - (RCAP\ 2H\ :RCAP\ 2L)])}$$

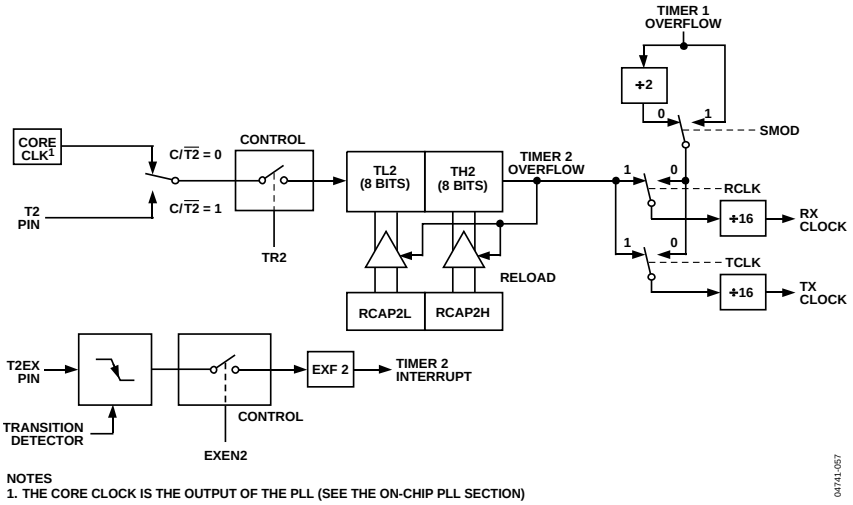

Figure 60. Timer 2, UART Baud Rates

as op amps and voltage reference) can be powered from the AV_{DD} supply line as well.

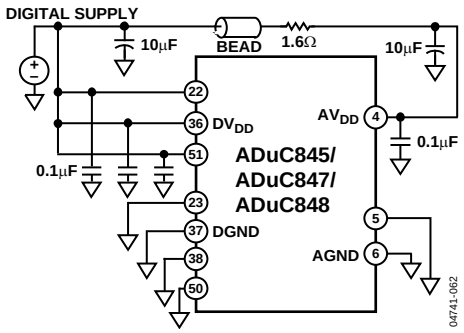

Figure 65. External Single-Supply Connections (56-Lead LFCSP Pin Numbering)

Notice that in both Figure 64 and Figure 65 a large value (10 µF) reservoir capacitor sits on DV_{DD} and a separate 10 µF capacitor sits on AV_{DD}. Also, local decoupling capacitors (0.1 µF) are located at each V_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are closer than the 10 µF capacitors to each V_{DD} pin with lead lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane. Finally, note that, at all times, the analog and digital ground pins on the device must be referenced to the same system ground reference point. It is recommended that the LFCSP paddle be soldered to ensure mechanical stability but be floated with respect to system V_{DD}s or grounds.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC845/ADuC847/ADuC848.

3 V Part

For DV_{DD} below 2.63 V, the internal POR holds the device in reset. As DV_{DD} rises above 2.63 V, an internal timer times out for typically 128 ms before the device is released from reset. The user must ensure that the power supply has at least reached a stable 2.7 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 66 illustrates the operation of the internal POR.

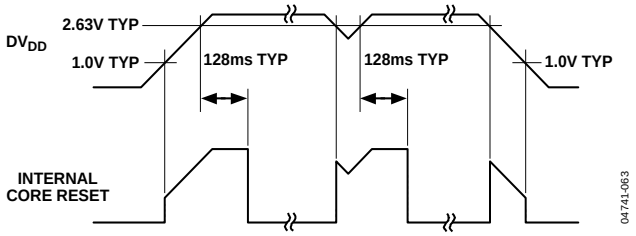

Figure 66. 3 V Part POR operation

5 V Part

For DV_{DD} below 4.5 V, the internal POR holds the device in reset. As DV_{DD} rises above 4.5 V, an internal timer times out for approximately 128 ms before the device is released from reset. The user must ensure that the power supply has reached a stable 4.75 V minimum level by this time. Likewise on power-down, the internal POR holds the device in reset until the power supply drops below 1 V. Figure 67 illustrates this operation.

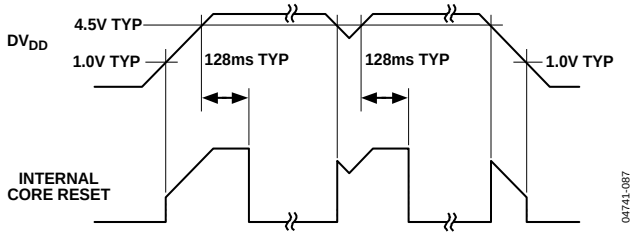

Figure 67. 5 V Part POR Operation

POWER CONSUMPTION

The DV_{DD} power supply current consumption is specified in normal and power-down modes. The AV_{DD} power supply current is specified with the analog peripherals disabled. The normal mode power consumption represents the current drawn from DV_{DD} by the digital core. The other on-chip peripherals (such as the watchdog timer and power supply monitor) consume negligible current and are therefore included with the normal operating current. The user must add any currents sourced by the parallel and serial I/O pins, and those sourced by the DAC to determine the total current needed at the ADuC845/ADuC847/ADuC848 DV_{DD} and AV_{DD} supply pins. Also, current drawn from the DV_{DD} supply increases by approximately 5 mA during Flash/EE erase and program cycles.

POWER-SAVING MODES

Setting the power-down mode bit, PCON.1, in the PCON SFR described in Table 6, allows the chip to be switched from normal mode into full power-down mode.

In power-down mode, both the PLL and the clock to the core are stopped. The on-chip oscillator can be halted or can continue to oscillate, depending on the state of the oscillator power-down bit (OSC_PD) in the PLLCON SFR. The TIC, driven directly from the oscillator, can also be enabled during power-down. However, all other on-chip peripherals are shut down. Port pins retain their logic levels in this mode, but the DAC output goes to a high impedance state (three-state) while ALE and $\overline{PSEN}$ outputs are held low. There are five ways to terminate power-down mode:

- **Asserting the RESET Pin**
  Returns to normal mode. All registers are set to their reset default value and program execution starts at the reset vector once the RESET pin is de-asserted.

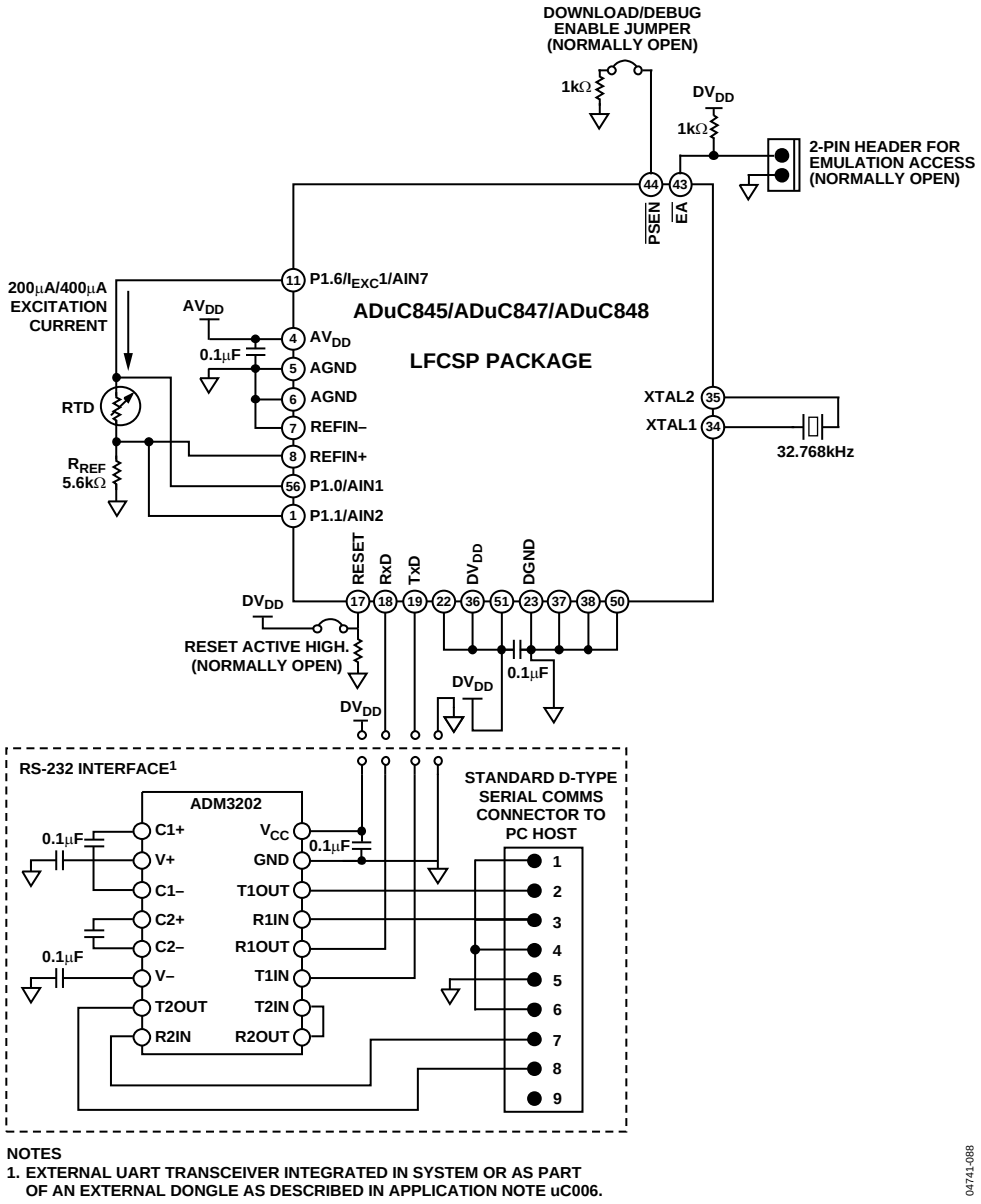

Figure 70. UART Connectivity in Typical System

In addition to the basic UART connections, users also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 70. To get the devices into download mode, connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available), and it is ready to receive a new program serially. With the jumper removed, the device powers on in normal mode (and runs the program) whenever power is cycled or RESET is toggled. Note that $\overline{\text{PSEN}}$ is normally an output and that it is sampled as an input only on the falling edge of RESET, that is, at power-on or upon an external manual reset. Note also that if any external circuitry unintentionally pulls $\overline{\text{PSEN}}$ low during power-on or reset events, it may cause the chip to enter download mode and fail to begin user code execution. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself or the method of download entry in use during a reset or power-cycle condition.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described previously. In fact, both serial download and serial port debug modes are essentially one mode of operation used in two different ways.

The serial port debugger is fully contained on the device, unlike ROM monitor type debuggers, and, therefore, no external memory is needed to enable in-system debug sessions.

TIMING SPECIFICATIONS

AC inputs during testing are driven at DV_{DD} – 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements are made at V_{IH} min for Logic 1 and V_{IL} max for Logic 0 as shown in Figure 72.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 72.

C_{LOAD} for all outputs = 80 pF, unless otherwise noted.

AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 64. CLOCK INPUT (External Clock Driven XTAL1) Parameter

		32.768 kHz External Crystal			
		Min	Typ	Max	Unit
t_{CK}	XTAL1 Period		30.52		µs
t_{CKL}	XTAL1 Width Low		6.26		µs
t_{CKH}	XTAL1 Width High		6.26		µs
t_{CKR}	XTAL1 Rise Time		9		ns
t_{CKF}	XTAL1 Fall Time		9		ns
$1/t_{CORE}$	Core Clock Frequency[1]	0.098	1.57	12.58	MHz
t_{CORE}	Core Clock Period[2]		0.636		µs
t_{CYC}	Machine Cycle Time[3]	10.2	0.636	0.08	µs

[1] ADuC845/ADuC847/ADuC848 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 12.58 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.
[2] This number is measured at the default Core_Clk operating frequency of 1.57 MHz.
[3] ADuC845/ADuC847/ADuC848 machine cycle time is nominally defined as 1/Core_Clk.

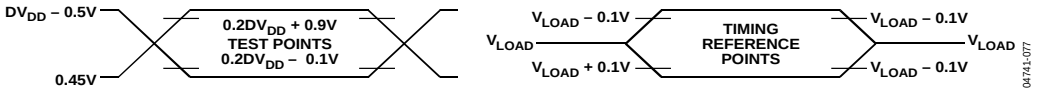

Figure 72. Timing Waveform Characteristics

Table 65. EXTERNAL DATA MEMORY READ CYCLE Parameter

		12.58 MHz Core Clock		6.29 MHz Core Clock		
		Min	Max	Min	Max	Unit
t_{RLRH}	$\overline{RD}$ Pulse Width	60		125		ns
t_{AVLL}	Address Valid After ALE Low	60		120		ns
t_{LLAX}	Address Hold After ALE Low	145		290		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		48		100	ns
t_{RHDX}	Data and Address Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		150		625	ns
t_{LLDV}	ALE Low to Valid Data In		170		350	ns
t_{AVDV}	Address to Valid Data In		230		470	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	130		255		ns
t_{AVWL}	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	190		375		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		15		35	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	60		120		ns

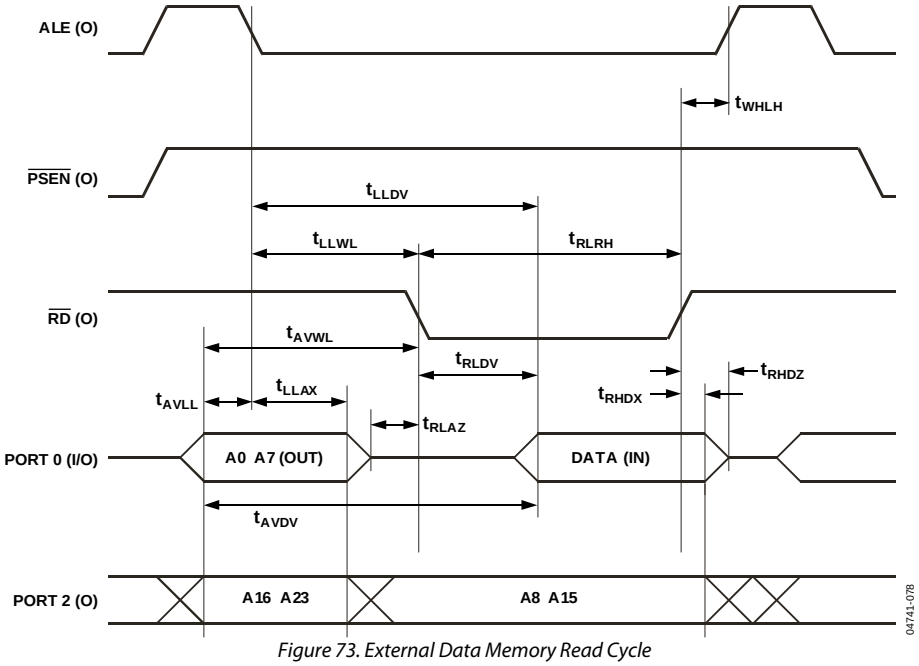

Figure 73. External Data Memory Read Cycle

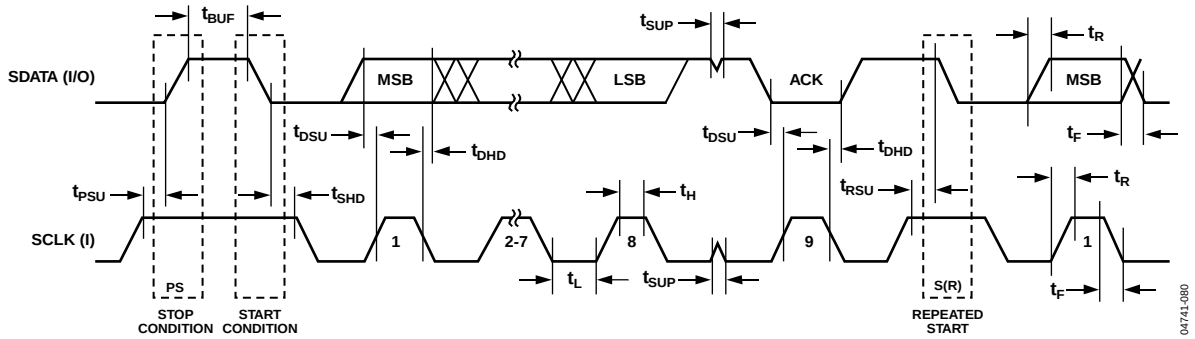

Figure 75. I²C-Compatible Interface Timing