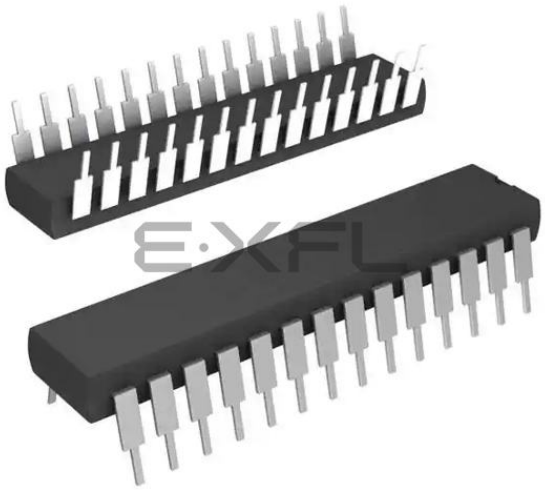

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0880pj020eg

Revision History

Each instance in the Revision History table below reflects a change to this document from its previous version. For more details, click the appropriate links in the table.

Date	Revision Level	Description	Page
Dec 2012	15	Added Timer Clock Source footnote to the TxCTS2 Register.	117
Nov 2012	14	In the Multi-Channel Timer chapter, corrected/ clarified instances of the TInA–TInD and TOutA–TOutD to T4CHA–T4CHD GPIO pins to more accurately address their relationship to T_{IN}.	120
Oct 2011	13	Revised Flash Sector Protect Register descriptions per CR 13212; revised Packaging chapter.	274, 371
May 2011	12	Correction to Trim Bit Address 0001H Register per CR 13091.	283
Oct 2010	11	Comparator 1 Control Register (CMP1) address formerly showed F90H; now corrected to F91H.	258
Sep 2010	10	Removed references to LSBF bit in Master-In/Slave-Out, Master-Out/Slave-In and SPI Master Operation sections.	199, 207
Aug 2010	09	Changed the frequency for the Internal Precision RC Oscillator from 1.3842 to 1.3824 in Table 168 per CR 12961.	316
Jun 2008	08	Updated Trim Option Bits at 0005H (TVREF).	287
Mar 2008	07	Updated Operation of the On-Chip Debugger Interface and Ordering Information sections. Added Target OCD Connector Interface.	296

The first 7 bits transmitted in the first byte are 11110XX. The 2 XX bits are the two most significant bits of the 10-bit address. The lowest bit of the first byte transferred is the Read/Write control bit (which is cleared to 0). The transmit operation is performed in the same manner as 7-bit addressing.

Observe the following steps for a master transmit operation to a 10-bit addressed slave:

1. The software initializes the MODE field in the I^2C Mode Register for MASTER/SLAVE Mode with 7- or 10-bit addressing (the I^2C bus protocol allows the mixing of slave address types). The MODE field selects the address width for this mode when addressed as a slave (but not for the remote slave). The software asserts the IEN bit in the I^2C Control Register.
2. The software asserts the TXI bit of the I^2C Control Register to enable transmit interrupts.
3. The I^2C interrupt asserts because the I^2C Data Register is empty.
4. The software responds to the TDRE interrupt by writing the first Slave Address byte (11110xx0). The least-significant bit must be 0 for the write operation.
5. The software asserts the start bit of the I^2C Control Register.
6. The I^2C controller sends a start condition to the I^2C Slave.
7. The I^2C controller loads the I^2C Shift Register with the contents of the I^2C Data Register.
8. After one bit of the address is shifted out by the SDA signal, the transmit interrupt asserts.
9. The software responds by writing the second byte of address into the contents of the I^2C Data Register.
10. The I^2C controller shifts the remainder of the first byte of the address and the Write bit out via the SDA signal.
11. The I^2C slave sends an Acknowledge by pulling the SDA signal Low during the next High period of SCL. The I^2C controller sets the ACK bit in the I^2C Status Register.

    If the slave does not acknowledge the first address byte, the I^2C controller sets the NCKI bit in the I^2C Status Register, sets the ACKV bit and clears the ACK bit in the I^2C State Register. The software responds to the Not Acknowledge interrupt by setting the stop bit and clearing the TXI bit. The I^2C controller flushes the second address byte from the Data Register, sends a stop condition on the bus and clears the stop and NCKI bits. The transaction is complete and the following steps can be ignored.
12. The I^2C controller loads the I^2C Shift Register with the contents of the I^2C Data Register (2nd address byte).
13. The I^2C controller shifts the second address byte out via the SDA signal. After the first bit has been sent, the transmit interrupt asserts.