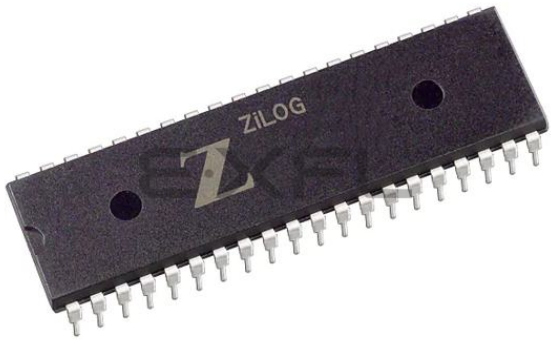
Zilog - Z8F0880PM020EG Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	33
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0880pm020eg

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List of Figures

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)[1]	Page #
F17	Timer 2 Control 1	T2CTL1	00	113
F28	Timer 2 PWM1 High Byte	T2PWM1H	00	111
F29	Timer 2 PWM1 Low Byte	T2PWM1L	00	111
F2A	Timer 2 Control 2	T2CTL2	00	117
F2B	Timer 2 Status	T2STA	00	118
F2E	Timer 2 Noise Filter Control	T2NFC	00	119
F2F–F3F	Reserved	—	XX	
LIN UART 0				
F40	LIN UART0 Transmit Data	U0TXD	XX	163
	LIN UART0 Receive Data	U0RXD	XX	164
F41	LIN UART0 Status 0—Standard UART Mode	U0STAT0	0000011Xb	165
	LIN UART0 Status 0—LIN Mode	U0STAT0	00000110b	166
F42	LIN UART0 Control 0	U0CTL0	00	170
F43	LIN UART0 Control 1—Multiprocessor Control	U0CTL1	00	172
	LIN UART0 Control 1—Noise Filter Control	U0CTL1	00	174
	LIN UART0 Control 1—LIN Control	U0CTL1	00	175
F44	LIN UART0 Mode Select and Status	U0MDSTAT	00	168
F45	UART0 Address Compare	U0ADDR	00	177
F46	UART0 Baud Rate High Byte	U0BRH	FF	177
F47	UART0 Baud Rate Low Byte	U0BRL	FF	178
LIN UART 1				
F48	LIN UART1 Transmit Data	U1TXD	XX	163
	LIN UART1 Receive Data	U1RXD	XX	164
F49	LIN UART1 Status 0—Standard UART Mode	U1STAT0	0000011Xb	165
	LIN UART1 Status 0—LIN Mode	U1STAT0	00000110b	166
F4A	LIN UART1 Control 0	U1CTL0	00	170

Notes:
1. XX=Undefined.
2. The Reserved space can be configured as General-Purpose Register File RAM depending on the user option bits (see the User Option Bits chapter on page 277) and the on-chip PRAM size (see the Ordering Information chapter on page 372). If the PRAM is programmed as General-Purpose Register File RAM on Reserved space, the starting address always begins immediately after the end of General-Purpose Register File RAM.

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)[1]	Page #
Analog-to-Digital Converter (ADC)				
F70	ADC Control 0	ADCCTL0	00	189
F71	ADC Raw Data High Byte	ADCRD_H	80	191
F72	ADC Data High Byte	ADCD_H	XX	191
F73	ADC Data Low Bits	ADCD_L	XX	192
F74	ADC Sample Settling Time	ADCSST	FF	193
F75	Sample Time	ADCST	XX	194
F76	ADC Clock Prescale Register	ADCCP	00	195
F77–F7F	Reserved	—	XX	
Low-Power Control				
F80	Power Control 0	PWRCTL0	80	44
F81	Reserved	—	XX	
LED Controller				
F82	LED Drive Enable	LEDEN	00	66
F83	LED Drive Level High Bit	LEDLVLH	00	67
F84	LED Drive Level Low Bit	LEDLVLL	00	67
F85	Reserved	—	XX	
Oscillator Control				
F86	Oscillator Control 0	OSCCTL0	A0	319
F87	Oscillator Control 1	OSCCTL1	00	320
F88–F8F	Reserved			
Comparator 0				
F90	Comparator 0 Control	CMP0	14	257
Comparator 1				
F91	Comparator 1 Control	CMP1	14	258
F92–F9F	Reserved	—	XX	

Notes:
1. XX=Undefined.
2. The Reserved space can be configured as General-Purpose Register File RAM depending on the user option bits (see the User Option Bits chapter on page 277) and the on-chip PRAM size (see the Ordering Information chapter on page 372). If the PRAM is programmed as General-Purpose Register File RAM on Reserved space, the starting address always begins immediately after the end of General-Purpose Register File RAM.

Table 48. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bits	7	6	5	4	3	2	1	0
Field	Reserved	MCTENL	U1RENL	U1TENL	C3ENL	C2ENL	C1ENL	C0ENL
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC8H							

Bit	Description
[7]	Reserved; must be 0.
[6] MCTENL	Multi-Channel Timer Interrupt Request Enable Low Bit (MCTENL)
[5] U1RENL	UART1 Receive Interrupt Request Enable Low Bit (U1RENL)
[4] U1TENL	UART1 Transmit Interrupt Request Enable Low Bit (U1TENL)
[3] C3ENL	Port C3 Interrupt Request Enable Low Bit (C3ENL)
[2] C2ENL	Port C2 Interrupt Request Enable Low Bit (C2ENL)
[1] C1ENL	Port C1 Interrupt Request Enable Low Bit (C1ENL)
[0] C0ENL	Port C0 Interrupt Request Enable Low Bit (C0ENL)

3. Write to the Timer Control 0 Register to set the timer interrupt configuration field TICONFIG.
4. Write to the Timer High and Low Byte registers to set the starting count value. This value only affects the first pass in COUNTER Mode. After the first timer reload in COUNTER Mode, counting always begins at the reset value of 0001H. Generally, in COUNTER Mode the Timer High and Low Byte registers must be written with the value 0001H.
5. Write to the Timer Reload High and Low Byte registers to set the reload value.
6. If required, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
7. Configure the associated GPIO port pin for the Timer Input alternate function.
8. When using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
9. Write to the Timer Control 1 Register to enable the timer.

In COUNTER Mode, the number of Timer Input transitions since the timer start is calculated using the following equation:

COUNTER Mode Timer Input Transitions = Current Count Value - Start Value

9.2.3.5. COMPARATOR COUNTER Mode

In COMPARATOR COUNTER Mode, the timer counts output transitions from an analog comparator output. The assignment of a comparator to a timer is based on the TIMTRG bits in the CMP0 and CMP1 registers. The TPOL bit in the Timer Control 1 Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPARATOR COUNTER Mode, the prescaler is disabled.

! Caution: The frequency of the comparator output signal must not exceed one-fourth the timer clock frequency.

Upon reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or High to Low) at timer reload.

Observe the following steps to configure a timer for COMPARATOR COUNTER Mode and initiate the count:

Table 60. Timer 0–2 PWM0 Low Byte Register (TxPWM0L)

Bit	7	6	5	4	3	2	1	0
Field	PWM0L							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H, F0DH, F15H							

Bit	Description
[7:0] PWM0H, PWM0L	**Pulse Width Modulator 0 High and Low Bytes** These two bytes, {PWM0H[7:0], PWM0L[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control 1 Register (TxCTL1). The TxPWM0H and TxPWM0L registers also store the 16-bit captured timer value when operating in CAPTURE, CAPTURE/COMPARE and DEMODULATION Modes.

9.3.4. Timer 0–2 PWM1 High and Low Byte Registers

The Timer 0–2 PWM1 High and Low Byte (TxPWM1H and TxPWM1L) registers, shown in Tables 61 and 62, store Capture values for DEMODULATION Mode.

Table 61. Timer 0-2 PWM1 High Byte Register (TxPWM1H)

Bit	7	6	5	4	3	2	1	0
Field	PWM1H							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F20H, F24H, F28H							

Table 62. Timer 0–2 PWM1 Low Byte Register (TxPWM1L)

Bit	7	6	5	4	3	2	1	0
Field	PWM1L							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F21H, F25H, F29H							

Bit	Description
[7:0] PWM1H, PWM1L	**Pulse Width Modulator 1 High and Low Bytes** These two bytes, {PWM1H[7:0], PWM1L[7:0]}, store the 16-bit captured timer value for DEMODULATION Mode.

12.3.4. LIN-UART Mode Select and Status Register

The LIN-UART Mode Select and Status Register, shown in Table 87, contains mode select and status bits.

Table 87. LIN-UART Mode Select and Status Register (U0MDSTAT = F44H)

Bit	7	6	5	4	3	2	1	0
Field	MSEL			MODE STATUS				
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R	R	R
Address	F44H, F4CH							

Note: R = Read; R/W = Read/Write.

Bit	Description
[7:5] MSEL	**Mode Select** This read/write field determines which control register is accessed when performing a write or read to the UART Control 1 Register address. This field also determines which status is returned in the Mode Status field when reading this register. 000 = Multiprocessor and normal UART control/status 001 = Noise filter control/status 010 = LIN protocol control/status 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = LIN-UART hardware revision (allows hardware revision to be read in the Mode Status field.
[4:0]	**Mode Status** This read-only field returns status corresponding to one of four modes selected by MSEL. These four modes are described in Table 88 on page 169. MSEL[2:0]=000, MULTIPROCESSOR Mode status = {0,0,0,NEWFRM, MPRX} MSEL[2:0]=001, Noise filter status = {NE,0,0,0,0} MSEL[2:0]=010, LIN mode status = {NE, RxBreakLength} MSEL[2:0]=011, Reserved; must be 00000 MSEL[2:0]=100, Reserved; must be 00000 MSEL[2:0]=101, Reserved; must be 00000 MSEL[2:0]=110, Reserved; must be 00000 MSEL[2:0]=111, LIN-UART hardware revision

14.3.5. Sample Settling Time Register

The Sample Settling Time Register, shown in Table 105, is used to program the length of time from the SAMPLE/HOLD signal to the start signal, when the conversion can begin. The number of clock cycles required for settling will vary from system to system depending on the system clock period used. The system designer should program this register to contain the number of clocks required to meet a 0.5µs minimum settling time.

Table 105. Sample Settling Time (ADCSST)

Bits	7	6	5	4	3	2	1	0
Field	Reserved				SST			
Reset	0				1	1	1	1
R/W	R				R/W			
Address	F74H							

Bit Position	Value (H)	Description
[7:4]	0	Reserved; must be 0.
[3:0] SST	0–F	Sample settling time in number of system clock periods to meet 0.5µs minimum.

Bit	Description (Continued)
[5:2] REFLVL	**Comparator 1 Internal Reference Voltage Level** This reference is independent of the ADC voltage reference. 0000 = 0.0 V 0001 = 0.2 V 0010 = 0.4 V 0011 = 0.6 V 0100 = 0.8 V 0101 = 1.0 V (Default) 0110 = 1.2 V 0111 = 1.4 V 1000 = 1.6 V 1001 = 1.8 V 1010–1111 = Reserved
[1:0] TIMTRG	**Timer Trigger (Comparator Counter Mode)** Enable/disable timer operation. 00 = Disable Timer Trigger. 01 = Comparator 1 output works as Timer 0 Trigger. 10 = Comparator 1 output works as Timer 1 Trigger. 11 = Comparator 1 output works as Timer 2 Trigger.

In these two equations, TEMPCALH and TEMPCALL are a pair of Flash option bits containing the calibration data. For more details, see the discussion of TEMPCALH and TEMPCALL in the Flash Option Bits chapter on page 276.

Note: The equations above are temporary test results of the Z8F1680 MCU, version A. The coefficient in the formula may change according to results from tests of version B.

19.1.1. Calibration

The temperature sensor undergoes calibration during the manufacturing process and is maximally accurate only at 30°C. Accuracy decreases as measured temperatures move further from the calibration point.

Because this sensor is an on-chip sensor, Zilog recommends that the user accounts for the difference between ambient and die temperatures when inferring ambient temperature conditions.

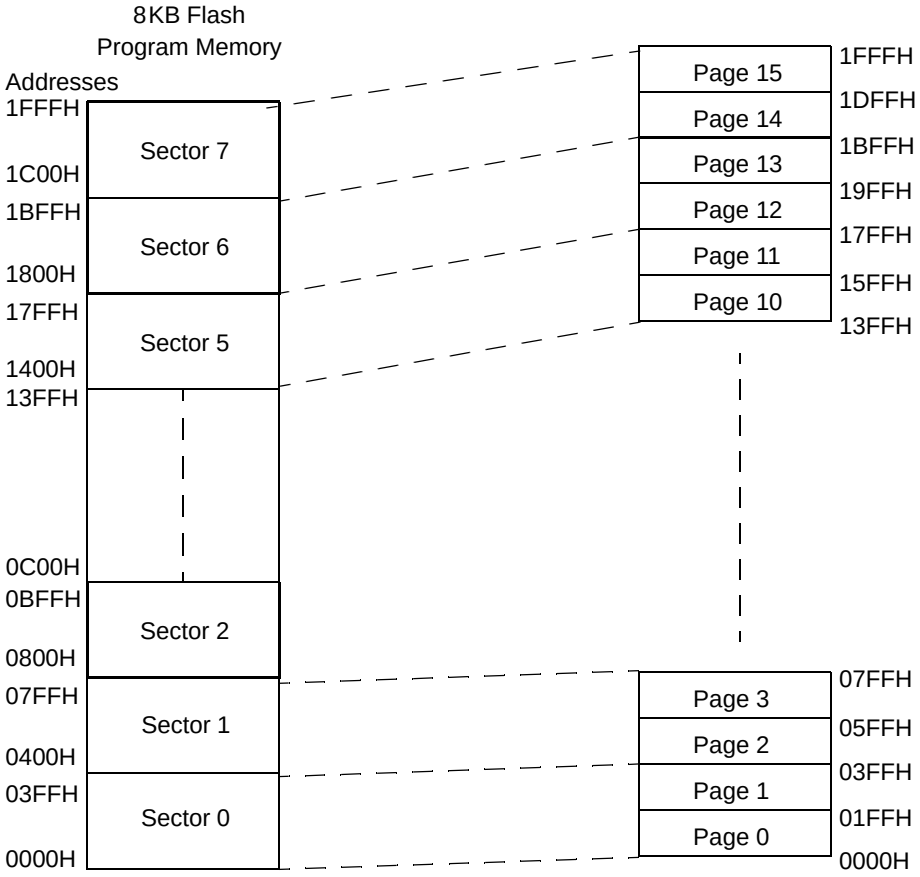

Figure 51. 8KB Flash Memory Arrangement

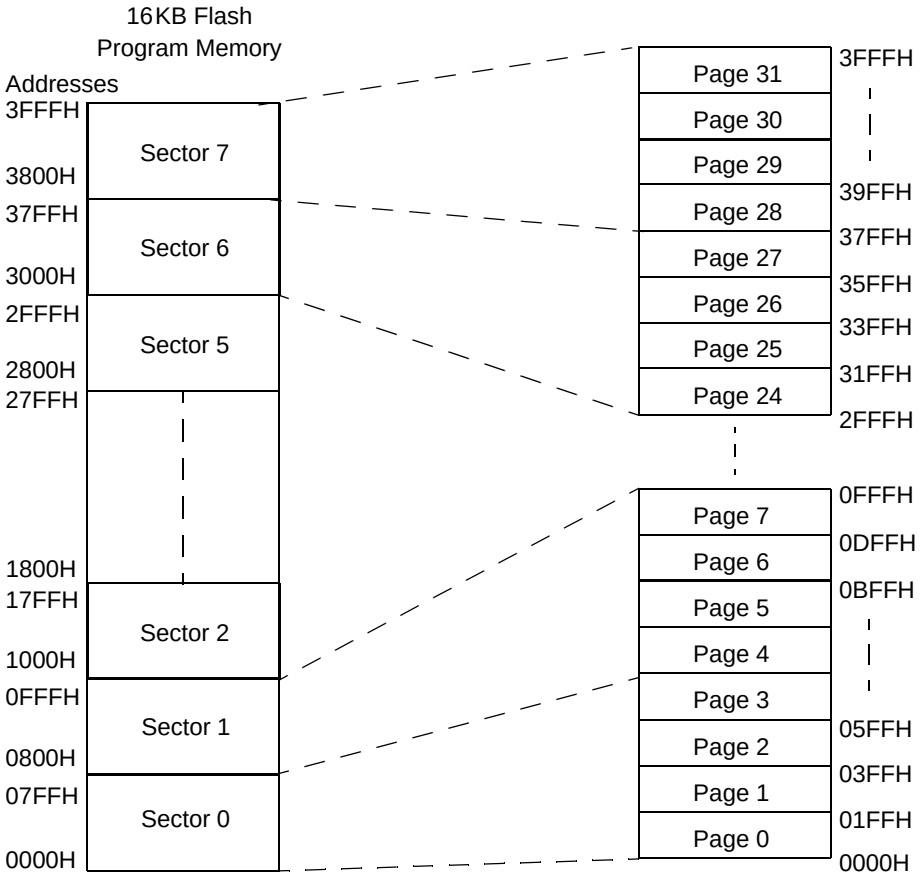

Figure 52. 16KB Flash Memory Arrangement

20.2.1. Flash Operation Timing Using Flash Frequency Registers

Before performing either a program or erase operation on Flash memory, you must first configure the Flash frequency High and Low Byte registers. The Flash frequency registers allow programming and erasing of the Flash with system clock frequencies ranging from 32 kHz (32768 Hz) through 20 MHz.

The Flash frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control timing for flash program and erase operations. The 16-bit binary Flash frequency value must contain the system clock frequency (in kHz). This value is calculated using the following equation:

$$FFREQ[15:0] = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

! Caution: Flash programming and erasure are not supported for system clock frequencies below 32 kHz (32768 Hz) or above 20 MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure operation of the Z8 Encore! XP F1680 Series devices.

20.2.2. Flash Code Protection Against External Access

The user code contained within Flash memory can be protected against external access with the On-Chip Debugger. Programming the FRP Flash option bit prevents reading of the user code with the On-Chip Debugger. For more details, see the Flash Option Bits chapter on page 276 and the On-Chip Debugger chapter on page 294.

20.2.3. Flash Code Protection Against Accidental Program and Erasure

The Z8 Encore! XP F1680 Series provides several levels of protection against accidental program and erasure of the contents of Flash memory. This protection is provided by a combination of the Flash Option bits, the register locking mechanism, the page select redundancy and the sector level protection control of the Flash Controller.

20.2.3.1. Flash Code Protection Using the Flash Option Bits

The FWP Flash option bit provides Flash Program Memory protection as listed in Table 133. For more details, see the Flash Option Bits chapter on page 276.

Table 141. Flash Option Bits at Program Memory Address 0001H

Bits	7	6	5	4	3	2	1	0
Field	EXTLTMG		FLASH_WR_PRO_EN	EXTL_AO	Reserved		X2_Mode	X2TL_AO
Reset	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0001H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:6] EXTLTMG	**External Crystal Reset Timing** 00 = 500 Internal Precision Oscillator Cycles. 01 = 1000 Internal Precision Oscillator Cycles. 10 = 5000 Internal Precision Oscillator Cycles. 11 = 10,000 Internal Precision Oscillator Cycles.
[5] FLASH_WR_PRO_EN	**Flash Write Operation Protect** 0 = Flash write protect disable. 1 = Flash write protect with internal LVD.
[4] EXTL_AO	**External Crystal Always ON** 0 = Crystal oscillator is enabled during Reset, resulting in longer reset timing. 1 = Crystal oscillator is disabled during Reset, resulting in shorter reset timing. Note: This bit determines the state of the external crystal oscillator at Reset. Its selection as system clock must be performed in the Oscillator Control Register (OSCCTL0).
[3:2]	Reserved; must be 00.
[1] X2_Mode	**Secondary Crystal Mode Select** 0 = External clock input. 1 = External 32kHz watch crystal.
[0] X2TL_AO	**Secondary Crystal Always ON** 0 = Secondary Crystal Oscillator is enabled during reset. 1 = Secondary Crystal Oscillator is disabled during reset.

Note: This bit determines state of the Secondary Crystal Oscillator at Reset. Its selection as peripheral clock must be performed in the Peripheral Control (for example, Timer Control2) register.

! **Caution:** When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 1.6V but remains above the Voltage Brown-Out threshold. The oscillator resumes oscillation when the supply voltage exceeds 1.6V.

25.4. Secondary Crystal Oscillator Operation

Figure 65 displays the recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 32kHz. The recommended 32kHz crystal specifications are provided in Table 173. Printed circuit board layout must add no more than 4pF of stray capacitance to either the X_{IN} or X_{OUT} pins. If oscillation does not occur, reduce the values of capacitors C_1 and C_2 to decrease loading.

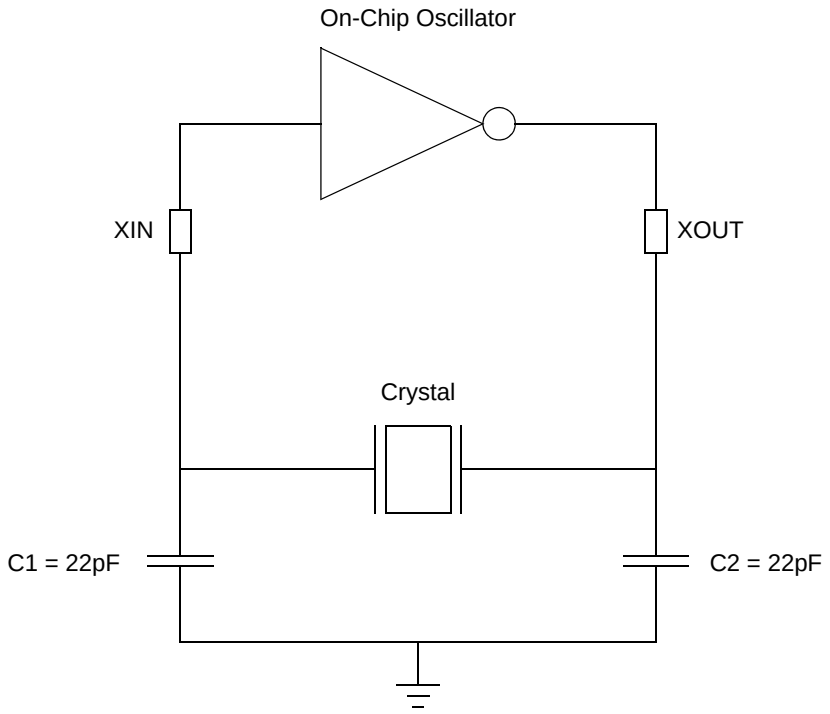

Figure 65. Recommended 32kHz Crystal Oscillator Configuration

Table 186. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
CLR dst	dst ← 00H	R		B0	–	–	–	–	–	–	2	2
		IR		B1							2	3
COM dst	dst ← ~dst	R		60	–	*	*	0	–	–	2	2
		IR		61							2	3
CP dst, src	dst – src	r	r	A2	*	*	*	*	–	–	2	3
		r	Ir	A3							2	4
		R	R	A4							3	3
		R	IR	A5							3	4
		R	IM	A6							3	3
		IR	IM	A7							3	4
CPC dst, src	dst – src – C	r	r	1F A2	*	*	*	*	–	–	3	3
		r	Ir	1F A3							3	4
		R	R	1F A4							4	3
		R	IR	1F A5							4	4
		R	IM	1F A6							4	3
		IR	IM	1F A7							4	4
CPCX dst, src	dst – src – C	ER	ER	1F A8	*	*	*	*	–	–	5	3
		ER	IM	1F A9							5	3
CPX dst, src	dst – src	ER	ER	A8	*	*	*	*	–	–	4	3
		ER	IM	A9							4	3
DA dst	dst ← DA(dst)	R		40	*	*	*	X	–	–	2	2
		IR		41							2	3
DEC dst	dst ← dst – 1	R		30	–	*	*	*	–	–	2	2
		IR		31							2	3
DECW dst	dst ← dst – 1	RR		80	–	*	*	*	–	–	2	5
		IRR		81							2	6
DI	IRQCTL[7] ← 0			8F	–	–	–	–	–	–	1	2

Flags notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

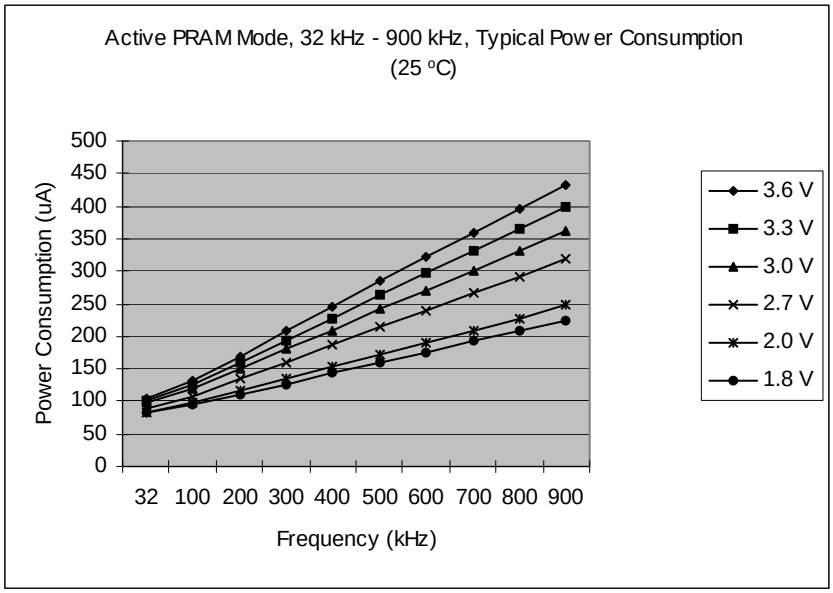

Figure 72. Typical Active PRAM Mode Supply Current (32–900 kHz)

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