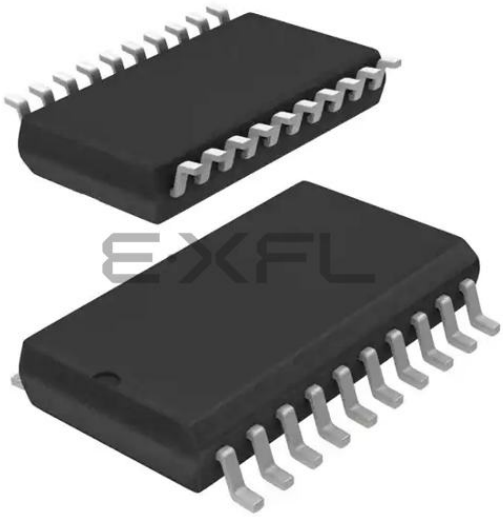

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0880sh020eg

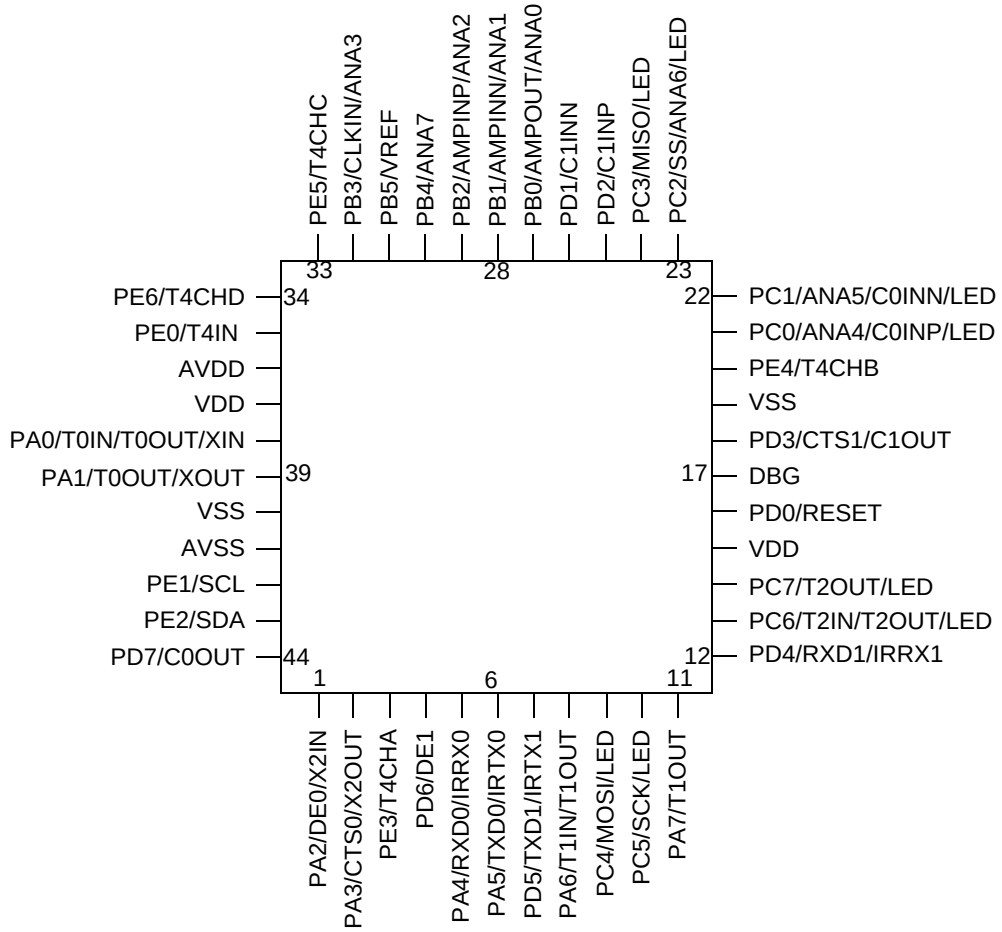


Figure 5. Z8F2480, Z8F1680 and Z8F0880 in 44-Pin Low-Profile Quad Flat Package (LQFP) or Quad Flat No Lead (QFN)

Table 4. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
SCK	I/O	SPI Serial Clock: The SPI master supplies this signal. If the F1680 Series MCU is the SPI master, this pin is an output. If it is the SPI slave, this pin is an input.
MOSI	I/O	Master Out Slave In: This signal is the data output from the SPI master device and the data input to the SPI slave device.
MISO	I/O	Master In Slave Out: This pin is the data input to the SPI master device and the data output from the SPI slave device.
Timers		
T0OUT/T1OUT/ T2OUT	O	Timer Output 0–2: These signals are output from the timers.
$\overline{\text{T0OUT}}$/$\overline{\text{T1OUT}}$/ $\overline{\text{T2OUT}}$	O	Timer Complement Output 0–2: These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0IN/T1IN/T2IN	I	Timer Input 0–2: These signals are used as the capture, gating and counter inputs. The T0IN/T1IN/T2IN signal is multiplexed with $\overline{\text{T0OUT}}$/$\overline{\text{T1OUT}}$/ $\overline{\text{T2OUT}}$ signals.
Multi-Channel Timers		
TACHA, TACHB, TACHC, TACHD	I/O	Multi-channel timer Input/Output: These signals function as Capture input or Compare output for channels CHA, CHB, CHC and CHD.
T4IN	I	Multi-channel Timer clock input: This signal allows external input to serve as the clock source for the Multi-channel timer.
Comparators		
C0INP/C0INN, C1INP/C1INN	I	Comparator Inputs: These signals are positive and negative inputs to the comparator 0 and comparator 1.
C0OUT/C1OUT	O	Comparator Outputs: These are the output from the comparator 0 and the comparator 1.
Analog		
ANA[7:0]	I	Analog Port: These signals are used as inputs to the ADC. The ANA0, ANA1 and ANA2 pins can also access the inputs and outputs of the integrated Low-Power Operational Amplifier.
VREF	I/O	ADC reference voltage input.
Low-Power Operational Amplifier		
AMPINP/AMPINN	I	Low-Power Operational Amplifier Inputs: If enabled, these pins drive the positive and negative amplifier inputs respectively.
AMPOUT	O	Low-Power Operational Amplifier Output: If enabled, this pin is driven by the on-chip low-power operational amplifier.

Table 4. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Oscillators		
XIN	I	External Crystal Input: The input pin to the crystal oscillator. A crystal can be connected between the pin and the XOUT pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
XOUT	O	External Crystal Output: This pin is the output of the crystal oscillator. A crystal can be connected between it and the XIN pin to form the oscillator.
X2IN	I	Watch Crystal Input: The input pin to the low-power 32 kHz oscillator. A watch crystal can be connected between the X2IN and the X2OUT pin to form the oscillator.
X2OUT	O	Watch Crystal Output: This pin is the output from the low power 32 kHz oscillator. A watch crystal can be connected between the X2IN and the X2OUT pin to form the oscillator.
Clock Input		
CLKIN	I	Clock Input Signal: This pin can be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	O	Direct LED Drive Capability: All Port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug: This signal is the control and data input and output of the On-Chip Debugger. **Caution:** The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET: Generates a Reset when asserted (driven Low). Also serves as a Reset indicator; the Z8 Encore! XP forces this pin Low when in Reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V_{DD}	I	Digital Power Supply.
AV_{DD}	I	Analog Power Supply.
V_{SS}	I	Digital Ground.
AV_{SS}	I	Analog Ground.

Note: The AV_{DD} and AV_{SS} signals are available only in 28-pin, 40-pin and 44-pin packages.

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)[1]	Page #
F4B	LIN UART1 Control 1—Multiprocessor Control	U1CTL1	00	172
	LIN UART1 Control 1—Noise Filter Control	U1CTL1	00	174
	LIN UART1 Control 1—LIN Control	U1CTL1	00	175
F4C	LIN UART1 Mode Select and Status	U1MDSTAT	00	168
F4D	UART1 Address Compare	U1ADDR	00	177
F4E	UART1 Baud Rate High Byte	U1BRH	FF	177
F4F	UART1 Baud Rate Low Byte	U1BRL	FF	178
I^2C				
F50	I^2C Data	I2CDATA	00	244
F51	I^2C Interrupt Status	I2CISTAT	80	245
F52	I^2C Control	I2CCTL	00	247
F53	I^2C Baud Rate High Byte	I2CBRH	FF	248
F54	I^2C Baud Rate Low Byte	I2CBRL	FF	249
F55	I^2C State	I2CSTATE	02	251
F56	I^2C Mode	I2CMODE	00	252
F57	I^2C Slave Address	I2CSLVAD	00	255
F58-F5F	Reserved	—	XX	
Enhanced Serial Peripheral Interface (ESPI)				
F60	ESPI Data	ESPIDATA	XX	214
F61	ESPI Transmit Data Command	ESPITDCR	00	214
F62	ESPI Control	ESPICTL	00	215
F63	ESPI Mode	ESPIMODE	00	217
F64	ESPI Status	ESPISTAT	01	219
F65	ESPI State	ESPISTATE	00	220
F66	ESPI Baud Rate High Byte	ESPIBRH	FF	220
F67	ESPI Baud Rate Low Byte	ESPIBRL	FF	220
F68–F6F	Reserved	—	XX	

Notes:
1. XX=Undefined.
2. The Reserved space can be configured as General-Purpose Register File RAM depending on the user option bits (see the User Option Bits chapter on page 277) and the on-chip PRAM size (see the Ordering Information chapter on page 372). If the PRAM is programmed as General-Purpose Register File RAM on Reserved space, the starting address always begins immediately after the end of General-Purpose Register File RAM.

Table 9. Reset and Stop Mode Recovery Characteristics and Latency

	Reset Characteristics and Latency		
Reset Type	**Control Registers**	**eZ8 CPU**	**Reset Latency (Delay)**
System Reset (non-POR Reset)	Reset (as applicable)	Reset	68 Internal Precision Oscillator Cycles after IPO starts up
System Reset (POR Reset)	Reset (as applicable)	Reset	68 Internal Precision Oscillator Cycles + 50ms Wait time
System Reset with Crystal Oscillator Enabled	Reset (as applicable)	Reset	568–10068 Internal Precision Oscillator Cycles after IPO starts up; see Table 141 on page 280 for a description of the EXTLTMG user option bit.
Stop Mode Recovery	Unaffected, except RSTSTAT and OSCCTL registers	Reset	4 Internal Precision Oscillator Cycles after IPO starts up

During a System Reset or Stop Mode Recovery, the Internal Precision Oscillator (IPO) requires 4µs to start up. When the reset type is a System Reset, the F1680 Series MCU is held in Reset for 68 IPO cycles. If the crystal oscillator is enabled in Flash option bits, the Reset period is increased to 568–10068 IPO cycles. For more details, see Table 141 on page 280 for a description of the EXTLTMG user option bit. When the reset type is a Stop Mode Recovery, the F1680 Series MCU goes to NORMAL Mode immediately after 4 IPO cycles. The total Stop Mode Recovey delay is less than 6µs. When a Reset occurs due to a VBO condition, this delay is measured from the time the supply voltage first exceeds the VBO level (discussed later in this chapter). When a Reset occurs due to a POR condition, this delay is measured from the time that the supply voltage first exceeds the POR level. If the external pin reset remains asserted at the end of the Reset period, the device remains in reset until the pin is deasserted.

Note: After a Stop Mode Recovery, the external crystal oscillator is unstable. Use software to wait until it is stable before you can use it as main clock.

At the beginning of Reset, all GPIO pins are configured as inputs with pull-up resistor disabled, except PD0 that is shared with the Reset pin. On Reset, the Port D0 pin is configured as a bidirectional open-drain Reset. The pin is internally driven Low during port reset, after which the user code can reconfigure this pin as a general-purpose output.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and WDT oscillator continue to function.

Chapter 9. Timers

The Z8 Encore! XP F1680 Series products contain three 16-bit reloadable timers that can be used for timing, event counting, or generation of pulse-width modulated signals. The timers' features include:

- 16-bit reload counter
- Programmable prescaler with prescale values ranging from 1 to 128
- PWM output generation
- Capture and compare capability
- Two independent capture/compare channels which reference the common timer
- External input pin for timer input, clock gating, or capture signal. External input pin signal frequency is limited to a maximum of one-fourth the timer clock frequency
- Timer output pin
- Timer interrupt
- Noise Filter on Timer input signal
- Operation in any mode with 32kHz secondary oscillator

In addition to the timers described in this chapter, the Baud Rate Generator (BRG) of unused UART peripheral can also be used to provide basic timing functionality. For more information about using the Baud Rate Generator as additional timers, see the LIN-UART chapter on page 144.

Table 53. TRIGGERED ONE-SHOT Mode Initialization Example (Continued)

Register	Value	Comment
T0CTL1	83H	TEN = 1 enables the timer. All other bits remain in their appropriate settings.

Note: After receiving the input trigger, Timer 0 will:
1. Count ABCDH timer clocks.
2. Upon Timer 0 reload, generate single clock cycle active High output pulse on Timer 0 Output pin.
3. Wait for next input trigger event.

9.2.3.3. CONTINUOUS Mode

In CONTINUOUS Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The Timer counts timer clocks up to the 16-bit reload value. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to `0001H` and counting resumes. Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or High to Low) on timer reload.

Observe the following steps to configure a timer for CONTINUOUS Mode and initiate the count:

1. Write to the Timer Control 1 Register to:
   - Disable the timer
   - Configure the timer for CONTINUOUS Mode
   - Set the prescale value
   - If using the Timer Output Alternate Function, set the initial output level (High or Low)
2. Write to the Timer Control 2 Register to choose the timer clock source.
3. Write to the Timer Control 0 Register to set the timer interrupt-configuration field TICONFIG.
4. Write to the Timer High and Low Byte registers to set the starting count value (usually `0001H`). This value only affects the first pass in CONTINUOUS Mode. After the first timer reload in CONTINUOUS Mode, counting always begins at the reset value of `0001H`.
5. Write to the Timer Reload High and Low Byte registers to set the reload value.
6. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
7. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
8. Write to the Timer Control 1 Register to enable the timer and initiate counting.

If the TPOL bit in the Timer Control 1 Register is set to 1, the Timer Output signal begins as High (1) and then transitions to Low (0) when the timer value matches the PWM value. The Timer Output signal returns to High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control 1 Register is set to 0, the Timer Output signal begins as Low (0) and then transitions to High (1) when the timer value matches the PWM value. The Timer Output signal returns to Low (0) after the timer reaches the reload value and is reset to 0001H.

Observe the following steps to configure a timer for PWM SINGLE OUTPUT Mode and initiate PWM operation:

1. Write to the Timer Control 1 Register to:
   - Disable the timer
   - Configure the timer for PWM mode
   - Set the prescale value
   - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output Alternate Function
2. Write to the Timer Control 2 Register to choose the timer clock source.
3. Write to the Timer Control 0 Register to set the timer interrupt configuration field TICONFIG.
4. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This value only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
5. Write to the Timer PWM0 High and Low Byte registers to set the PWM value.
6. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
7. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
8. Configure the associated GPIO port pin for the Timer Output alternate function.
9. Write to the Timer Control 1 Register to enable the timer and initiate counting.

The PWM period is calculated using the following equation:

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT Mode equation must be used to determine the first PWM time-out period.

- Configure the timer for DEMODULATION Mode. Setting the mode also involves writing to the TMODEHI bit in the TxCTL0 Register
- Set the prescale value
- Set the TPOL bit to set the Capture edge (rising or falling) for the Timer Input. This setting applies only if the TPOLHI bit in the TxCTL2 Register is not set

2. Write to the Timer Control 2 Register to:
   - Choose the timer clock source
   - Set the TPOLHI bit if the Capture is required on both edges of the input signal
3. Write to the Timer Control 0 Register to set the timer interrupt configuration field TICONFIG.
4. Write to the Timer High and Low Byte registers to set the starting count value (typically `0001H`).
5. Write to the Timer Reload High and Low Byte registers to set the reload value.
6. Clear the Timer TxPWM0 and TxPWM1 High and Low Byte registers to `0000H`.
7. If required, enable the noise filter and set the noise filter control by writing to the relevant bits in the Noise Filter Control Register.
8. If required, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt will be generated for both input capture and reload events. If required, configure the timer interrupt to be generated only at the input Capture event or the Reload event by setting TICONFIG field of the Timer Control 0 Register.
9. Configure the associated GPIO port pin for the Timer Input alternate function.
10. Write to the Timer Control 1 Register to enable the timer. Counting will start on the occurrence of the first external input transition.

In DEMODULATION Mode, the elapsed time from timer start to Capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{Timer Clock Frequency (Hz)}}$$

9.3.1. Timer 0–2 High and Low Byte Registers

The Timer 0–2 High and Low Byte (TxH and TxL) registers, shown in Tables 55 and 56, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reading from the TxL reads the register directly.

Writing to the Timer High and Low Byte registers when the timer is enabled is not recommended. There are no temporary holding registers available for write operations; therefore simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

Table 55. Timer 0–2 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H, F08H, F10H							

Table 56. Timer 0–2 Low Byte Register (TxL)

Bit	7	6	5	4	3	2	1	0
Field	TL							
Reset	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H, F11H							

Bit	Description
[7:0] TH, TL	**Timer High and Low Bytes** These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

9.3.2. Timer Reload High and Low Byte Registers

The Timer 0–2 Reload High and Low Byte (TxRH and TxRL) registers, shown in Tables 57 and 58, store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte Register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, this temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit timer reload value.

Chapter 14. Analog-to-Digital Converter

The Z8 Encore! includes an eight-channel Successive Approximation Register Analog-to-Digital converter (SAR ADC). The ADC converts an analog input signal to a 10-bit binary number. The features of the ADC include:

- Eight analog input sources multiplexed with general-purpose I/O ports
- Fast conversion time, less than 4.9 µs
- Programmable timing controls
- Interrupt on conversion complete
- Internal 1.6 V voltage reference generator
- Internal reference voltage available externally
- Ability to supply external reference voltage

14.1. Architecture

The ADC architecture, shown in Figure 30, consists of an 8-input multiplexer, sample-and-hold amplifier and 10-bit SAR ADC. The ADC digitizes the signal on a selected channel and stores the digitized data in the ADC data registers. In environments with high electrical noise, an external RC filter must be added at the input pins to reduce high-frequency noise.

14.2. Operation

The ADC converts the analog input, ANA_X, to a 10-bit digital representation. The equation for calculating the digital value is calculated by:

$$\text{ADC Output} = 1024 \times (ANA_x \div V_{REF})$$

Assuming zero gain and offset errors, any voltage outside the ADC input limits of AV_{SS} and V_{REF} returns all 0s or 1s, respectively.

A new conversion can be initiated by software write to the ADC Control Register's start bit. Initiating a new conversion stops any conversion currently in progress and begins a new conversion. To avoid disrupting a conversion already in progress, this start bit can be read to indicate ADC operation status (busy or available).

Bit Position	Value (H)	Description (Continued)
[5] REFEN	0	Select external reference.
	1	Select internal reference.
[4] ADCEN	0	ADC is disabled.
	1	ADC is enabled for normal use. This bit cannot change with bit 7 (start) at the same time.
[3:0] ANAIN		**Analog Input Select**
	0000	ANA0 input is selected for analog-to-digital conversion.
	0001	ANA1 input is selected for analog-to-digital conversion.
	0010	ANA2 input is selected for analog-to-digital conversion.
	0011	ANA3 input is selected for analog-to-digital conversion.
	0100	ANA4 input is selected for analog-to-digital conversion.
	0101	ANA5 input is selected for analog-to-digital conversion.
	0110	ANA6 input is selected for analog-to-digital conversion.
	0111	ANA7 input is selected for analog-to-digital conversion.
	1000	Hold LPO input nodes (ANA1 and ANA2) to ground.
	1001	Temperature Sensor.
	1100	Temperature Sensor output to ANA3 PAD.
	1101	vbg_chop signal output to ANA3 PAD.
	Others	Reserved.

Bit	Description (Continued)
[6,0] ESPIEN1, ESPIEN0	**ESPI Enable and Direction Control** 00 = The ESPI block is disabled. BRG can be used as a general-purpose timer by setting BRGCTL = 1. 01 = Receive Only Mode. Use this setting in SLAVE Mode if software application is receiving data but not sending. TDRE will not assert. Transmitted data will be all 1s. Not valid in MASTER Mode since Master must source data to drive the transfer. 10 = Transmit Only Mode Use this setting in MASTER or SLAVE Mode when the software application is sending data but not receiving. RDRNE will not assert. 11 = Transmit/Receive Mode Use this setting if the software application is both sending and receiving information. Both TDRE and RDRNE will be active.
[5] BRGCTL	**Baud Rate Generator Control** The function of this bit depends upon ESPIEN1,0. When ESPIEN1,0 = 00, this bit allows enabling the BRG to provide periodic interrupts. **If the ESPI is disabled** 0 = The Baud Rate Generator timer function is disabled. Reading the Baud Rate High and Low registers returns the BRG reload value. 1 = The Baud Rate Generator timer function and time-out interrupt is enabled. Reading the Baud Rate High and Low registers returns the BRG Counter value. **If the ESPI is enabled** 0 = Reading the Baud Rate High and Low registers returns the BRG reload value. If MMEN = 1, the BRG is enabled to generate SCK. If MMEN = 0, the BRG is disabled. 1 = Reading the Baud Rate High and Low registers returns the BRG Counter value. If MMEN = 1, the BRG is enabled to generate SCK. If MMEN = 0 the BRG is enabled to provide a Slave SCK time-out. See the SLAVE Mode Abort error description on page 211. **Caution:** If reading the counter one byte at a time while the BRG is counting keep in mind that the values will not be in sync. Zilog recommends reading the counter using (2-byte) word reads.
[4] PHASE	**Phase Select** Sets the phase relationship of the data to the clock. For more information about operation of the PHASE bit, see the ESPI Clock Phase and Polarity Control section on page 201.
[3] CLKPOL	**Clock Polarity** 0 = SCK idles Low (0). 1 = SCK idles High (1).
[2] WOR	**Wire-OR (Open-Drain) Mode Enabled** 0 = ESPI signal pins not configured for open-drain. 1 = All four ESPI signal pins (SCK, $\overline{SS}$, MISO and MOSI) configured for open-drain function. This setting is typically used for multi-Master and/or Multi-Slave configurations.
[1] MMEN	**ESPI MASTER Mode Enable** This bit controls the data I/O pin selection and SCK direction. 0 = Data out on MISO, data in on MOSI (used in SPI SLAVE Mode), SCK is an input. 1 = Data out on MOSI, data in on MISO (used in SPI MASTER Mode), SCK is an output.

On-Chip Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The write-only Flash Control Register shares its Register File address with the read-only Flash Status Register.

Table 134. Flash Control Register (FCTL)

Bits	7	6	5	4	3	2	1	0
Field	FCMD							
Reset	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Address	FF8H							

Bit	Description
[7:0] FCMD	**Flash Command** 73H = First unlock command. 8CH = Second unlock command. 95H = Page Erase command (must be third command in sequence to initiate Page Erase). 63H = Mass Erase command (must be third command in sequence to initiate Mass Erase). 5EH = Enable Flash Sector Protect Register Access

20.3.2. Flash Status Register

The Flash Status register (Table 135) indicates the current state of the Flash Controller. This register can be read at any time. The read-only Flash Status Register shares its Register File address with the write-only Flash Control Register.

Table 135. Flash Status Register (FSTAT)

Bits	7	6	5	4	3	2	1	0
Field	Program_status		FSTAT					
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	FF8H							

Bit	Description
[7:6] Program_ status	**Indicate the fail or success after Flash Write/Erase** 00 = Success. 10 = Success. 11 = Fail due to low power. 01 = Reserved.

21.2.2. Trim Bit Data Option Bits

The Trim Bit Data Register, shown in Table 142, contains the read or write data for access to the trim option bits.

Table 142. Trim Bit Data Register (TRMDR)

Bits	7	6	5	4	3	2	1	0
Field	TRMDR—Trim Bit Data							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF7H							

21.2.3. Trim Bit Address Option Bits

The Trim Bit Address Register, shown in Table 143, contains the target address for access to the trim option bits. Trim Bit addresses in the range 00H-1FH map to the Information Area address range 20H-3FH, as indicated in Table 142.

Table 143. Trim Bit Address Register (TRMADR)

Bits	7	6	5	4	3	2	1	0
Field	TRMADR—Trim Bit Address (00H to 1FH)							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

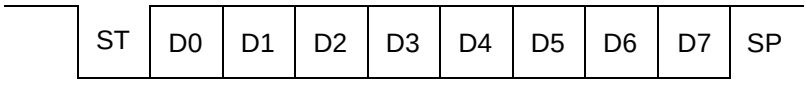
Table 144. Trim Bit Address Map

Trim Bit Address	Information Area Address
00H	20H
01H	21H
02H	22H
03H	23H
:	:
1FH	3FH

- Voltage Brown-Out reset
- Asserting the $\overline{\text{RESET}}$ pin Low to initiate a Reset
- Driving the DBG pin Low when the device is in STOP Mode initiates a System Reset

23.2.2. OCD Data Format

The On-Chip Debugger (OCD) interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 start bit, 8 data bits (least-significant bit first) and 1 stop bit (see Figure 59).



ST = Start bit
SP = Stop bit
D0–D7 = Data bits

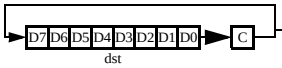
Figure 59. OCD Data Format

23.2.3. OCD Autobaud Detector/Generator

To run over a range of baud rates (bits per second) with various system clock frequencies, the On-Chip Debugger has an Autobaud Detector/Generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character 80H. The character 80H contains eight continuous bits Low (one start bit plus 7 data bits). The Autobaud Detector measures this period and sets the OCD Baud Rate Generator accordingly.

The Autobaud Detector/Generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. If the data can be synchronized with the system clock, the autobaud generator can run as high as the system clock frequency (1 clock/bit). The maximum recommended baud rate is the system clock frequency divided by 8. Table 162 lists the minimum and recommended maximum baud rates for sample crystal frequencies.

Table 186. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
POPX dst	dst ← @SP SP ← SP + 1	ER		D8	–	–	–	–	–	–	3	2
PUSH src	SP ← SP – 1 @SP ← src	R		70	–	–	–	–	–	–	2	2
		IR		71							2	3
		IM		IF70							3	2
PUSHX src	SP ← SP – 1 @SP ← src	ER		C8	–	–	–	–	–	–	3	2
RCF	C ← 0			CF	0	–	–	–	–	–	1	2
RET	PC ← @SP SP ← SP + 2			AF	–	–	–	–	–	–	1	4
RL dst		R		90	*	*	*	*	–	–	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	–	–	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	–	–	2	2
		IR		E1							2	3
RRC dst		R		C0	*	*	*	*	–	–	2	2
		IR		C1							2	3
SBC dst, src	dst ← dst – src – C	r	r	32	*	*	*	*	1	*	2	3
		r	Ir	33							2	4
		R	R	34							3	3
		R	IR	35							3	4
		R	IM	36							3	3
		IR	IM	37							3	4
SBCX dst, src	dst ← dst – src – C	ER	ER	38	*	*	*	*	1	*	4	3
		ER	IM	39							4	3

Flags notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 199. Low Power Operational Amplifier Characteristics

		TA = 0°C to +70°C TA = –40°C to +105°C							
		V_{DD} = 2.7 to 3.6V			V_{DD} = 1.8 to 2.7V				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
AV	DC Gain	–	80	–	–	60	–	dB	
PM	Phase Margin	–	53	–	–	45	–	deg	13 pF loading
GBW	Gain Bandwidth Product	–	0.3	–	–	0.3	–	MHz	
V_{OS}	Input Offset Voltage	–4	–	4	–4	–	4	mV	
V_{OSTA}	Input Offset Temperature Drift	–	1	10	–	1	10	µV/°C	
I_{outTA}	Output Current (Drive ability of LPO)	50	–	–	40	–	–	µA	
I_{DD}LPO	LPO Active Current	–	10	–	–	10	–	µA	
I_{DDQ}LPO	LPO Quiescent Current	–	5	–	–	5	–	nA	
V_{COM}	Maximum Common Input Voltage	–	–	1.4	–	–	0.7	V	

Table 200. IPO Electrical Characteristics

		V_{DD} = 1.8 to 3.6V T_A = –40°C to +105°C			V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
T_{SETUP}	Setup Time for Output Frequency			15			15	µs	
I_{DD}IPO	IPO Active Supply Current		500			500		µA	
I_{DDQ}IPO	IPO Quiescent Current		5			5		nA	

29.4.3. On-Chip Debugger Timing

Figure 77 and Table 206 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4ns maximum rise and fall time.

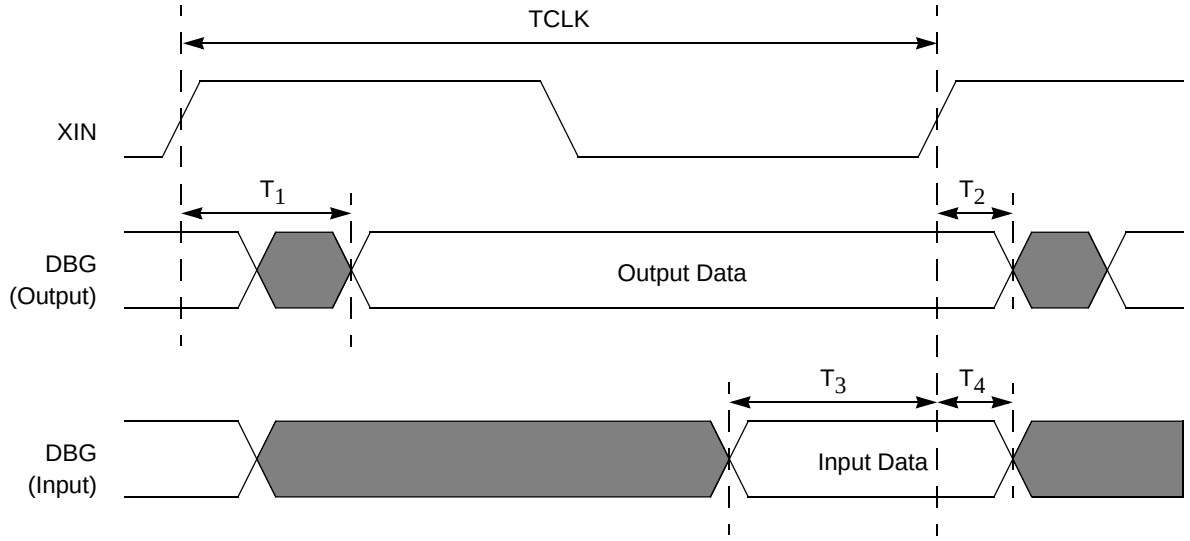


Figure 77. On-Chip Debugger Timing

Table 206. On-Chip Debugger Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Min**	**Max**
DBG			
T_1	X_{IN} Rise to DBG Valid Delay	–	15
T_2	X_{IN} Rise to DBG Output Hold Time	2	–
T_3	DBG to XIN Rise Input Setup Time	5	–
T_4	DBG to XIN Rise Input Hold Time	5	–