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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1680hj020eg

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)[1]	Page #
FD2	Port A Input Data	PAIN	XX	60
FD3	Port A Output Data	PAOUT	00	60
GPIO Port B				
FD4	Port B Address	PBADDR	00	58
FD5	Port B Control	PBCTL	00	60
FD6	Port B Input Data	PBIN	XX	60
FD7	Port B Output Data	PBOUT	00	60
GPIO Port C				
FD8	Port C Address	PCADDR	00	58
FD9	Port C Control	PCCTL	00	60
FDA	Port C Input Data	PCIN	XX	60
FDB	Port C Output Data	PCOUT	00	60
GPIO Port D				
FDC	Port D Address	PDADDR	00	58
FDD	Port D Control	PDCTL	00	60
FDE	Port D Input Data	PDIN	XX	60
FDF	Port D Output Data	PDOUT	00	60
GPIO Port E				
FE0	Port E Address	PEADDR	00	58
FE1	Port E Control	PECTL	00	60
FE2	Port E Input Data	PEIN	XX	60
FE3	Port E Output Data	PEOUT	00	60
FE4–FEF	Reserved	—	XX	
Reset				
FF0	Reset Status	RSTSTAT	XX	40
FF1	Reserved	—	XX	

Notes:
1. XX=Undefined.
2. The Reserved space can be configured as General-Purpose Register File RAM depending on the user option bits (see the User Option Bits chapter on page 277) and the on-chip PRAM size (see the Ordering Information chapter on page 372). If the PRAM is programmed as General-Purpose Register File RAM on Reserved space, the starting address always begins immediately after the end of General-Purpose Register File RAM.

reconfigure the oscillator control block such that the correct system clock source is enabled and selected.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address. Following Stop Mode Recovery, the stop bit in the Reset Status Register is set to 1. Table 11 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information about each of the Stop Mode Recovery sources.

Table 11. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP Mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Interrupt from Timer enabled for STOP Mode operation	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Interrupt from Comparator enabled for STOP Mode operation	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery
	Assertion of external $\overline{\text{RESET}}$ Pin	System Reset
	Debug Pin driven Low	System Reset

5.3.1. Stop Mode Recovery Using Watchdog Timer Time-Out

If the WDT times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status Register, the WDT and stop bits are set to 1. If the WDT is configured to generate an interrupt on time-out and the F1680 Series MCU is configured to respond to interrupts. The eZ8 CPU services the WDT interrupt request following the normal Stop Mode Recovery sequence.

5.3.2. Stop Mode Recovery Using Timer Interrupt

If a Timer with 32K crystal enabled for STOP Mode operation interrupts during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status Register, the stop bit is set to 1. If the F1680 Series MCU is configured to respond to interrupts, the

7.10. GPIO Interrupts

Many of the GPIO port pins can be used as interrupt sources. Some port pins can be configured to generate an interrupt request on either the rising edge or falling edge of the pin-input signal. Other port-pin interrupt sources generate an interrupt when any edge occurs (both rising and falling). For more details about interrupts using the GPIO pins, see the Interrupt Controller chapter on page 68.

7.11. GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data and output data. Table 20 lists these port registers. Use Port A–E Address and Control registers together to provide access to subregisters for port configuration and control.

Table 20. GPIO Port Registers and Subregisters

Port Register Mnemonic	Port Register Name
P*x*ADDR	Port A–E Address Register (Selects subregisters)
P*x*CTL	Port A–E Control Register (Provides access to subregisters)
P*x*IN	Port A–E Input Data Register
P*x*OUT	Port A–E Output Data Register
Port Subregister Mnemonic	**Port Register Name**
P*x*DD	Data Direction
P*x*AF	Alternate Function
P*x*OC	Output Control (Open-Drain)
P*x*HDE	High Drive Enable
P*x*SMRE	Stop Mode Recovery Source Enable
P*x*PUE	Pull-up Enable
PxAFS1	Alternate Function Set 1
PxAFS2	Alternate Function Set 2

Table 54 provides an example initialization sequence for configuring Timer 0 in DEMODULATION Mode and initiating operation.

Table 54. DEMODULATION Mode Initialization Example

Register	Value	Comment
T0CTL0	C0H	TMODE[3:0] = 1100B selects DEMODULATION Mode. TICONFIG[1:0] = 10B enables interrupt only on Capture events. CSC = 0 selects the Timer Input from the GPIO pin. PWMD[2:0] = 000B has no effect. INPCAP = 0 has no effect. TEN = 0 disables the timer. PRES[2:0] = 000B sets prescaler to divide by 1. TPOLHI,TPOL = 10 enables trigger and Capture on both rising and falling edges of Timer Input. TCLKS = 1 enables 32kHz peripheral clock as timer clock source
T0CTL1	04H	
T0CTL2	11H	
T0H	00H	Timer starting value = 0001H.
T0L	01H	
T0RH	ABH	Timer reload value = ABCDH
T0RL	CDH	
T0PWM0H	00H	Initial PWM0 value = 0000H
T0PWM0L	00H	
T0PWM1H	00H	Initial PWM1 value = 0000H
T0PWM1H	00H	
T0NFC	C0H	NFEN = 1 enables noise filter NFCTL = 100B enables 8-bit up/down counter
PAADDR	02H	Selects Port A Alternate Function control register.
PACTL[1:0]	11B	PACTL[0] enables Timer 0 Input alternate function. PACTL[1] enables Timer 0 Output alternate function.
IRQ0ENH[5]	0B	Disables the Timer 0 interrupt.
IRQ0ENL[5]	0B	
T0CTL1	84H	TEN = 1 enables the timer. All other bits remain in their appropriate settings.

Notes: After receiving the input trigger (rising or falling edge), Timer 0 will:

1. Start counting on the timer clock.
2. Upon receiving a Timer 0 Input rising edge, save the Capture value in the T0PWM0 registers, generate an interrupt, and continue to count.
3. Upon receiving a Timer 0 Input falling edge, save the Capture value in the T0PWM1 registers, generate an interrupt, and continue to count.
4. After the timer count to ABCD clocks, set the reload event flag and reset the Timer count to the start value.

Table 88. Mode Status Fields

MULTIPROCESSOR Mode Status Field	**NEWFRM** Status bit denoting the start of a new frame. Reading the LIN-UART Receive Data Register resets this bit to 0. 0 = The current byte is not the first data byte of a new frame. 1 = The current byte is the first data byte of a new frame.
	Multiprocessor Receive (MPRX) Returns the value of the last multiprocessor bit received. Reading from the LIN-UART Receive Data Register resets this bit to 0.
Digital Noise Filter Mode Status Field	**Noise Event (NE); MSEL = 001b** This bit is asserted if digital noise is detected on the receive data line when the data is sampled (center of bit-time). If this bit is set, it does not mean that the receive data is corrupted (though it can be in extreme cases), means that one or more of the noise filter data samples near the center of the bit-time did not match the average data value.
LIN Mode Status Field	**Noise Event (NE); MSEL = 010b** This bit is asserted if some noise level is detected on the receive data line when the data is sampled (center of bit-time). If this bit is set, it does not indicate that the receive data is corrupt (though it can be in extreme cases), means that one or more of the 16x data samples near the center of the bit-time did not match the average data value.
	RxBreakLength LIN mode received break length. This field can be read following a break (LIN Wake-up or Break) so that the software can determine the measured duration of the break. If the break exceeds 15 bit times the value saturates at 1111b.
Hardware Revision Mode Status Field	**Noise Event (NE); MSEL = 111b** This field indicates the hardware revision of the LIN-UART block. 00_xxx LIN UART hardware revision. 01_xxx Reserved. 10_xxx Reserved. 11_xxx Reserved.

Table 97. LIN-UART Baud Rates, 10.0 MHz System Clock (Continued)

Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
38.4	16	39.1	1.73	0.30	2083	0.30	0.2
19.2	33	18.9	0.16				

Table 98. LIN-UART Baud Rates, 5.5296 MHz System Clock

Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	9.60	36	9.60	0.00
625.0	N/A	N/A	N/A	4.80	72	4.80	0.00
250.0	1	345.6	38.24	2.40	144	2.40	0.00
115.2	3	115.2	0.00	1.20	288	1.20	0.00
57.6	6	57.6	0.00	0.60	576	0.60	0.00
38.4	9	38.4	0.00	0.30	1152	0.30	0.00
19.2	18	19.2	0.00				

Table 99. LIN-UART Baud Rates, 3.579545 MHz System Clock

Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Applicable Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	9.60	23	9.73	1.32
625.0	N/A	N/A	N/A	4.80	47	4.76	–0.83
250.0	1	223.72	–10.51	2.40	93	2.41	0.23
115.2	2	111.9	–2.90	1.20	186	1.20	0.23
57.6	4	55.9	–2.90	0.60	373	0.60	–0.04
38.4	6	37.3	–2.90	0.30	746	0.30	–0.04
19.2	12	18.6	–2.90				

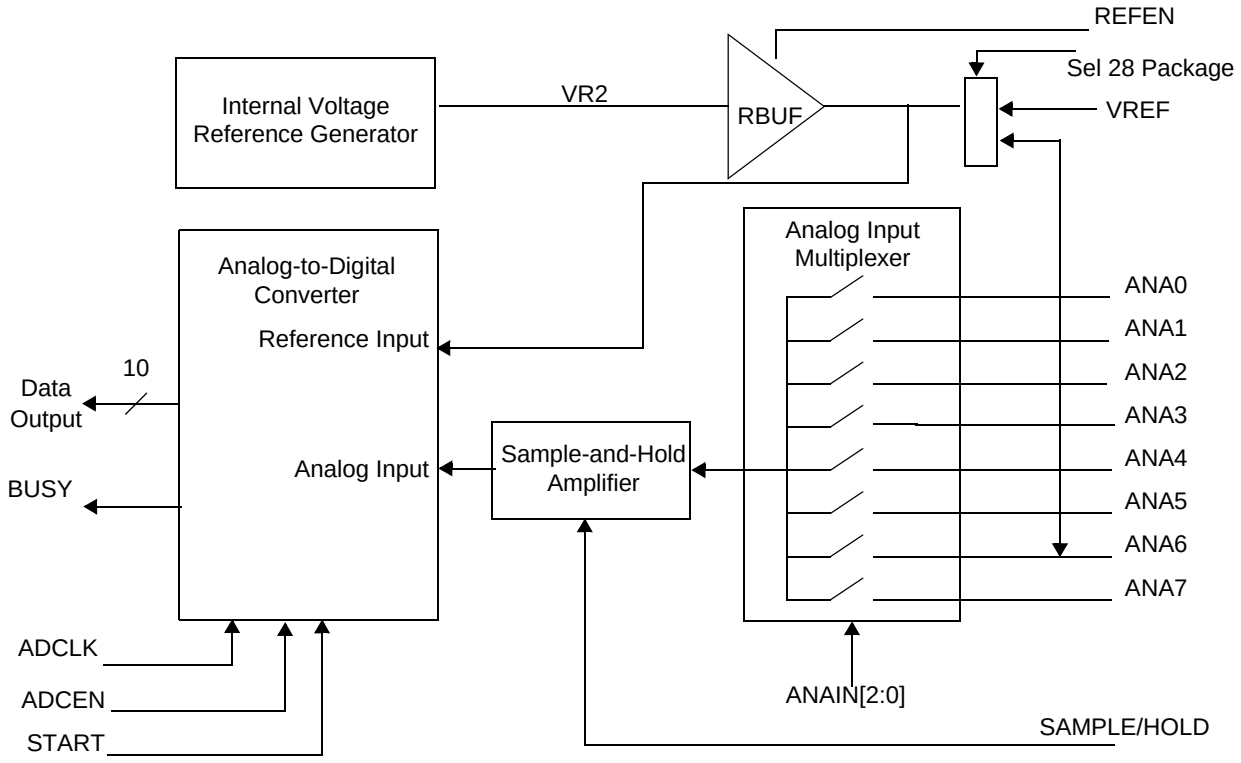

Figure 30. Analog-to-Digital Converter Block Diagram

14.2.1. ADC Timing

Each ADC measurement consists of 3 phases:

1. Input sampling (programmable, minimum of 1.8µs).
2. Sample-and-hold amplifier settling (programmable, minimum of 0.5µs).
3. Conversion is 13 ADCLK cycles.

Figure 31 displays the timing of an ADC conversion.

Table 125. I²C State Register (I2CSTATE)—Description when DIAG = 0

Bits	7	6	5	4	3	2	1	0
Field	ACKV	ACK	AS	DS	10B	RSTR	SCLOUT	BUSY
Reset	0	0	0	0	0	0	1	0
R/W	R	R	R	R	R	R	R	R
Address	F55H							

Bit	Description
[7] ACKV	**ACK Valid** This bit is set, if sending data (Master or Slave) and the ACK bit in this register is valid for the byte just transmitted. This bit can be monitored if it is appropriate for software to verify the ACK value before writing the next byte to be sent. To operate in this mode, the Data Register must not be written when TDRE asserts; instead, the software waits for ACKV to assert. This bit clears when transmission of the next byte begins or the transaction is ended by a stop or restart condition.
[6] ACK	**Acknowledge** This bit indicates the status of the Acknowledge for the last byte transmitted or received. This bit is set for an Acknowledge and cleared for a Not Acknowledge condition.
[5] AS	**Address State** This bit is active High while the address is being transferred on the I²C bus.
[4] DS	**Data State** This bit is active High while the data is being transferred on the I²C bus.
[3] 10B	**10B** This bit indicates whether a 7-bit or 10-bit address is being transmitted when operating as a Master. After the start bit is set, if the five most-significant bits of the address are 11110B, this bit is set. When set, it is Reset after the address has been sent.
[2] RSTR	**RESTART** This bit is updated each time a stop or restart interrupt occurs (SPRS bit set in I2CISTAT Register). 0 = Stop condition. 1 = Restart condition.
[1] SCLOUT	**Serial Clock Output** Current value of Serial Clock being output onto the bus. The actual values of the SCL and SDA signals on the I²C bus can be observed via the GPIO Input Register.
[0] BUSY	**I²C Bus Busy** 0 = No activity on the I²C Bus. 1 = A transaction is underway on the I²C bus.

Chapter 20. Flash Memory

The products in the Z8 Encore! XP F1680 Series feature either 24KB (24576 bytes), 16KB (16384 bytes) and 8KB (8192 bytes) of nonvolatile Flash memory with read/write/erase capability. The Flash memory can be programmed and erased in-circuit by either user code or through the On-Chip Debugger.

The Flash memory array is arranged in pages with 512 bytes per page. The 512 byte page is the minimum Flash block size that can be erased. Each page is divided into 4 rows of 128 bytes.

For program/data protection, Flash memory is also divided into sectors. In the Z8 Encore! XP F1680 Series, Flash memory is divided into 8 sectors which can be protected from programming and erase operation on a per sector basis.

The first 2 bytes of the Flash program memory are used as Flash option bits. For more information about their operation, see the Flash Option Bits chapter on page 276.

Table 132 lists the Flash memory configuration for each device in the Z8 Encore! XP F1680 Series.

Table 132. Z8 Encore! XP F1680 Series Flash Memory Configurations

Part Number	Flash Size in KB (Bytes)	Flash Pages	Program Memory Addresses	Flash Sector Size (bytes)	Number of Sectors	Pages per Sector
Z8F2480	24 (24576)	48	0000H–5FFFH	3072	8	6
Z8F1680	16 (16384)	32	0000H–3FFFH	2048	8	4
Z8F0880	8 (8192)	16	0000H–1FFFH	1024	8	2

20.1. Flash Information Area

The Flash Information Area is separate from Program Memory and is mapped to the address range FE00H to FFFFH. Not all these addresses are user-accessible. Factory trim values for the analog peripherals are stored in the Flash Information Area, and so are factory calibration data for the Temperature Sensor. Figures 51 through 53 display the Flash memory arrangement.

20.2.8. Flash Controller Behavior in Debug Mode

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the On-Chip Debugger:

- The Flash Write Protect option bit is ignored
- The Flash Sector Protect register is ignored for programming and erase operations
- Programming operations are not limited to the page selected in the Page Select Register
- Bits in the Flash Sector Protect register can be written to 1 or 0
- The second write of the Page Select register to unlock the Flash Controller is not necessary
- The Page Select register can be written when the Flash Controller is unlocked
- The Mass Erase command is enabled through the Flash Control Register

! Caution: For security reasons, the Flash controller allows only a single page to be opened for write/erase. When writing multiple Flash pages, the Flash controller must go through the unlock sequence again to select another page.

20.3. Flash Control Register Definitions

This section defines the features of the following Flash Control registers.

Flash Control Register: see page 271

Flash Status Register: see page 272

Flash Page Select Register: see page 273

Flash Sector Protect Register: see page 274

Flash Frequency High and Low Byte Registers: see page 274

20.3.1. Flash Control Register

The Flash Controller must be unlocked using the Flash Control Register (see Table 134) before programming or erasing Flash memory. The Flash Controller is unlocked by writing to the Flash Page Select Register, then 73H 8CH, sequentially, to the Flash Control Register, and finally again to the Flash Page Select Register with the same value as the previous write. When the Flash Controller is unlocked, Mass Erase or Page Erase can be initiated by writing the appropriate command to the FCTL. Erase applies only to the active page selected in the Flash Page Select Register. Mass Erase is enabled only through the

Chapter 21. Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! XP F1680 Series MCU operation. The feature configuration data is stored in Flash program memory and are read during Reset. The features available for control through the Flash option bits include:

- Watchdog Timer time-out response selection–interrupt or System Reset
- Watchdog Timer enabled at Reset
- The ability to prevent unwanted read access to user code in Program Memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in Program Memory
- VBO configuration-always enabled or disabled during STOP Mode to reduce STOP Mode power consumption
- LVD voltage threshold selection
- Oscillator mode selection for high, medium and low-power crystal oscillators or an external RC oscillator
- Factory trimming information for the IPO and Temperature Sensor

21.1. Operation

This section describes the types of option bits and their configuration in the Option Configuration registers.

21.1.1. Option Bit Configuration by Reset

Each time the Flash option bits are programmed or erased, the device must be Reset for the change to take effect. During any Reset operation (System Reset or Stop Mode Recovery), the Flash option bits are automatically read from Flash Program Memory and written to the Option Configuration registers. These Option Configuration registers control operation of the devices within the Z8 Encore! XP F1680 Series MCU. Option bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access.

Table 150. LVD_Trim Values (Continued)

	LVD Threshold (V)			
LVD_TRIM	**Minimum**	**Typical**	**Maximum**	**Description**
01101		2.55		
01110		2.50		
01111		2.45		
10000		2.40		
10001		2.35		
10010		2.30		
10011		2.25		
10100		2.20		
10101		2.15		
10110		2.10		
10111		2.05		
11000		2.00		
11001		1.95		
11010		1.90		
11011		1.85		
11100		1.80		
11101		1.75		
11110		1.70		
11111		1.65		Minimum LVD threshold, default on Reset.

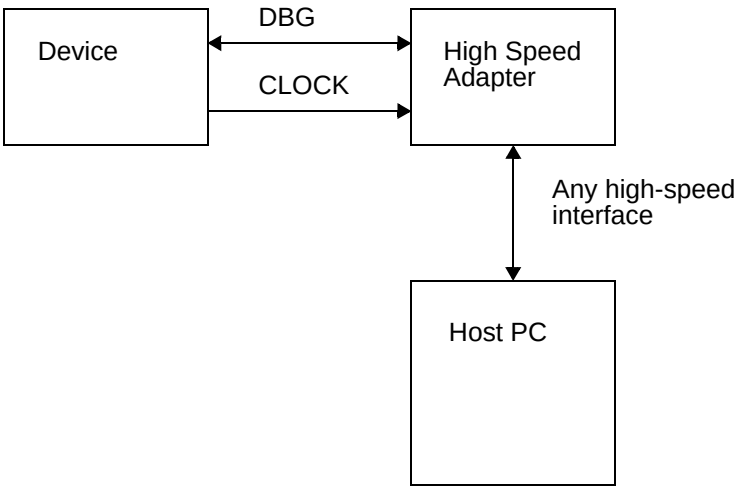

Figure 60. Synchronous Operation

23.2.5. OCD Serial Errors

The On-Chip Debugger can detect any of the following error conditions on the DBG pin:

- Serial Break (a minimum of ten continuous bits Low)
- Framing Error (received stop bit is Low)
- Transmit Collision (OCD and host simultaneous transmission detected by the OCD)

When the OCD detects one of these errors, it aborts any command currently in progress, transmits a Serial Break 4096 system clock cycles long back to the host and resets the Autobaud Detector/Generator. A Framing Error or Transmit Collision can be caused by the host sending a Serial Break to the OCD. Because of the open-drain nature of the interface, returning a Serial Break back to the host only extends the length of the Serial Break if the host releases the Serial Break early.

The host transmits a Serial Break on the DBG pin when first connecting to theZ8 Encore! XP F1680 Series device or when recovering from an error. A Serial Break from the host resets the Autobaud Generator/Detector but does not reset the OCD Control Register. A Serial Break leaves the device in DEBUG mode if that is the current mode. The OCD is held in Reset until the end of the Serial Break when the DBG pin returns High. Because of the open-drain nature of the DBG pin, the host can send a Serial Break to the OCD even if the OCD is transmitting a character.

23.2.6. Automatic Reset

The Z8 Encore! XP F1680 Series devices have the capability to switch clock sources during operation. If the Autobaud is set and the clock source is switched, the Autobaud value becomes invalid. A new Autobaud value must be configured with the new clock frequency.

The oscillator control logic has clock switch detection. If a clock switch is detected and the Autobaud is set, the device will automatically send a Serial Break for 4096 clocks. This will reset the Autobaud and indicate to the host that a new Autobaud character should be sent.

23.2.7. Transmit Flow Control

Transmit flow control is implemented by the use of a remote start bit. When transmit flow control is enabled, the transmitter will wait for the remote host to send the start bit. Transmit flow control is useful in applications where receive overruns can occur.

The remote host can transmit a remote start bit by sending the character FFH. The transmitter will append its data after the start bit. Due to the *wire-and* nature of the open drain bus, the start bit sent by the remote host and the data bits sent by the Z8 Encore! XP F1680 Series device appear as one character; see Figure 61.

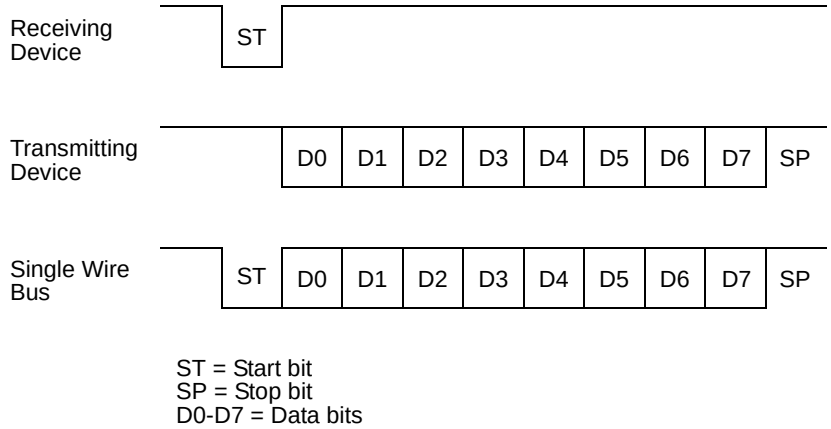

Figure 61. Start Bit Flow Control

23.2.8. Breakpoints

Execution breakpoints are generated using the BRK instruction (op code 00H). When the eZ8 CPU decodes a BRK instruction, it signals the On-Chip Debugger. If breakpoints are enabled, the OCD idles the eZ8 CPU and enters DEBUG mode. If breakpoints are not

23.4.3. Line Control Register

The Line Control Register, shown in Table 166, is used to configure the output driver characteristics during transmission. This register is only used in high-speed implementations.

Table 166. OCD Line Control Register (OCDLCR)

Bit	7	6	5	4	3	2	1	0
Field	Reset		NBTX	NBEN	TXFC	TXDH	TXD	TXHD
Reset	00		0	0	0	0	0	0
R/W	R		R/W	R/W	R/W	R/W	R/W	R/W

Bit	Description
[7:6] Reset	**Reset**
[5] NBTX	**Nine Bit Transmit** This control bit sets the polarity of the ninth bit when nine bit mode is enabled. 0 = Ninth bit is zero. 1 = Ninth bit is one.
[4] NBEN	**Nine Bit Enable** This control bit enables nine-bit mode; it is useful when transmit flow control using remote start bit is enabled to detect valid characters. 0 = Nine Bit mode disabled. 1 = Nine Bit mode enabled.
[3] TXFC	**Transmit Flow Control** 0 = Transmit Flow Control disabled. 1 = Transmit Flow Control using remote start bit.
[2] TXDH	**Transmit Drive High** 0 = Pin is not driven High during 0 to 1 transitions. 1 = Pin is driven High during 0 to 1 transitions.
[1] TXD	**Transmit Drive** 0 = Pin is only driven Low during transmission (Open-Drain). 1 = Pin is always driven during transmission.
[0] TXHD	**Transmit High Drive Strength** 0 = Pin output driver is Low drive strength. 1 = Pin output driver is High drive strength.

Table 186. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
LD dst, rc	dst ← src	r	IM	0C-FC	–	–	–	–	–	–	2	2
		r	X(r)	C7							3	3
		X(r)	r	D7							3	4
		r	Ir	E3							2	3
		R	R	E4							3	2
		R	IR	E5							3	4
		R	IM	E6							3	2
		IR	IM	E7							3	3
		Ir	r	F3							2	3
		IR	R	F5							3	3
LDC dst, src	dst ← src	r	Irr	C2	–	–	–	–	–	–	2	5
		Ir	Irr	C5							2	9
		Irr	r	D2							2	5
LDCI dst, src	dst ← src r ← r + 1 rr ← rr + 1	Ir	Irr	C3	–	–	–	–	–	–	2	9
		Irr	Ir	D3							2	9
LDE dst, src	dst ← src	r	Irr	82	–	–	–	–	–	–	2	5
		Irr	r	92							2	5
LDEI dst, src	dst ← src r ← r + 1 rr ← rr + 1	Ir	Irr	83	–	–	–	–	–	–	2	9
		Irr	Ir	93							2	9
LDWX dst, src	dst ← src	ER	ER	1FE8	–	–	–	–	–	–	5	4

Flags notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Figures 67 and 68 provide information about each of the eZ8 CPUinstructions.

Upper Nibble (Hex) \ Lower Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	1.1 **BRK**	2.2 **SRP** IM	2.3 **ADD** r1,r2	2.4 **ADD** r1,Ir2	3.3 **ADD** R2,R1	3.4 **ADD** IR2,R1	3.3 **ADD** R1,IM	3.4 **ADD** IR1,IM	4.3 **ADDX** ER2,ER1	4.3 **ADDX** IM,ER1	2.3 **DJNZ** r1,X	2.2 **JR** cc,X	2.2 **LD** r1,IM	3.2 **JP** cc,DA	1.2 **INC** r1	1.2 **NOP**
1	2.2 **RLC** R1	2.3 **RLC** IR1	2.3 **ADC** r1,r2	2.4 **ADC** r1,Ir2	3.3 **ADC** R2,R1	3.4 **ADC** IR2,R1	3.3 **ADC** R1,IM	3.4 **ADC** IR1,IM	4.3 **ADCX** ER2,ER1	4.3 **ADCX** IM,ER1						See 2nd Op Code Map
2	2.2 **INC** R1	2.3 **INC** IR1	2.3 **SUB** r1,r2	2.4 **SUB** r1,Ir2	3.3 **SUB** R2,R1	3.4 **SUB** IR2,R1	3.3 **SUB** R1,IM	3.4 **SUB** IR1,IM	4.3 **SUBX** ER2,ER1	4.3 **SUBX** IM,ER1						1, 2 ATM
3	2.2 **DEC** R1	2.3 **DEC** IR1	2.3 **SBC** r1,r2	2.4 **SBC** r1,Ir2	3.3 **SBC** R2,R1	3.4 **SBC** IR2,R1	3.3 **SBC** R1,IM	3.4 **SBC** IR1,IM	4.3 **SBCX** ER2,ER1	4.3 **SBCX** IM,ER1						
4	2.2 **DA** R1	2.3 **DA** IR1	2.3 **OR** r1,r2	2.4 **OR** r1,Ir2	3.3 **OR** R2,R1	3.4 **OR** IR2,R1	3.3 **OR** R1,IM	3.4 **OR** IR1,IM	4.3 **ORX** ER2,ER1	4.3 **ORX** IM,ER1						
5	2.2 **POP** R1	2.3 **POP** IR1	2.3 **AND** r1,r2	2.4 **AND** r1,Ir2	3.3 **AND** R2,R1	3.4 **AND** IR2,R1	3.3 **AND** R1,IM	3.4 **AND** IR1,IM	4.3 **ANDX** ER2,ER1	4.3 **ANDX** IM,ER1						1.2 **WDT**
6	2.2 **COM** R1	2.3 **COM** IR1	2.3 **TCM** r1,r2	2.4 **TCM** r1,Ir2	3.3 **TCM** R2,R1	3.4 **TCM** IR2,R1	3.3 **TCM** R1,IM	3.4 **TCM** IR1,IM	4.3 **TCMX** ER2,ER1	4.3 **TCMX** IM,ER1						1.2 **STOP**
7	2.2 **PUSH** R2	2.3 **PUSH** IR2	2.3 **TM** r1,r2	2.4 **TM** r1,Ir2	3.3 **TM** R2,R1	3.4 **TM** IR2,R1	3.3 **TM** R1,IM	3.4 **TM** IR1,IM	4.3 **TMX** ER2,ER1	4.3 **TMX** IM,ER1						1.2 **HALT**
8	2.5 **DECW** RR1	2.6 **DECW** IRR1	2.5 **LDE** r1,Irr2	2.9 **LDEI** Ir1,Irr2	3.2 **LDX** r1,ER2	3.3 **LDX** Ir1,ER2	3.4 **LDX** IRR2,R1	3.5 **LDX** IRR2,IR1	3.4 **LDX** r1,rr2,X	3.4 **LDX** rr1,r2,X						1.2 **DI**
9	2.2 **RL** R1	2.3 **RL** IR1	2.5 **LDE** r2,Irr1	2.9 **LDEI** Ir2,Irr1	3.2 **LDX** r2,ER1	3.3 **LDX** Ir2,ER1	3.4 **LDX** R2,IRR1	3.5 **LDX** IR2,IRR1	3.3 **LEA** r1,r2,X	3.5 **LEA** rr1,rr2,X						1.2 **EI**
A	2.5 **INCW** RR1	2.6 **INCW** IRR1	2.3 **CP** r1,r2	2.4 **CP** r1,Ir2	3.3 **CP** R2,R1	3.4 **CP** IR2,R1	3.3 **CP** R1,IM	3.4 **CP** IR1,IM	4.3 **CPX** ER2,ER1	4.3 **CPX** IM,ER1						1.4 **RET**
B	2.2 **CLR** R1	2.3 **CLR** IR1	2.3 **XOR** r1,r2	2.4 **XOR** r1,Ir2	3.3 **XOR** R2,R1	3.4 **XOR** IR2,R1	3.3 **XOR** R1,IM	3.4 **XOR** IR1,IM	4.3 **XORX** ER2,ER1	4.3 **XORX** IM,ER1						1.5 **IRET**
C	2.2 **RRC** R1	2.3 **RRC** IR1	2.5 **LDC** r1,Irr2	2.9 **LDCI** Ir1,Irr2	2.3 **JP** IRR1	2.9 **LDC** Ir1,Irr2		3.4 **LD** r1,r2,X	3.2 **PUSHX** ER2							1.2 **RCF**
D	2.2 **SRA** R1	2.3 **SRA** IR1	2.5 **LDC** r2,Irr1	2.9 **LDCI** Ir2,Irr1	2.6 **CALL** IRR1	2.2 **BSWAP** R1	3.3 **CALL** DA	3.4 **LD** r2,r1,X	3.2 **POPX** ER1							1.2 **SCF**
E	2.2 **RR** R1	2.3 **RR** IR1	2.2 **BIT** p,b,r1	2.3 **LD** r1,Ir2	3.2 **LD** R2,R1	3.3 **LD** IR2,R1	3.2 **LD** R1,IM	3.3 **LD** IR1,IM	4.2 **LDX** ER2,ER1	4.2 **LDX** IM,ER1						1.2 **CCF**
F	2.2 **SWAP** R1	2.3 **SWAP** IR1	2.6 **TRAP** Vector	2.3 **LD** Ir1,r2	2.8 **MULT** RR1	3.3 **LD** R2,IR1	3.3 **BTJ** p,b,r1,X	3.4 **BTJ** p,b,Ir1,X								

Figure 67. First Op Code Map

Table 199. Low Power Operational Amplifier Characteristics

		TA = 0°C to +70°C TA = –40°C to +105°C							
		V_{DD} = 2.7 to 3.6V			V_{DD} = 1.8 to 2.7V				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
AV	DC Gain	–	80	–	–	60	–	dB	
PM	Phase Margin	–	53	–	–	45	–	deg	13 pF loading
GBW	Gain Bandwidth Product	–	0.3	–	–	0.3	–	MHz	
V_{OS}	Input Offset Voltage	–4	–	4	–4	–	4	mV	
V_{OSTA}	Input Offset Temperature Drift	–	1	10	–	1	10	µV/°C	
I_{outTA}	Output Current (Drive ability of LPO)	50	–	–	40	–	–	µA	
I_{DD}LPO	LPO Active Current	–	10	–	–	10	–	µA	
I_{DDQ}LPO	LPO Quiescent Current	–	5	–	–	5	–	nA	
V_{COM}	Maximum Common Input Voltage	–	–	1.4	–	–	0.7	V	

Table 200. IPO Electrical Characteristics

		V_{DD} = 1.8 to 3.6V T_A = –40°C to +105°C			V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
T_{SETUP}	Setup Time for Output Frequency			15			15	µs	
I_{DD}IPO	IPO Active Supply Current		500			500		µA	
I_{DDQ}IPO	IPO Quiescent Current		5			5		nA	

29.4.1. General Purpose I/O Port Input Data Sample Timing

Figure 75 displays timing of the GPIO Port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The Port value is available to the eZ8 CPU on the second rising clock edge following the change of the Port value.

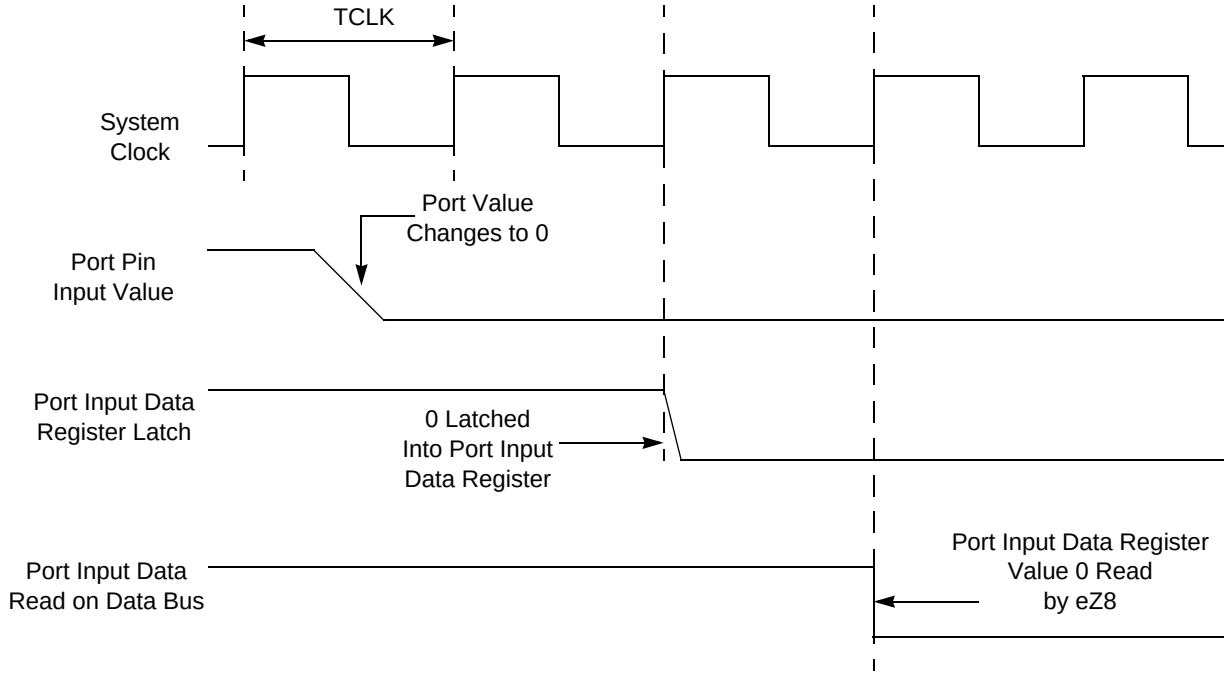

Figure 75. Port Input Sample Timing

Table 204. GPIO Port Input Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Min**	**Max**
T_{S_PORT}	Port Input Transition to XIN Rise Setup Time (Not pictured)	5	–
T_{H_PORT}	XIN Rise to Port Input Transition Hold Time (Not pictured)	0	–
T_{SMR}	GPIO Port Pin Pulse Width to ensure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources)	1 µs	

Table 209. Ordering Information for the Z8 Encore! XP F1680 Series of MCUs (Continued)

Part Number	Flash	Register RAM	Program RAM	NVDS	I^2C	SPI	I/O Lines	Interrupt Vectors	16-Bit Timers w/ PWM	10-Bit A/D Channels	UART with IrDA	Comparator	Temperature Sensor	Multichannel Timer	Description
Z8 Encore! XP F1680 Series with 8KB Flash, 10-Bit Analog-to-Digital Converter															
Standard Temperature: 0°C to 70°C															
Z8F0880SH020SG	8KB	1KB	1KB	128 B	1	0	17	20	3	7	1	1	1	0	SOIC 20-pin package
Z8F0880HH020SG	8KB	1KB	1KB	128 B	1	0	17	20	3	7	1	1	1	0	SSOP 20-pin package
Z8F0880PH020SG	8KB	1KB	1KB	128 B	1	0	17	20	3	7	1	1	1	0	PDIP 20-pin package
Z8F0880SJ020SG	8KB	1KB	1KB	128 B	1	1	23	21	3	8	1	1	1	0	SOIC 28-pin package
Z8F0880HJ020SG	8KB	1KB	1KB	128 B	1	1	23	21	3	8	1	1	1	0	SSOP 28-pin package
Z8F0880PJ020SG	8KB	1KB	1KB	128 B	1	1	23	21	3	8	1	1	1	0	PDIP 28-pin package
Z8F0880PM020SG	8KB	1KB	1KB	128 B	1	1	33	23	3	8	2	2	1	0	PDIP 40-pin package
Z8F0880AN020SG	8KB	1K B	1KB	128 B	1	1	37	24	3	8	2	2	1	1	LQFP 44-pin package
Z8F0880QN020SG	8KB	1KB	1KB	128 B	1	1	37	24	3	8	2	2	1	1	QFN 44-pin package
Extended Temperature: –40°C to 105°C															
Z8F0880SH020EG	8KB	1KB	1KB	128 B	1	0	17	20	3	7	1	1	1	0	SOIC 20-pin package
Z8F0880HH020EG	8KB	1KB	1KB	128 B	1	0	17	20	3	7	1	1	1	0	SSOP 20-pin package
Z8F0880PH020EG	8KB	1KB	1KB	128 B	1	0	17	20	3	7	1	1	1	0	PDIP 20-pin package
Z8F0880SJ020EG	8KB	1KB	1KB	128 B	1	1	23	21	3	8	1	1	1	0	SOIC 28-pin package
Z8F0880HJ020EG	8KB	1KB	1KB	128 B	1	1	23	21	3	8	1	1	1	0	SSOP 28-pin package
Z8F0880PJ020EG	8KB	1KB	1KB	128 B	1	1	23	21	3	8	1	1	1	0	PDIP 28-pin package
Z8F0880PM020EG	8KB	1KB	1KB	128 B	1	1	33	23	3	8	2	2	1	0	PDIP 40-pin package
Z8F0880AN020EG	8KB	1KB	1KB	128 B	1	1	37	24	3	8	2	2	1	1	LQFP 44-pin package
Z8F0880QN020EG	8KB	1KB	1KB	128 B	1	1	37	24	3	8	2	2	1	1	QFN 44-pin package
Z8F16800128ZCOG	Z8 Encore! XP F1680 28-pin Series Development Kit														
Z8F16800144ZCOG	Z8 Encore! XP Dual 44-pin F1680 Series Development Kit														
ZUSBSC00100ZACG	USB Smart Cable Accessory Kit														
ZUSBOPTSC01ZACG	USB Opto-Isolated Smart Cable Accessory Kit														
ZENETSC0100ZACG	Ethernet Smart Cable Accessory Kit														