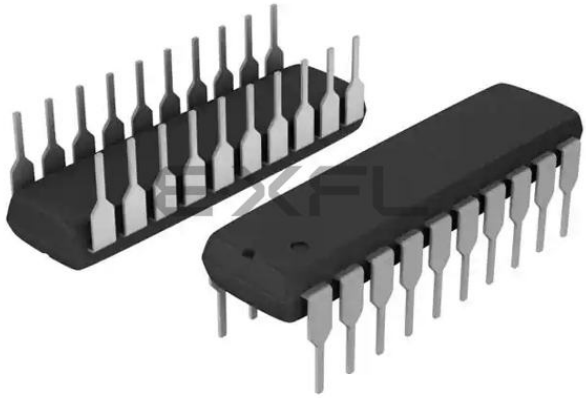

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1680ph020eg

List of Tables

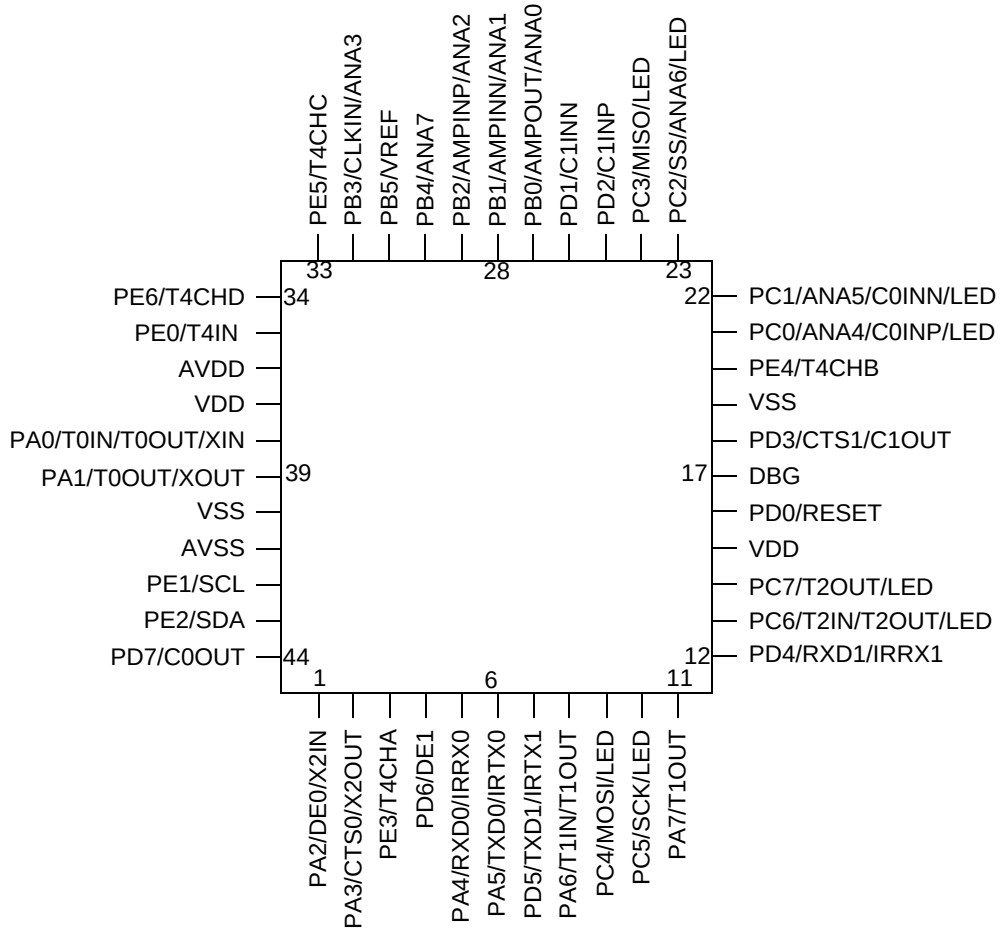

Figure 5. Z8F2480, Z8F1680 and Z8F0880 in 44-Pin Low-Profile Quad Flat Package (LQFP) or Quad Flat No Lead (QFN)

Table 4. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
SCK	I/O	SPI Serial Clock: The SPI master supplies this signal. If the F1680 Series MCU is the SPI master, this pin is an output. If it is the SPI slave, this pin is an input.
MOSI	I/O	Master Out Slave In: This signal is the data output from the SPI master device and the data input to the SPI slave device.
MISO	I/O	Master In Slave Out: This pin is the data input to the SPI master device and the data output from the SPI slave device.
Timers		
T0OUT/T1OUT/ T2OUT	O	Timer Output 0–2: These signals are output from the timers.
$\overline{\text{T0OUT}}$/$\overline{\text{T1OUT}}$/ $\overline{\text{T2OUT}}$	O	Timer Complement Output 0–2: These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0IN/T1IN/T2IN	I	Timer Input 0–2: These signals are used as the capture, gating and counter inputs. The T0IN/T1IN/T2IN signal is multiplexed with $\overline{\text{T0OUT}}$/$\overline{\text{T1OUT}}$/ $\overline{\text{T2OUT}}$ signals.
Multi-Channel Timers		
TACHA, TACHB, TACHC, TACHD	I/O	Multi-channel timer Input/Output: These signals function as Capture input or Compare output for channels CHA, CHB, CHC and CHD.
T4IN	I	Multi-channel Timer clock input: This signal allows external input to serve as the clock source for the Multi-channel timer.
Comparators		
C0INP/C0INN, C1INP/C1INN	I	Comparator Inputs: These signals are positive and negative inputs to the comparator 0 and comparator 1.
C0OUT/C1OUT	O	Comparator Outputs: These are the output from the comparator 0 and the comparator 1.
Analog		
ANA[7:0]	I	Analog Port: These signals are used as inputs to the ADC. The ANA0, ANA1 and ANA2 pins can also access the inputs and outputs of the integrated Low-Power Operational Amplifier.
VREF	I/O	ADC reference voltage input.
Low-Power Operational Amplifier		
AMPINP/AMPINN	I	Low-Power Operational Amplifier Inputs: If enabled, these pins drive the positive and negative amplifier inputs respectively.
AMPOUT	O	Low-Power Operational Amplifier Output: If enabled, this pin is driven by the on-chip low-power operational amplifier.

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)[1]	Page #
F4B	LIN UART1 Control 1—Multiprocessor Control	U1CTL1	00	172
	LIN UART1 Control 1—Noise Filter Control	U1CTL1	00	174
	LIN UART1 Control 1—LIN Control	U1CTL1	00	175
F4C	LIN UART1 Mode Select and Status	U1MDSTAT	00	168
F4D	UART1 Address Compare	U1ADDR	00	177
F4E	UART1 Baud Rate High Byte	U1BRH	FF	177
F4F	UART1 Baud Rate Low Byte	U1BRL	FF	178
I^2C				
F50	I^2C Data	I2CDATA	00	244
F51	I^2C Interrupt Status	I2CISTAT	80	245
F52	I^2C Control	I2CCTL	00	247
F53	I^2C Baud Rate High Byte	I2CBRH	FF	248
F54	I^2C Baud Rate Low Byte	I2CBRL	FF	249
F55	I^2C State	I2CSTATE	02	251
F56	I^2C Mode	I2CMODE	00	252
F57	I^2C Slave Address	I2CSLVAD	00	255
F58-F5F	Reserved	—	XX	
Enhanced Serial Peripheral Interface (ESPI)				
F60	ESPI Data	ESPIDATA	XX	214
F61	ESPI Transmit Data Command	ESPITDCR	00	214
F62	ESPI Control	ESPICTL	00	215
F63	ESPI Mode	ESPIMODE	00	217
F64	ESPI Status	ESPISTAT	01	219
F65	ESPI State	ESPISTATE	00	220
F66	ESPI Baud Rate High Byte	ESPIBRH	FF	220
F67	ESPI Baud Rate Low Byte	ESPIBRL	FF	220
F68–F6F	Reserved	—	XX	

Notes:
1. XX=Undefined.
2. The Reserved space can be configured as General-Purpose Register File RAM depending on the user option bits (see the User Option Bits chapter on page 277) and the on-chip PRAM size (see the Ordering Information chapter on page 372). If the PRAM is programmed as General-Purpose Register File RAM on Reserved space, the starting address always begins immediately after the end of General-Purpose Register File RAM.

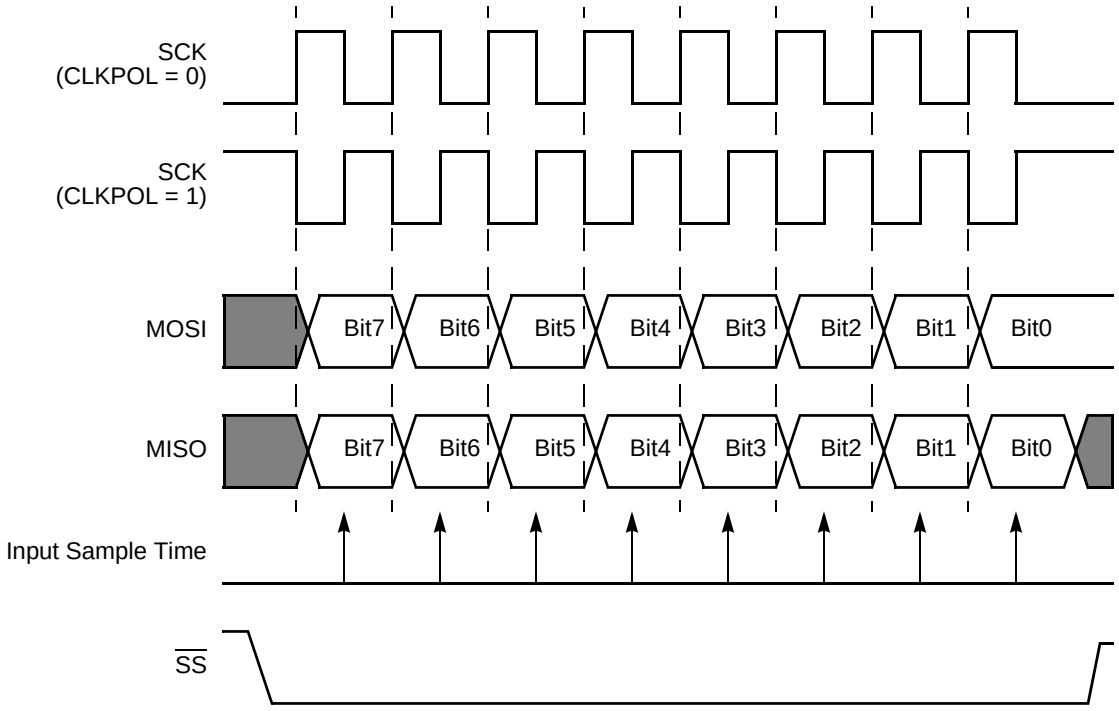

Figure 35. ESPI Timing when PHASE = 1

16.3.3. Slave Select Modes of Operation

This section describes the different modes of data transfer supported by the ESPI block. The mode is selected by the Slave Select Mode (SSMD) field of the Mode Register.

16.3.3.1. SPI Mode

This mode is selected by setting the SSMD field of the Mode Register to 00. In this mode software controls the assertion of the $\overline{SS}$ signal directly via the SSV bit of the SPI Transmit Data Command register. Software can be used to control an SPI mode transaction. Prior to or simultaneously with writing the first transmit data byte; software sets the SSV bit. Software sets the SSV bit either by performing a byte write to the Transmit Data Command register prior to writing the first transmit character to the Data Register or by performing a word write to the Data Register address which loads the first transmit character and simultaneously sets the SSV bit. $\overline{SS}$ will remain asserted when one or more characters are transferred. There are two mechanisms for deasserting $\overline{SS}$ at the end of the transaction. One method used by software is to set the TEOF bit of the Transmit Data Command register, when the last TDRE interrupt is being serviced (set TEOF before or simultaneously with writing the last data byte). After the last bit of the last character is

Bit	Description
[3] BRKPC	**Break when PC == OCDCNTR** If this bit is set to 1, then the OCDCNTR Register is used as a hardware breakpoint. When the program counter matches the value in the OCDCNTR Register, DBGMODE is automatically set to 1. If this bit is set, the OCDCNTR Register does not count when the CPU is running. 0 = OCDCNTR is set up as a counter. 1 = OCDCNTR generates a hardware break when PC == OCDCNTR.
[2] BRKZRO	**Break when OCDCNTR == 0000H** If this bit is set, then the OCD automatically sets the DBGMODE bit when the OCDCNTR Register counts down to 0000H. If this bit is set, the OCDCNTR Register is not reset when the part exits DEBUG Mode. 0 = OCD does not generate BRK when OCDCNTR decrements to 0000H. 1 = OCD sets DBGMODE to 1 when OCDCNTR decrements to 0000H.
[1]	Reserved; must be 0.
[0] RST	**Reset** Setting this bit to 1 resets the device. The controller goes through a normal POR sequence with the exception that the On-Chip Debugger is not reset. This bit is automatically cleared to 0 when the reset finishes. 0 = No effect. 1 = Reset the device.

Table 188. Absolute Maximum Ratings* (Continued)

Parameter	Min	Max	Units	Notes
44-Pin QFN Maximum Ratings at –40°C to 70°C				
Total power dissipation		750	mW	
Maximum current into V_{DD} or out of V_{SS}		200	mA	
44-Pin QFN Maximum Ratings at 70°C to 105°C				
Total power dissipation		295	mW	
Maximum current into V_{DD} or out of V_{SS}		83	mA	
44-pin LQFP Maximum Ratings at –40°C to 70°C				
Total power dissipation		750	mW	
Maximum current into V_{DD} or out of V_{SS}		200	mA	
44-pin LQFP Maximum Ratings at 70°C to 105°C				
Total power dissipation		410	mW	
Maximum current into V_{DD} or out of V_{SS}		114	mA	

Notes:
*Operating temperature is specified in DC Characteristics.
1. This voltage applies to all pins except the following: V_{DD}, AV_{DD}.

29.2. DC Characteristics

Table 189 lists the DC characteristics of the Z8 Encore! XP F1680 Series products. All voltages are referenced to V_{SS}, which is the primary system ground.

Table 189. DC Characteristics

		T_A = 0°C to +70°C T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{DD}	Supply Voltage	1.8	–	3.6	V	
V_{IL1}	Low Level Input Voltage	–0.3	–	0.3*V_{DD}	V	For all input pins except $\overline{\text{RESET}}$, DBG, XIN
V_{IL2}	Low Level Input Voltage	–0.3	–	0.2*V_{DD}	V	For $\overline{\text{RESET}}$, DBG, XIN
V_{IH1}	High Level Input Voltage	0.7*V_{DD}	–	5.5	V	Port A, B, C, D and E pins (Digital inputs)

Notes:
1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.

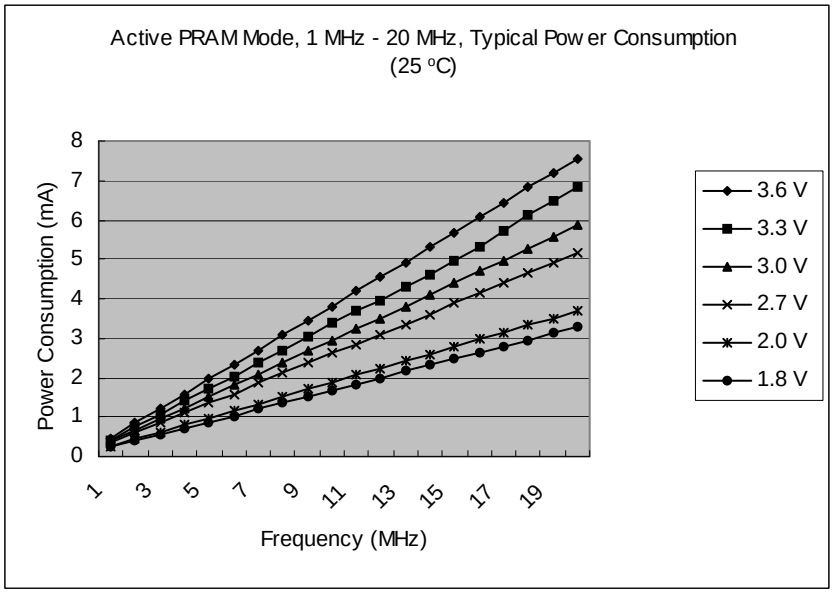

Figure 70. Typical Active PRAM Mode Supply Current (1–20MHz)

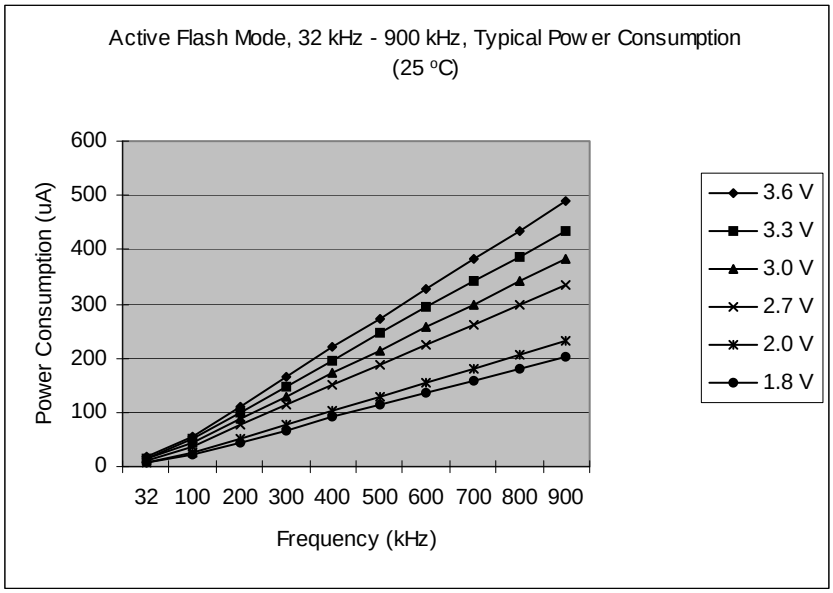

Figure 71. Typical Active Flash Mode Supply Current (32–900kHz)