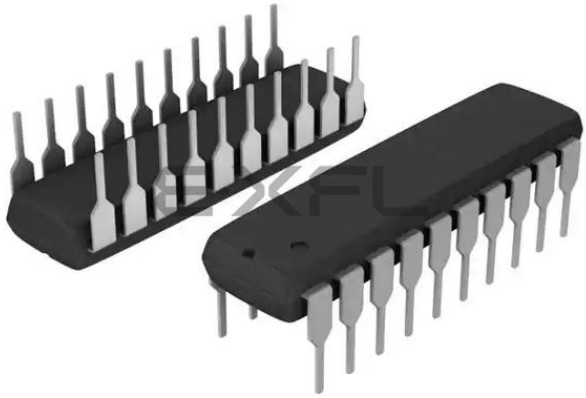

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f2480ph020sg

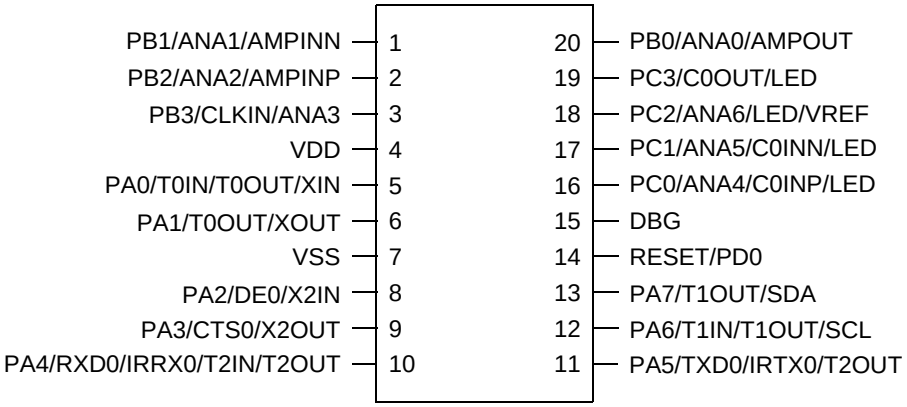

Figure 2. Z8F2480, Z8F1680 and Z8F0880 in 20-Pin SOIC, SSOP or PDIP Packages

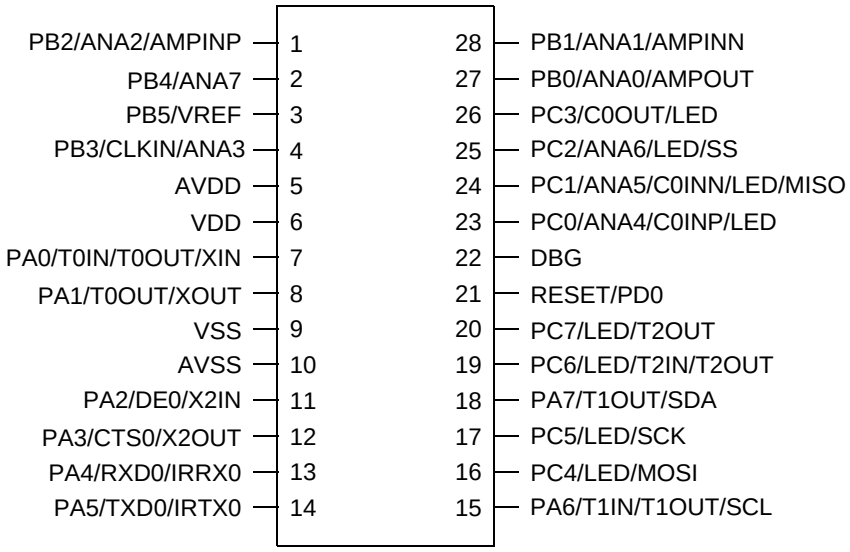

Figure 3. Z8F2480, Z8F1680 and Z8F0880 in 28-Pin SOIC, SSOP or PDIP Packages

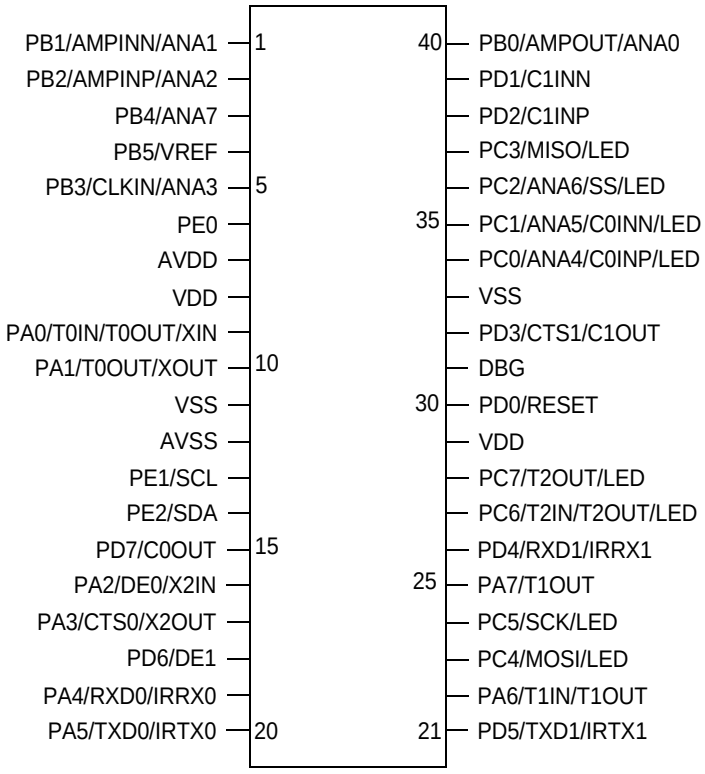

Figure 4. Z8F2480, Z8F1680 and Z8F0880 in 40-Pin Dual Inline Package (PDIP)

Table 6. F1680 Series MCU Program Memory Maps (Continued)

Program Memory Address (Hex)	Function
Z8F1680 Device	
0000–0001	Flash option bits
0002–0003	Reset vector
0004–0005	WDT interrupt vector
0006–0007	Illegal instruction trap
0008–0037	Interrupt vectors*
0038–003D	Oscillator fail traps*
003E–3FFF	Program Flash
E000–E3FF	1KB PRAM
Z8F0880 Device	
0000–0001	Flash option bits
0002–0003	Reset vector
0004–0005	WDT interrupt vector
0006–0007	Illegal instruction trap
0008–0037	Interrupt vectors*
0038–003D	Oscillator fail traps*
003E–1FFF	Program Flash
E000–E3FF	1KB PRAM

Note: *See Table 36 on page 69 for a list of interrupt vectors and traps.

3.3. Data Memory

The F1680 Series MCU does not use the eZ8 CPU's 64KB Data Memory address space.

3.4. Flash Information Area

Table 7 describes the F1680 Series MCU Flash Information Area. This 512-byte Information Area is accessed by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash Information Area is mapped into the Program Memory and overlays the 512bytes at addresses FE00H to FFFFH. When the Information Area access is enabled, all reads from these Program Memory addresses return the Information Area data rather than the Program Memory data. Access to the Flash Information Area is read-only.

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)[1]	Page #
Multi-Channel Timer				
FA0	MCT High Byte	MCTH	00	130
FA1	MCT Low Byte	MCTL	00	130
FA2	MCT Reload High Byte	MCTRH	FF	131
FA3	MCT Reload Low Byte	MCTRL	FF	131
FA4	MCT Subaddress	MCTSA	XX	132
FA5	MCT Subregister 0	MCTSR0	XX	132
FA6	MCT Subregister 1	MCTSR1	XX	132
FA7	MCT Subregister 2	MCTSR2	XX	132
FA8–FBF	Reserved	—	XX	
Interrupt Controller				
FC0	Interrupt Request 0	IRQ0	00	73
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	76
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	77
FC3	Interrupt Request 1	IRQ1	00	74
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	78
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	79
FC6	Interrupt Request 2	IRQ2	00	75
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	80
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	81
FC9–FCC	Reserved	—	XX	
FCD	Interrupt Edge Select	IRQES	00	82
FCE	Shared Interrupt Select	IRQSS	00	82
FCF	Interrupt Control	IRQCTL	00	83
GPIO Port A				
FD0	Port A Address	PAADDR	00	58
FD1	Port A Control	PACTL	00	60

Notes:
1. XX=Undefined.
2. The Reserved space can be configured as General-Purpose Register File RAM depending on the user option bits (see the User Option Bits chapter on page 277) and the on-chip PRAM size (see the Ordering Information chapter on page 372). If the PRAM is programmed as General-Purpose Register File RAM on Reserved space, the starting address always begins immediately after the end of General-Purpose Register File RAM.

7.11.5. Port A–E Output Control Subregisters

The Port A–E Output Control Subregister, shown in Table 25, is accessed through the Port A–E Control Register by writing 03H to the Port A–E Address Register. Setting the bits in the Port A–E Output Control subregisters to 1 configures the specified port pins for open-drain operation. These subregisters affect the pins directly and, as a result, alternate functions are also affected.

Table 25. Port A–E Output Control Subregisters (PxOC)

Bits	7	6	5	4	3	2	1	0
Field	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 03H in Port A–E Address Register, accessible through the Port A–E Control Register							

Bit	Description
[7:0] POC	**Port Output Control** These bits function independently of the alternate function bit and always disable the drains if set to 1. 0 = The drains are enabled for any output mode (unless overridden by the alternate function). 1 = The drain of the associated pin is disabled (open-drain mode).

7.11.6. Port A–E High Drive Enable Subregisters

The Port A–E High Drive Enable Subregister, shown in Table 26, is accessed through the Port A–E Control Register by writing 04H to the Port A–E Address Register. Setting the bits in the Port A–E High Drive Enable subregisters to 1 configures the specified port pins for high-current output drive operation. The Port A–E High Drive Enable Subregister affects the pins directly and, as a result, alternate functions are also affected.

Table 26. Port A–E High Drive Enable Subregisters (PxHDE)

Bits	7	6	5	4	3	2	1	0
Field	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 04H in Port A–E Address Register, accessible through the Port A–E Control Register							

Bit	Description
[7:0] PHDE	**Port High Drive Enabled** 0 = The Port pin is configured for standard output current drive. 1 = The Port pin is configured for high output current drive.

7.11.7. Port A–E Stop Mode Recovery Source Enable Subregisters

The Port A–E Stop Mode Recovery Source Enable Subregister, shown in Table 27, is accessed through the Port A–E Control Register by writing 05H to the Port A–E Address Register. Setting the bits in the Port A–E Stop Mode Recovery Source Enable subregisters to 1 configures the specified port pins as Stop Mode Recovery sources. During STOP Mode, any logic transition on a port pin enabled as a Stop Mode Recovery source initiates Stop Mode Recovery.

Table 27. Port A–E Stop Mode Recovery Source Enable Subregisters (PxSMRE)

Bits	7	6	5	4	3	2	1	0
Field	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 05H in Port A–E Address Register, accessible through the Port A–E Control Register.							

Bit	Description
[7:0] PSMRE	**Port Stop Mode Recovery Source Enabled** 0 = The Port pin is not configured as a Stop Mode Recovery source. Transitions on this pin during STOP Mode do not initiate Stop Mode Recovery. 1 = The Port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP Mode initiates Stop Mode Recovery.

7.11.8. Port A–E Pull-up Enable Subregisters

The Port A–E Pull-up Enable Subregister, shown in Table 28, is accessed through the Port A–E Control Register by writing 06H to the Port A–E Address Register. Setting the bits in the Port A–E Pull-up Enable subregisters enables a weak internal resistive pull-up on the specified port pins.

Table 28. Port A–E Pull-Up Enable Subregisters (PxPUE)

Bits	7	6	5	4	3	2	1	0
Field	PPUE7	PPUE6	PPUE5	PPUE4	PPUE3	PPUE2	PPUE1	PPUE0
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 06H in Port A–E Address Register, accessible through the Port A–E Control Register.							

Bit	Description
[7:0] PPUE	**Port Pull-up Enabled** 0 = The weak pull-up on the Port pin is disabled. 1 = The weak pull-up on the Port pin is enabled.

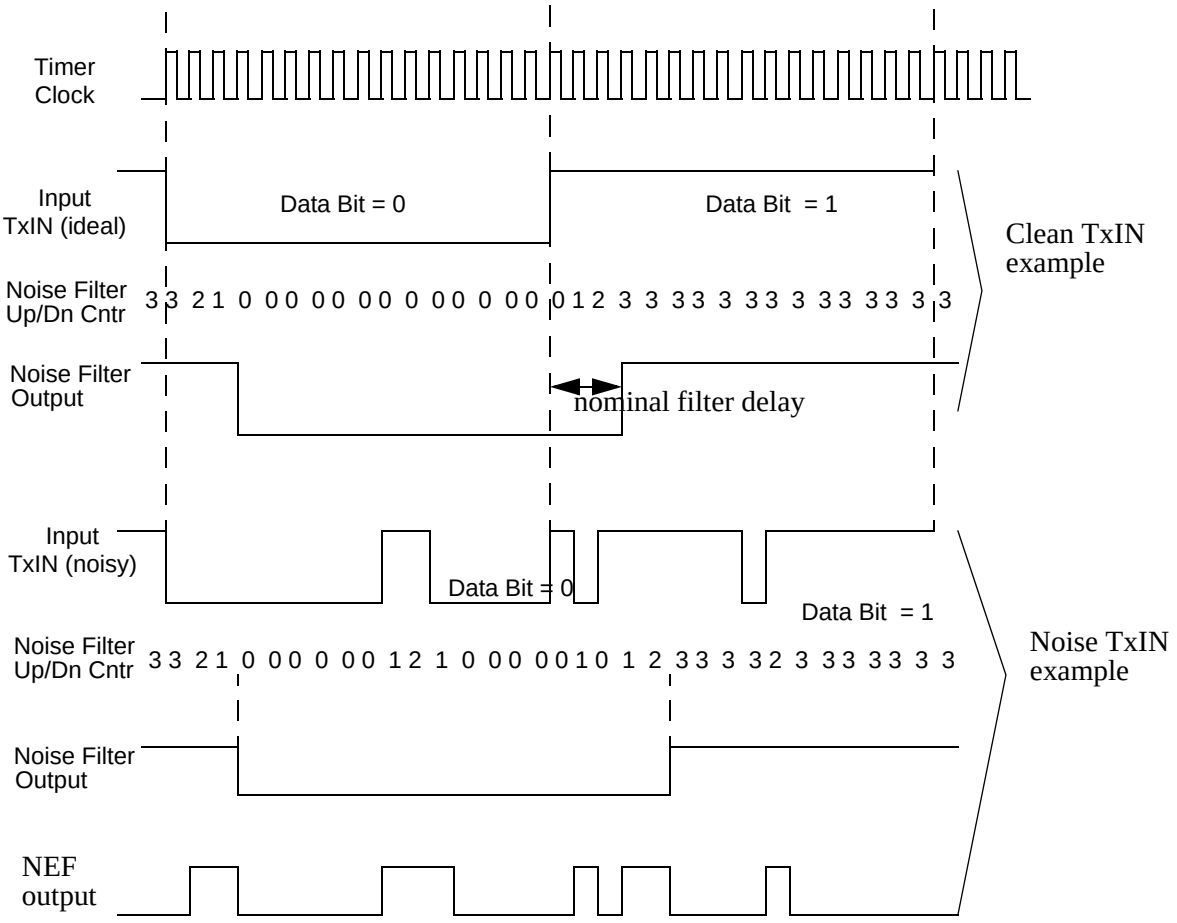

Figure 13. Noise Filter Operation

9.3. Timer Control Register Definitions

This section defines the features of the following Timer Control registers.

Timer 0–2 High and Low Byte Registers: see page 109

Timer Reload High and Low Byte Registers: see page 109

Timer 0–2 PWM0 High and Low Byte Registers: see page 110

Timer 0–2 PWM1 High and Low Byte Registers: see page 111

Timer 0–2 Control Registers: see page 112

Timer 0–2 Status Registers: see page 118

Timer 0–2 Noise Filter Control Register: see page 119

9.3.1. Timer 0–2 High and Low Byte Registers

The Timer 0–2 High and Low Byte (TxH and TxL) registers, shown in Tables 55 and 56, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register when the timers are enabled. When the timer is disabled, reading from the TxL reads the register directly.

Writing to the Timer High and Low Byte registers when the timer is enabled is not recommended. There are no temporary holding registers available for write operations; therefore simultaneous 16-bit writes are not possible. If either the Timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

Table 55. Timer 0–2 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H, F08H, F10H							

Table 56. Timer 0–2 Low Byte Register (TxL)

Bit	7	6	5	4	3	2	1	0
Field	TL							
Reset	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H, F11H							

Bit	Description
[7:0] TH, TL	**Timer High and Low Bytes** These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

9.3.2. Timer Reload High and Low Byte Registers

The Timer 0–2 Reload High and Low Byte (TxRH and TxRL) registers, shown in Tables 57 and 58, store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte Register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, this temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit timer reload value.

Bit	Description (Continued)
[6] TPOL	**Timer Input/Output Polarity** Operation of this field is a function of the current operating modes of the timer. **ONE-SHOT Mode** When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer reload. **CONTINUOUS Mode** When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer reload. **COUNTER Mode** When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer reload. 0 = Count occurs on the rising edge of the Timer Input signal. 1 = Count occurs on the falling edge of the Timer Input signal. **PWM SINGLE OUTPUT Mode** 0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) on PWM count match and forced Low (0) on Reload. 1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) on PWM count match and forced High (1) on Reload. **CAPTURE Mode** 0 = Count is captured on the rising edge of the Timer Input signal. 1 = Count is captured on the falling edge of the Timer Input signal. **COMPARE Mode** When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented on timer reload. **GATED Mode** 0 = Timer counts when the Timer Input signal is High (1) and interrupts are generated on the falling edge of the Timer Input. 1 = Timer counts when the Timer Input signal is Low (0) and interrupts are generated on the rising edge of the Timer Input. **CAPTURE/COMPARE Mode** 0 = Counting is started on the first rising edge of the Timer Input signal. The current count is captured on subsequent rising edges of the Timer Input signal. 1 = Counting is started on the first falling edge of the Timer Input signal. The current count is captured on subsequent falling edges of the Timer Input signal.

Table 77. Multi-Channel Timer Channel Status 1 Register (MCTCHS1)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				CHDEF	CHCEF	CHBEF	CHAEF
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Address	See note.							

Note: If a 01H is in the Subaddress Register, it is accessible through Subregister 1.

Bit	Description
[7:4]	Reserved; must be 0.
[3:0] CHyEF	**Channel y Event Flag** This bit indicates if a Capture/Compare event occurred for this channel. Software can use this bit to determine the channel(s) responsible for generating the Multi-Channel Timer channel interrupt. This event flag is cleared by writing a 1 to the bit. These bits will be set when an event occurs independent of the setting of the CHIEN bit. This bit is cleared when TEN=0 (TEN is the MSB of MCTCTL1). 0 = No Capture/Compare Event occurred for this channel. 1 = A Capture/Compare Event occurred for this channel.

Bit	Description (Continued)
[2] SBRK	**Send Break** This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has completed sending data before setting this bit. In standard UART mode, the duration of the break is determined by how long the software leaves this bit asserted. Also the duration of any required stop bits following the break must be timed by software before writing a new byte to be transmitted to the Transmit Data Register. In LIN mode, the master sends a Break character by asserting SBRK. The duration of the break is timed by hardware and the SBRK bit is deasserted by hardware when the Break is completed. The duration of the Break is determined by the TxBreakLength field of the LIN Control Register. One or two stop bits are automatically provided by the hardware in LIN mode as defined by the stop bit. 0 = No break is sent. 1 = The output of the transmitter is 0.
[1] STOP	**Stop Bit Select** 0 = The transmitter sends one stop bit. 1 = The transmitter sends two stop bits.
[0] LBEN	**Loop Back Enable** 0 = Normal operation. 1 = All transmitted data is looped back to the receiver within the IrDA module.

12.3.6. LIN-UART Control 1 Registers

Multiple registers, shown in Tables 90 and 91, are accessible by a single bus address. The register selected is determined by the Mode Select (MSEL) field. These registers provide additional control over LIN-UART operation.

16.4.5. ESPI Status Register

The ESPI Status Register, shown in Table 113, indicates the current state of the ESPI. All bits revert to their Reset state if the ESPI is disabled.

Table 113. ESPI Status Register (ESPISTAT)

Bits	7	6	5	4	3	2	1	0
Field	TDRE	TUND	COL	ABT	ROVR	RDRNE	TFST	SLAS
Reset	1	0	0	0	0	0	0	1
R/W	R	R/W*	R/W*	R/W*	R/W*	R	R	R
Address	F64H							

Note: R/W* = Read access. Write a 1 to clear the bit to 0.

Bit	Description
[7] TDRE	**Transmit Data Register Empty** 0 = Transmit Data Register is full or ESPI is disabled. 1 = Transmit Data Register is empty. A write to the ESPI (Transmit) Data Register clears this bit.
[6] TUND	**Transmit Underrun** 0 = A Transmit Underrun error has not occurred. 1 = A Transmit Underrun error has occurred.
[5] COL	**Collision** 0 = A multi-Master collision (mode fault) has not occurred. 1 = A multi-Master collision (mode fault) has occurred.
[4] ABT	**SLAVE Mode Transaction Abort** This bit is set if the ESPI is configured in SLAVE Mode, a transaction is occurring and $\overline{SS}$ deasserts before all bits of a character have been transferred as defined by the NUMBITS field of the ESPIMODE register. This bit can also be set in SLAVE Mode by an SCK monitor time-out (MMEN = 0, BRGCTL = 1). 0 = A SLAVE Mode transaction abort has not occurred. 1 = A SLAVE Mode transaction abort has occurred.
[3] ROVR	**Receive Overrun** 0 = A Receive Overrun error has not occurred. 1 = A Receive Overrun error has occurred.
[2] RDRNE	**Receive Data Register Not Empty** 0 = Receive Data Register is empty. 1 = Receive Data Register is not empty.

Table 116. ESPI Baud Rate High Byte Register (ESPIBRH)

Bits	7	6	5	4	3	2	1	0
Field	BRH							
Reset	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F66H							

Bit	Description
[7:0] BRH	**ESPI Baud Rate High Byte** The most significant byte, BRG[15:8], of the ESPI Baud Rate Generator's reload value.

Table 117. ESPI Baud Rate Low Byte Register (ESPIBRL)

Bits	7	6	5	4	3	2	1	0
Field	BRL							
Reset	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/w
Address	F67H							

Bit	Description
[7:0] BRL	**ESPI Baud Rate Low Byte** The least significant byte, BRG[7:0], of the ESPI Baud Rate Generator's reload value.

transferred from the Slave to the Master. The transaction field labels are defined as follows:

S Start
W Write
A Acknowledge
$\overline{A}$ Not Acknowledge
P Stop

17.2.5.4. Master Write Transaction with a 7-Bit Address

Figure 43 displays the data transfer format from a Master to a 7-bit addressed slave.

S	Slave Address	W = 0	A	Data	A	Data	A	Data	A/$\overline{A}$	P/S

Figure 43. Data Transfer Format—Master Write Transaction with a 7-Bit Address

Observe the following steps for a Master transmit operation to a 7-bit addressed slave:

1. The software initializes the MODE field in the I^2C Mode Register for MASTER/SLAVE Mode with either a 7-bit or 10-bit slave address. The MODE field selects the address width for this mode when addressed as a slave (but not for the remote slave). The software asserts the IEN bit in the I^2C Control Register.
2. The software asserts the TXI bit of the I^2C Control Register to enable transmit interrupts.
3. The I^2C interrupt asserts, because the I^2C Data Register is empty.
4. The software responds to the TDRE bit by writing a 7-bit slave address plus the Write bit (which is cleared to 0) to the I^2C Data Register.
5. The software sets the start bit of the I^2C Control Register.
6. The I^2C controller sends a start condition to the I^2C slave.
7. The I^2C controller loads the I^2C Shift Register with the contents of the I^2C Data Register.
8. After one bit of the address has been shifted out by the SDA signal, the transmit interrupt asserts.
9. The software responds by writing the transmit data into the I^2C Data Register.
10. The I^2C controller shifts the remainder of the address and the Write bit out via the SDA signal.

Bit	Description (Continued)
[5:2] REFLVL	**Comparator 0 Internal Reference Voltage Level** This reference is independent of the ADC voltage reference. 0000 = 0.0 V 0001 = 0.2 V 0010 = 0.4 V 0011 = 0.6 V 0100 = 0.8 V 0101 = 1.0 V (Default) 0110 = 1.2 V 0111 = 1.4 V 1000 = 1.6 V 1001 = 1.8 V 1010–1111 = Reserved
[1:0] TIMTRG	**Timer Trigger (COMPARATOR COUNTER MODE)** 00 = Disable Timer Trigger. 01 = Comparator 0 output works as Timer 0 Trigger. 10 = Comparator 0 output works as Timer 1 Trigger. 11 = Comparator 0 output works as Timer 2 Trigger.

18.2.2. Comparator 1 Control Register

The Comparator 1 Control Register (CMP1), shown in Table 131, configures the comparator 1 inputs and sets the value of the internal voltage reference.

Table 131. Comparator 1 Control Register (CMP1)

Bits	7	6	5	4	3	2	1	0
Field	INPSEL	INNSEL	REFLVL				TIMTRG	
Reset	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F91H							

Bit	Description
[7] INPSEL	**Signal Select for Positive Input** 0 = GPIO pin used as positive comparator 1 input. 1 = Temperature sensor used as positive comparator 1 input.
[6] INNSEL	**Signal Select for Negative Input** 0 = Internal reference disabled, GPIO pin used as negative comparator 1 input. 1 = Internal reference enabled as negative comparator 1 input.

Table 147. Trim Option Bits at 0001H (TTEMP1)

Bits	7	6	5	4	3	2	1	0
Field	TS_NEG				TS_COARSE			
Reset	1	0	1	0	0	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0021H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:4] TS_NEG	**Temperature Sensor Negative Control Trim Bits** Negative control offset trimming bits for the Temperature Sensor.
[3:0] TS_COARSE	**Temperature Sensor Coarse Control Trim Bits** Contains coarse control offset trimming bits for the Temperature Sensor.

21.2.4.2. Trim Bit Address 0002H

The Trim Option Bits Register at address 0002H, shown in Table 148, governs control of the Internal Precision Oscillator trim bits.

Table 148. Trim Option Bits at 0002H (TIPO)

Bits	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
Reset	U							
R/W	R/W							
Address	Information Page Memory 0022H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0] IPO_TRIM	**Internal Precision Oscillator Trim Byte** Contains trimming bits for Internal Precision Oscillator.

Table 184. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	—	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Table 185. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

Table 186. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
AND dst, src	dst ← dst AND src	r	r	52	–	*	*	0	–	–	2	3
		r	Ir	53							2	4
		R	R	54							3	3
		R	IR	55							3	4
		R	IM	56							3	3
		IR	IM	57							3	4
ANDX dst, src	dst ← dst AND src	ER	ER	58	–	*	*	0	–	–	4	3
		ER	IM	59							4	3
ATM	Block all interrupt and DMA requests during execution of the next 3 instructions			2F	–	–	–	–	–	–	1	2
BCLR bit, dst	dst[bit] ← 0	r		E2	–	*	*	0	–	–	2	2
BIT p, bit, dst	dst[bit] ← p	r		E2	–	*	*	0	–	–	2	2
BRK	Debugger Break			00	–	–	–	–	–	–	1	1
BSET bit, dst	dst[bit] ← 1	r		E2	–	*	*	0	–	–	2	2
BSWAP dst	dst[7:0] ← dst[0:7]	R		D5	X	*	*	0	–	–	2	2
BTJ p, bit, src, dst	if src[bit] = p PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4
BTJNZ bit, src, dst	if src[bit] = 1 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4
BTJZ bit, src, dst	if src[bit] = 0 PC ← PC + X		r	F6	–	–	–	–	–	–	3	3
			Ir	F7							3	4
CALL dst	SP ← SP -2 @SP ← PC PC ← dst	IRR		D4	–	–	–	–	–	–	2	6
		DA		D6							3	3
CCF	C ← ~C			EF	*	–	–	–	–	–-	1	2

Flags notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 196. Analog-to-Digital Converter Electrical Characteristics and Timing

		T_A = 0°C to +70°C T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
N	Resolution	–	10	–	Bit	
INL	Integral Nonlinearity	–5		5	LSB	
DNL	Differential Nonlinearity	–1		4	LSB	
	Gain Error		15		LSB	
	Offset Error	–15		15	LSB	PDIP package
		–9		9	LSB	Other packages
I_{DD}ADC	ADC Active Current	–	–	2.5	mA	
I_{DDQ}ADC	ADC Quiescent Current	–	5	–	nA	
V_{INT_REF}	Internal Reference Voltage	–	1.6	–	V	REFEN=1, INTREF_SEL=0. See Table 101 on page 189.
		–	AVDD	–	V	REFEN=1, INTREF_SEL=1. See Table 101 on page 189.
V_{EXT_REF}	External Reference Voltage	1.6	–	90% AV_{DD}	V	REFEN=0. See Table 101 on page 189.
V_{INANA}	Analog Input Range	0	–	1.6	V	Internal reference = 1.6V
		0	–	90% AV_{DD}	V	External reference or use AVDD as internal reference
C_{IN}	Analog Input Load	–	–	5	pF	
T_S	Sample Time	1.8	–	–	µs	
T_H	Hold Time	0.5	–	–	µs	
T_{CONV}	Conversion Time	–	13	–	clock cycles	
GBW_{IN}	Input Bandwidth	–	200	–	kHz	
T_{WAKE}	Wake-up Time	–	–	10	µs	External reference
		–	–	10	µs	Internal reference
f_{ADC_CLK}	Maximum Frequency of adc_clk	–	–	5	MHz	V_{DD} = 2.7V to 3.6V
		–	–	2.5	MHz	V_{DD} = 1.8V to 2.7V

29.4.3. On-Chip Debugger Timing

Figure 77 and Table 206 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4ns maximum rise and fall time.

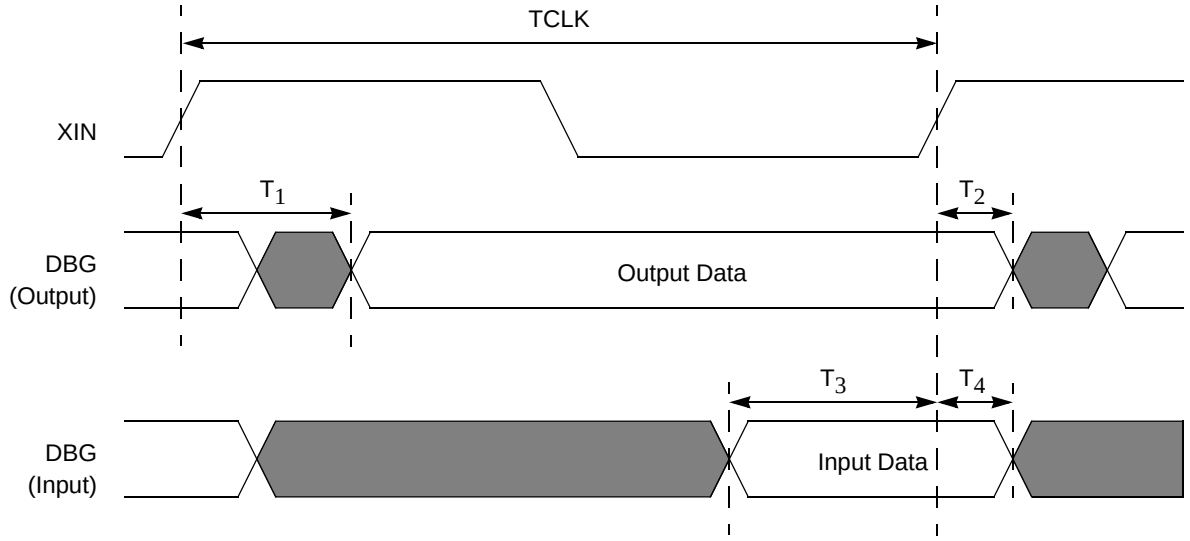

Figure 77. On-Chip Debugger Timing

Table 206. On-Chip Debugger Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Min**	**Max**
DBG			
T_1	X_{IN} Rise to DBG Valid Delay	–	15
T_2	X_{IN} Rise to DBG Output Hold Time	2	–
T_3	DBG to XIN Rise Input Setup Time	5	–
T_4	DBG to XIN Rise Input Hold Time	5	–