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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny828r-au

- Low Power Consumption
  - Active Mode: 0.2 mA at 1.8V and 1MHz
  - Idle Mode: 30 µA at 1.8V and 1MHz
  - Power-Down Mode (WDT Enabled): 1 µA at 1.8V
  - Power-Down Mode (WDT Disabled): 100 nA at 1.8V

1. Pin Configurations

Figure 1. ATtiny828 Pinout in MLF32.

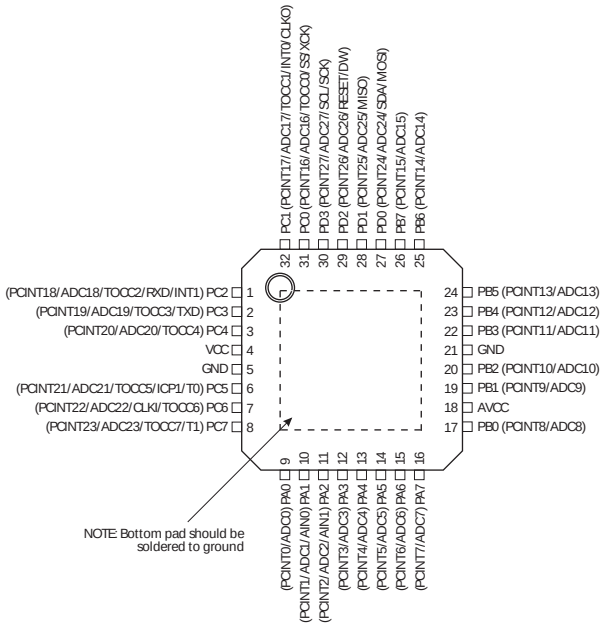
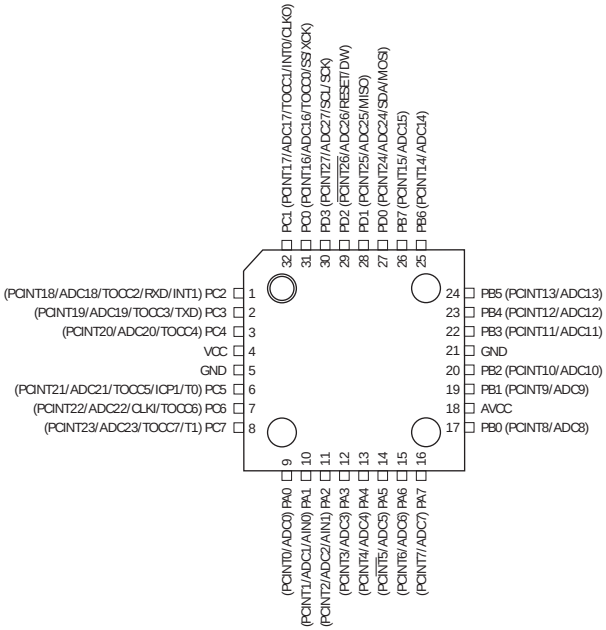


Figure 2. ATtiny828 Pinout in TQFP32.



Writing a logic one to this bit shuts down the Timer/Counter0 module. When the Timer/Counter0 is enabled, operation will continue like before the shutdown.

- **Bit 3 – PRTIM1: Power Reduction Timer/Counter1**

Writing a logic one to this bit shuts down the Timer/Counter1 module. When the Timer/Counter1 is enabled, operation will continue like before the shutdown.

- **Bit 2 – PRSPI: Power Reduction SPI**

Writing a logic one to this bit shuts down the SPI by stopping the clock to the module. When waking up the SPI again, the SPI should be re-initialized to ensure proper operation.

- **Bit 1 – PRUSART0: Power Reduction USART0**

Writing a logic one to this bit shuts down the USART0 module. When the USART0 is enabled, operation will continue like before the shutdown.

- **Bit 0 – PRADC: Power Reduction ADC**

Writing a logic one to this bit shuts down the ADC. The ADC must be disabled before shut down. The analog comparator cannot be used when the ADC is shut down.

Pin	Signal	Composition
PB6	PUOE	0
	PUOV	0
	DDOE	0
	DDOV	0
	PVOE	0
	PVOV	0
	PTOE	0
	DIEOE	(PCINT14 • PCIE1) + ADC14D
	DIEOV	PCINT14 • PCIE1
	DI	PCINT14 Input
	AIO	ADC14 Input
PB7	PUOE	0
	PUOV	0
	DDOE	0
	DDOV	0
	PVOE	0
	PVOV	0
	PTOE	0
	DIEOE	(PCINT15 • PCIE1) + ADC15D
	DIEOV	PCINT15 • PCIE1
	DI	PCINT15 Input
	AIO	ADC15 Input

10.3.3 Alternative Functions of Port C

The alternative functions of port C are shown in Table 25.

Table 25. Alternative Functions of Port C

Pin	Function	Description of Alternative Function
PC0	PCINT16	Pin change interrupt source
	ADC16	Input channel for analog to digital converter (ADC)
	TOCC0	Timer/counter output compare, channel 0 (1)
	SS	SPI Slave Select input (2)
	XCK	USART transfer clock

2. When SPI is enabled as a slave, this pin is automatically configured as an input, regardless of the data direction bit of the pin. When SPI is enabled as a master normal pin control of data direction is resumed.
3. When the CKOUT fuse is programmed, the system clock is output on this pin, regardless of pin settings. The clock is also output when the device is reset.

Table 26, below, summarises the override signals used by the alternative functions of the port. For an illustration on how signals are used, see Figure 25 on page 64.

Table 26. Override Signals of Port C

Pin	Signal	Composition
PC0	PUOE	0
	PUOV	0
	DDOE	SPE • $\overline{\text{MSTR}}$
	DDOV	0
	PVOE	TOCC0OE + XCK_MASTER (1)
	PVOV	XCK_MASTER • XCK_OUT + $\overline{\text{XCK\_MASTER}}$ • TOCC0_OUT
	PTOE	0
	DIEOE	(PCINT16 • PCIE2) + ADC16D + (XCK_SLAVE(2) • RXEN • SFDE)
	DIEOV	(PCINT16 • PCIE2) + (XCK_SLAVE(2) • RXEN • SFDE)
	DI	PCINT16 Input / XCK_IN / $\overline{\text{SS}}$ Input
	AIO	ADC16 Input
PC1	PUOE	0
	PUOV	0
	DDOE	CKOUT(3)
	DDOV	CKOUT(3)
	PVOE	0TOCC1E + CKOUT(3)
	PVOV	CKOUT(3) • SYSTEM_CLOCK + $\overline{\text{CKOUT}}$ • TOCC1_OUT
	PTOE	0
	DIEOE	(PCINT17 • PCIE2) + ADC17D + INT0
	DIEOV	PCINT17 • PCIE2 + INT0
	DI	PCINT17 Input / INT0 Input
	AIO	ADC17 Input

A change of the COM0x[1:0] bits state will have effect at the first Compare Match after the bits are written. For non-PWM modes, the action can be forced to have immediate effect by using the Force Output Compare bits. See “TCCR0B – Timer/Counter Control Register B” on page 100.

11.7 Modes of Operation

The mode of operation, i.e., the behavior of the Timer/Counter and the Output Compare pins, is defined by the combination of the Waveform Generation mode (WGM[2:0]) and Compare Output mode (COM0x[1:0]) bits. The Compare Output mode bits do not affect the counting sequence, while the Waveform Generation mode bits do. The COM0x[1:0] bits control whether the PWM output generated should be inverted or not (inverted or non-inverted PWM). For non-PWM modes the COM0x[1:0] bits control whether the output should be set, cleared, or toggled at a Compare Match (See “Modes of Operation” on page 92).

For detailed timing information refer to Figure 33 on page 96, Figure 34 on page 96, Figure 35 on page 97 and Figure 36 on page 97 in “Timer/Counter Timing Diagrams” on page 96.

11.7.1 Normal Mode

The simplest mode of operation is the Normal mode (WGM0[2:0] = 0). In this mode the counting direction is always up (incrementing), and no counter clear is performed. The counter simply overruns when it passes its maximum 8-bit value (TOP = 0xFF) and then restarts from the bottom (0x00). In normal operation the Timer/Counter Overflow Flag (TOV0) will be set in the same timer clock cycle as the TCNT0 becomes zero. The TOV0 Flag in this case behaves like a ninth bit, except that it is only set, not cleared. However, combined with the timer overflow interrupt that automatically clears the TOV0 Flag, the timer resolution can be increased by software. There are no special cases to consider in the Normal mode, a new counter value can be written anytime.

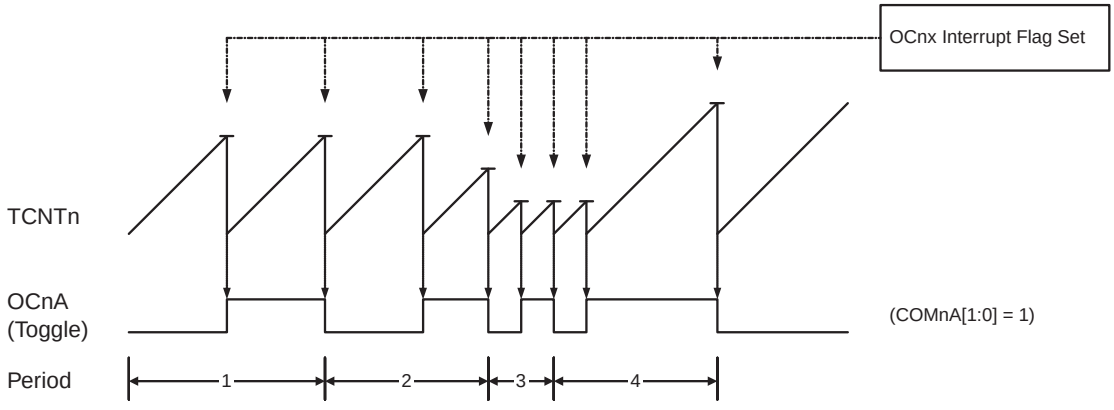
The Output Compare Unit can be used to generate interrupts at some given time. Using the Output Compare to generate waveforms in Normal mode is not recommended, since this will occupy too much of the CPU time.

11.7.2 Clear Timer on Compare Match (CTC) Mode

In Clear Timer on Compare or CTC mode (WGM0[2:0] = 2), the OCR0A Register is used to manipulate the counter resolution. In CTC mode the counter is cleared to zero when the counter value (TCNT0) matches the OCR0A. The OCR0A defines the top value for the counter, hence also its resolution. This mode allows greater control of the Compare Match output frequency. It also simplifies the operation of counting external events.

The timing diagram for the CTC mode is shown in Figure 30 on page 92. The counter value (TCNT0) increases until a Compare Match occurs between TCNT0 and OCR0A, and then counter (TCNT0) is cleared.

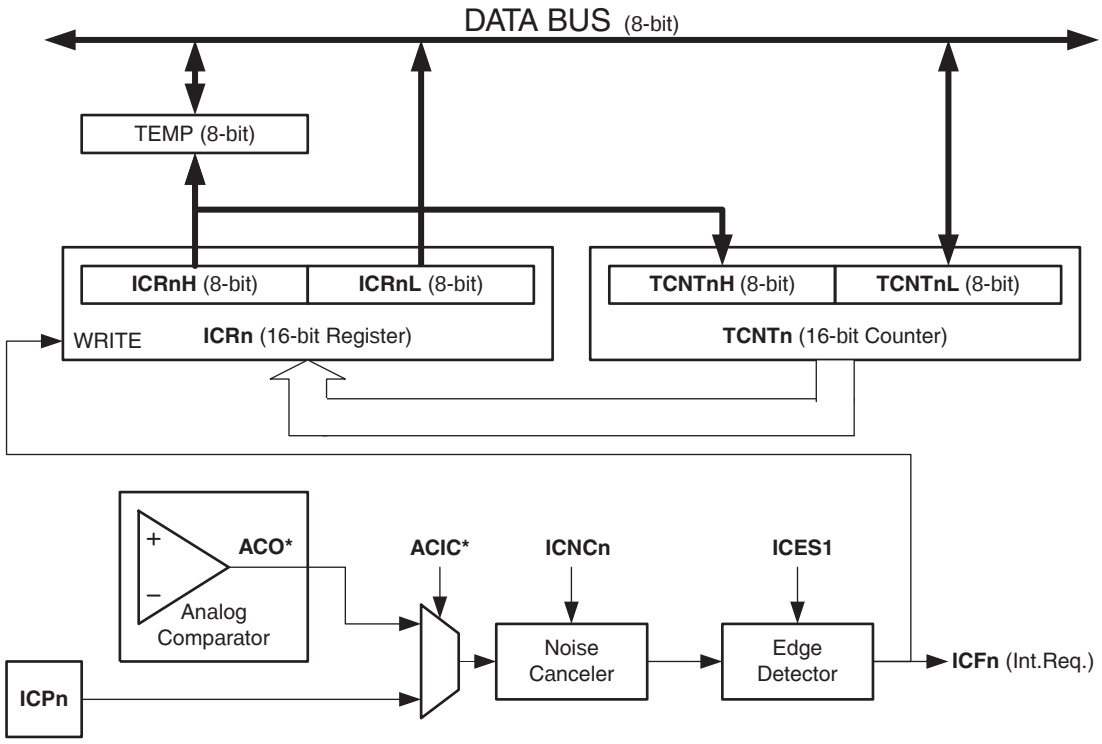
Figure 30. CTC Mode, Timing Diagram



An interrupt can be generated each time the counter value reaches the TOP value by using the OCF0A Flag. If the interrupt is enabled, the interrupt handler routine can be used for updating the TOP value. However, changing TOP to a value close to BOTTOM when the counter is running with none or a low prescaler value must be done with care since the

or alternatively, via the analog-comparator unit. The time-stamps can then be used to calculate frequency, duty-cycle, and other features of the signal applied. Alternatively the time-stamps can be used for creating a log of the events.

Figure 39. Input Capture Unit Block Diagram



The Input Capture unit is illustrated by the block diagram shown in Figure 39. The elements of the block diagram that are not directly a part of the Input Capture unit are gray shaded. The small “n” in register and bit names indicates the Timer/Counter number.

When a change of the logic level (an event) occurs on the Input Capture pin (ICP1), alternatively on the Analog Comparator output (ACO), and this change confirms to the setting of the edge detector, a capture will be triggered. When a capture is triggered, the 16-bit value of the counter (TCNT1) is written to the Input Capture Register (ICR1). The Input Capture Flag (ICF1) is set at the same system clock as the TCNT1 value is copied into ICR1 Register. If enabled (ICIE1 = 1), the Input Capture Flag generates an Input Capture interrupt. The ICF1 flag is automatically cleared when the interrupt is executed. Alternatively the ICF1 flag can be cleared by software by writing a logical one to its I/O bit location.

Reading the 16-bit value in the Input Capture Register (ICR1) is done by first reading the low byte (ICR1L) and then the high byte (ICR1H). When the low byte is read the high byte is copied into the high byte temporary register (TEMP). When the CPU reads the ICR1H I/O location it will access the TEMP Register.

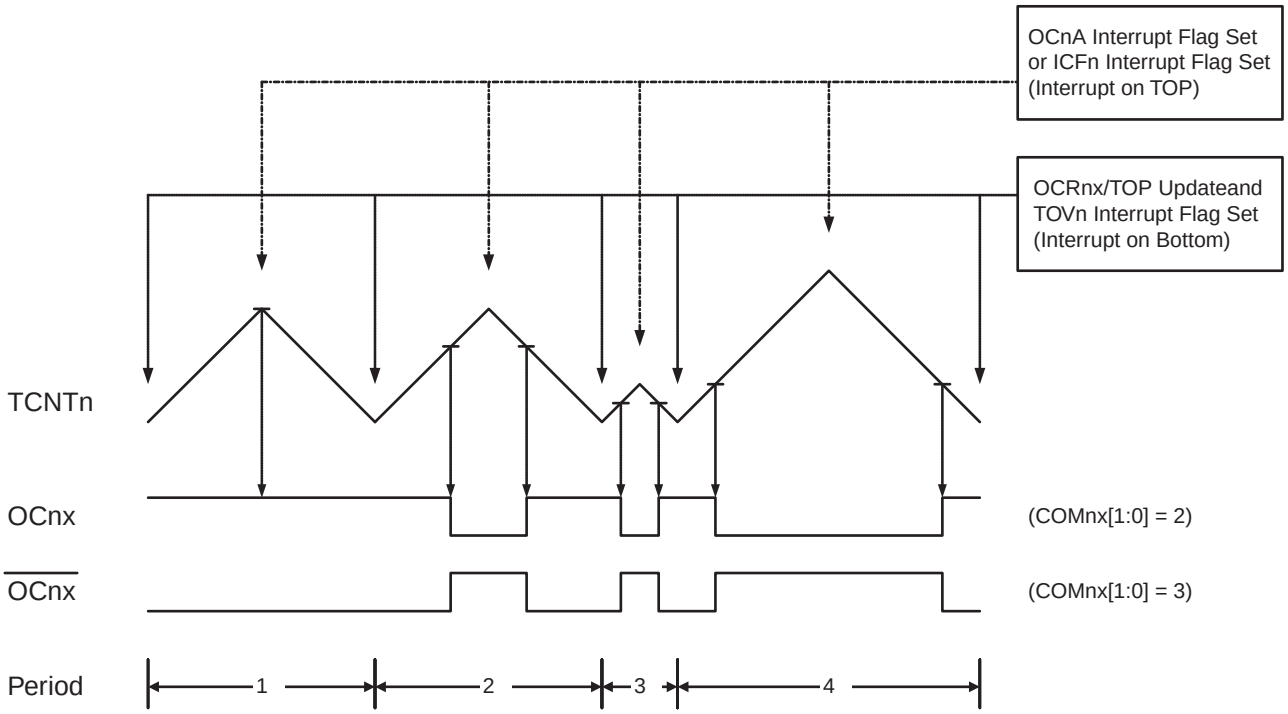
The ICR1 Register can only be written when using a Waveform Generation mode that utilizes the ICR1 Register for defining the counter’s TOP value. In these cases the Waveform Generation mode (WGM1[3:0]) bits must be set before the TOP value can be written to the ICR1 Register. When writing the ICR1 Register the high byte must be written to the ICR1H I/O location before the low byte is written to ICR1L.

For more information on how to access the 16-bit registers refer to “Accessing 16-bit Registers” on page 120.

12.5.1 Input Capture Trigger Source

The main trigger source for the Input Capture unit is the Input Capture pin (ICP1). Timer/Counter1 can alternatively use the Analog Comparator output as trigger source for the Input Capture unit. The Analog Comparator is selected as trigger source by setting the Analog Comparator Input Capture (ACIC) bit in the Analog Comparator Control and Status Register (ACSR). Be aware that changing trigger source can trigger a capture. The Input Capture Flag must therefore be cleared after the change.

Figure 45. Phase and Frequency Correct PWM Mode, Timing Diagram



The Timer/Counter Overflow Flag (TOV1) is set at the same timer clock cycle as the OCR1x Registers are updated with the double buffer value (at BOTTOM). When either OCR1A or ICR1 is used for defining the TOP value, the OC1A or ICF1 flag set when TCNT1 has reached TOP. The interrupt flags can then be used to generate an interrupt each time the counter reaches the TOP or BOTTOM value.

When changing the TOP value the program must ensure that the new TOP value is higher or equal to the value of all of the Compare Registers. If the TOP value is lower than any of the Compare Registers, a compare match will never occur between the TCNT1 and the OCR1x.

As Figure 45 shows the output generated is, in contrast to the phase correct mode, symmetrical in all periods. Since the OCR1x Registers are updated at BOTTOM, the length of the rising and the falling slopes will always be equal. This gives symmetrical output pulses and is therefore frequency correct.

Using the ICR1 Register for defining TOP works well when using fixed TOP values. By using ICR1, the OCR1A Register is free to be used for generating a PWM output on OC1A. However, if the base PWM frequency is actively changed by changing the TOP value, using the OCR1A as TOP is clearly a better choice due to its double buffer feature.

In phase and frequency correct PWM mode, the compare units allow generation of PWM waveforms on the OC1x pins. Setting the COM1x[1:0] bits to two will produce a non-inverted PWM and an inverted PWM output can be generated by setting the COM1x[1:0] to three (See Table 41 on page 124). The actual OC1x value will only be visible on the port pin if the data direction for the port pin is set as output (DDR_OC1x). The PWM waveform is generated by setting (or clearing) the OC1x Register at the compare match between OCR1x and TCNT1 when the counter increments, and clearing (or setting) the OC1x Register at compare match between OCR1x and TCNT1 when the counter decrements. The PWM frequency for the output when using phase and frequency correct PWM can be calculated by the following equation:

$$f_{OCnxPFCPWM} = \frac{f_{clk\_I/O}}{2 \cdot N \cdot TOP}$$

The N variable represents the prescaler divider (1, 8, 64, 256, or 1024).

The extreme values for the OCR1x Register represents special cases when generating a PWM waveform output in the phase correct PWM mode. If the OCR1x is set equal to BOTTOM the output will be continuously low and if set equal to

- **Bits 1:0 – WGM1[1:0]: Waveform Generation Mode**

Combined with the WGM1[3:2] bits found in the TCCR1B Register, these bits control the counting sequence of the counter, the source for maximum (TOP) counter value, and what type of waveform generation to be used, see Table 42. Modes of operation supported by the Timer/Counter unit are: Normal mode (counter), Clear Timer on Compare match (CTC) mode, and three types of Pulse Width Modulation (PWM) modes. (“Modes of Operation” on page 111).

Table 42. Waveform Generation Modes

Mode	WGM1[3:0]	Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
0	0000	Normal	0xFFFF	Immediate	MAX
1	0001	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0010	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0011	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0100	CTC (Clear Timer on Compare)	OCR1A	Immediate	MAX
5	0101	Fast PWM, 8-bit	0x00FF	TOP	TOP
6	0110	Fast PWM, 9-bit	0x01FF	TOP	TOP
7	0111	Fast PWM, 10-bit	0x03FF	TOP	TOP
8	1000	PWM, Phase & Freq. Correct	ICR1	BOTTOM	BOTTOM
9	1001	PWM, Phase & Freq. Correct	OCR1A	BOTTOM	BOTTOM
10	1010	PWM, Phase Correct	ICR1	TOP	BOTTOM
11	1011	PWM, Phase Correct	OCR1A	TOP	BOTTOM
12	1100	CTC (Clear Timer on Compare)	ICR1	Immediate	MAX
13	1101	(Reserved)	–	–	–
14	1110	Fast PWM	ICR1	TOP	TOP
15	1111	Fast PWM	OCR1A	TOP	TOP

12.11.2 TCCR1B – Timer/Counter1 Control Register B

Bit	7	6	5	4	3	2	1	0	
(0x81)	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ICNC1: Input Capture Noise Canceler**

Setting this bit (to one) activates the Input Capture Noise Canceler. When the noise canceler is activated, the input from the Input Capture pin (ICP1) is filtered. The filter function requires four successive equal valued samples of the ICP1 pin for changing its output. The Input Capture is therefore delayed by four Oscillator cycles when the noise canceler is enabled.

12.11.3 TCCR1C – Timer/Counter1 Control Register C

Bit	7	6	5	4	3	2	1	0	
(0x82)	FOC1A	FOC1B	–	–	–	–	–	–	TCCR1C
Read/Write	W	W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – FOC1A: Force Output Compare for Channel A**
- **Bit 6 – FOC1B: Force Output Compare for Channel B**

The FOC1A/FOC1B bits are only active when the WGM1[3:0] bits specifies a non-PWM mode. However, for ensuring compatibility with future devices, these bits must be set to zero when TCCR1A is written when operating in a PWM mode. When writing a logical one to the FOC1A/FOC1B bit, an immediate compare match is forced on the Waveform Generation unit. The OC1A/OC1B output is changed according to its COM1x[1:0] bits setting. Note that the FOC1A/FOC1B bits are implemented as strobes. Therefore it is the value present in the COM1x[1:0] bits that determine the effect of the forced compare.

A FOC1A/FOC1B strobe will not generate any interrupt nor will it clear the timer in Clear Timer on Compare match (CTC) mode using OCR1A as TOP.

The FOC1A/FOC1B bits are always read as zero.

- **Bits 5:0 – Res: Reserved Bit**

These bits are reserved for future use. To ensure compatibility with future devices, these bits must be set to zero when the register is written.

12.11.4 TOCPMSA1 and TOCPMSA0 – Timer/Counter Output Compare Pin Mux Selection Registers

Bit	7	6	5	4	3	2	1	0	
(0xE9)	TOCC7S1	TOCC7S0	TOCC6S1	TOCC6S0	TOCC5S1	TOCC5S0	TOCC4S1	TOCC4S0	TOCPMSA1
(0xE8)	TOCC3S1	TOCC3S0	TOCC2S1	TOCC2S0	TOCC1S1	TOCC1S0	TOCC0S1	TOCC0S0	TOCPMSA0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7:0 – TOCCnS1 and TOCCnS0: Timer/Counter Output Compare Channel Select**

TOCCnS1 and TOCCnS bits select which Timer/Counter compare output is routed to the corresponding TOCCn pin. The two timer/counters provide four possible compare outputs that can be routed to output pins, as shown in the table below.

Table 44. Selecting Timer/Counter Compare Output for TOCCn Pins

TOCCnS1	TOCCnS0	TOCCn Output (1)
0	0	OC0A
0	1	OC0B
1	0	OC1A
1	1	OC1B

Note: 1. See “Alternative Functions of Port C” on page 73.

12.11.11TIFR1 – Timer/Counter Interrupt Flag Register

Bit	7	6	5	4	3	2	1	0	
0x16 (0x36)	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	TIFR1
Read/Write	R	R	R/W	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7, 6, 4, 3 – Res: Reserved Bit**

These bits are reserved for future use. To ensure compatibility with future devices, these bits must be set to zero when the register is written.

- **Bit 5 – ICF1: Timer/Counter1, Input Capture Flag**

This flag is set when a capture event occurs on the ICP1 pin. When the Input Capture Register (ICR1) is set by the WGM1[3:0] to be used as the TOP value, the ICF1 flag is set when the counter reaches the TOP value.

ICF1 is automatically cleared when the Input Capture Interrupt Vector is executed. Alternatively, ICF1 can be cleared by writing a logic one to its bit location.

- **Bit 2 – OCF1B: Timer/Counter1, Output Compare B Match Flag**

This flag is set in the timer clock cycle after the counter (TCNT1) value matches the Output Compare Register B (OCR1B).

Note that a Forced Output Compare (1B) strobe will not set the OCF1B flag.

OCF1B is automatically cleared when the Output Compare Match B Interrupt Vector is executed. Alternatively, OCF1B can be cleared by writing a logic one to its bit location.

- **Bit 1 – OCF1A: Timer/Counter1, Output Compare A Match Flag**

This flag is set in the timer clock cycle after the counter (TCNT1) value matches the Output Compare Register A (OCR1A).

Note that a Forced Output Compare (1A) strobe will not set the OCF1A flag.

OCF1A is automatically cleared when the Output Compare Match A Interrupt Vector is executed. Alternatively, OCF1A can be cleared by writing a logic one to its bit location.

- **Bit 0 – TOV1: Timer/Counter1, Overflow Flag**

The setting of this flag is dependent of the WGM1[3:0] bits setting. In Normal and CTC modes, the TOV1 flag is set when the timer overflows. See Table 42 on page 125 for the TOV1 flag behavior when using another WGM1[3:0] bit setting.

TOV1 is automatically cleared when the Timer/Counter1 Overflow Interrupt Vector is executed. Alternatively, TOV1 can be cleared by writing a logic one to its bit location.

Table 56. SPI Modes

SPI Mode	Conditions	Leading Edge	Trailing eDge
0	CPOL=0, CPHA=0	Sample (Rising)	Setup (Falling)
1	CPOL=0, CPHA=1	Setup (Rising)	Sample (Falling)
2	CPOL=1, CPHA=0	Sample (Falling)	Setup (Rising)
3	CPOL=1, CPHA=1	Setup (Falling)	Sample (Rising)

16.5 Register Description

16.5.1 SPCR – SPI Control Register

Bit	7	6	5	4	3	2	1	0	
0x2C (0x4C)	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – SPIE: SPI Interrupt Enable**

When this bit is set, the SPI interrupt is enabled. Provided the Global Interrupt Enable bit in SREG is set, the SPI interrupt service routine will be executed when the SPIF bit in SPSR is set.

- **Bit 6 – SPE: SPI Enable**

When this bit is set, the SPI is enabled. This bit must be set to enable any SPI operations.

- **Bit 5 – DORD: Data Order**

When this bit is set, the LSB of the data word is transmitted first.

When this bit is cleared, the MSB of the data word is transmitted first.

- **Bit 4 – MSTR: Master/Slave Select**

This bit selects Master SPI mode when written to one, and Slave SPI mode when written logic zero. If $\overline{SS}$ is configured as an input and is driven low while MSTR is set, MSTR will be cleared, and SPIF in SPSR will become set. The user will then have to set MSTR to re-enable SPI Master mode.

- **Bit 3 – CPOL: Clock Polarity**

When this bit is set, SCK is high when idle. When this bit is cleared, SCK is low when idle. Refer to Figure 68 and Figure 69 for an example. The CPOL functionality is summarized below:

Table 57. CPOL Functionality

CPOL	Leading Edge	Trailing Edge
0	Rising	Falling
1	Falling	Rising

- **Bit 4 – RXEN: Receiver Enable**

Writing this bit to one enables the USART Receiver in MSPIM mode. The receiver will override normal port operation for the RxD pin when enabled. Disabling the receiver will flush the receive buffer. Only enabling the receiver in MSPI mode (i.e. setting RXEN=1 and TXEN=0) has no meaning since it is the transmitter that controls the transfer clock and since only master mode is supported.

- **Bit 3 – TXEN: Transmitter Enable**

Writing this bit to one enables the USART Transmitter. The transmitter will override normal port operation for the TxD pin when enabled. The disabling of the transmitter (writing TXEN to zero) will not become effective until ongoing and pending transmissions are completed, i.e., when the transmit shift register and transmit buffer register do not contain data to be transmitted. When disabled, the transmitter will no longer override the TxD port.

- **Bits 2:0 – Reserved Bits in MSPI mode**

When in MSPI mode, these bits are reserved for future use. For compatibility with future devices, these bits must be written to zero when UCSRB is written.

18.8.4 UCSRC – USART MSPIM Control and Status Register C

Bit	7	6	5	4	3	2	1	0	
(0xC2)	UMSEL1	UMSEL0	-	-	-	UDORD	UCPHA	UCPOL	UCSRC
Read/Write	R/W	R/W	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	1	1	0	

- **Bits 7:6 – UMSEL[1:0]: USART Mode Select**

These bits select the mode of operation of the USART as shown in Table 76. See “UCSRC – USART Control and Status Register C” on page 186 for full description of the normal USART operation. The MSPIM is enabled when both UMSEL bits are set to one. The UDORD, UCPHA, and UCPOL can be set in the same write operation where the MSPIM is enabled.

Table 76. UMSEL Bits Settings

UMSEL1	UMSEL0	Mode
0	0	Asynchronous USART
0	1	Synchronous USART
1	0	(Reserved)
1	1	Master SPI (MSPIM)

- **Bits 5:3 – Reserved Bits in MSPI mode**

When in MSPI mode, these bits are reserved for future use. For compatibility with future devices, these bits must be written to zero when UCSRC is written.

- **Bit 2 – UDORD: Data Order**

When set to one the LSB of the data word is transmitted first. When set to zero the MSB of the data word is transmitted first. See “Frame Formats” on page 191 for details.

Table 82. Setting the Size of Application and Boot Loader Sections

BOOTSZ1	BOOTSZ0	Application Section		Boot Loader Section		
		Start	End	Start [1]	End	Size (words)
0	0	0x000	0xBFF	0xC00	0xFFF	1024
0	1		0xDFF	0xE00		512
1	0		0xEFF	0xF00		256
1	1		0xF7F	0xF80		128

Note: 1. Start of boot loader section = boot reset address.

Boot Loader Section options are illustrated in Figure 91, below.

Figure 91. Flash Memory Sections vs. BOOTSZ Fuse Bits.

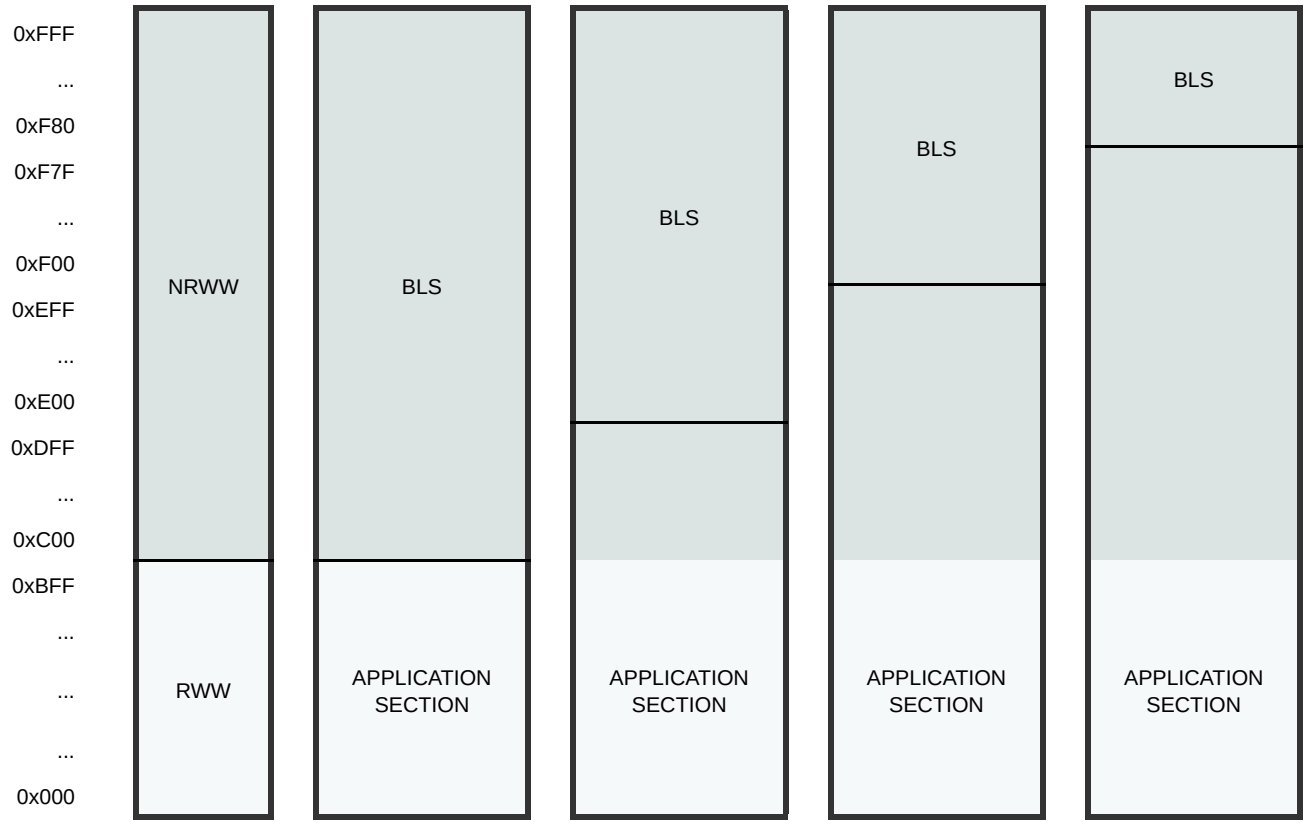
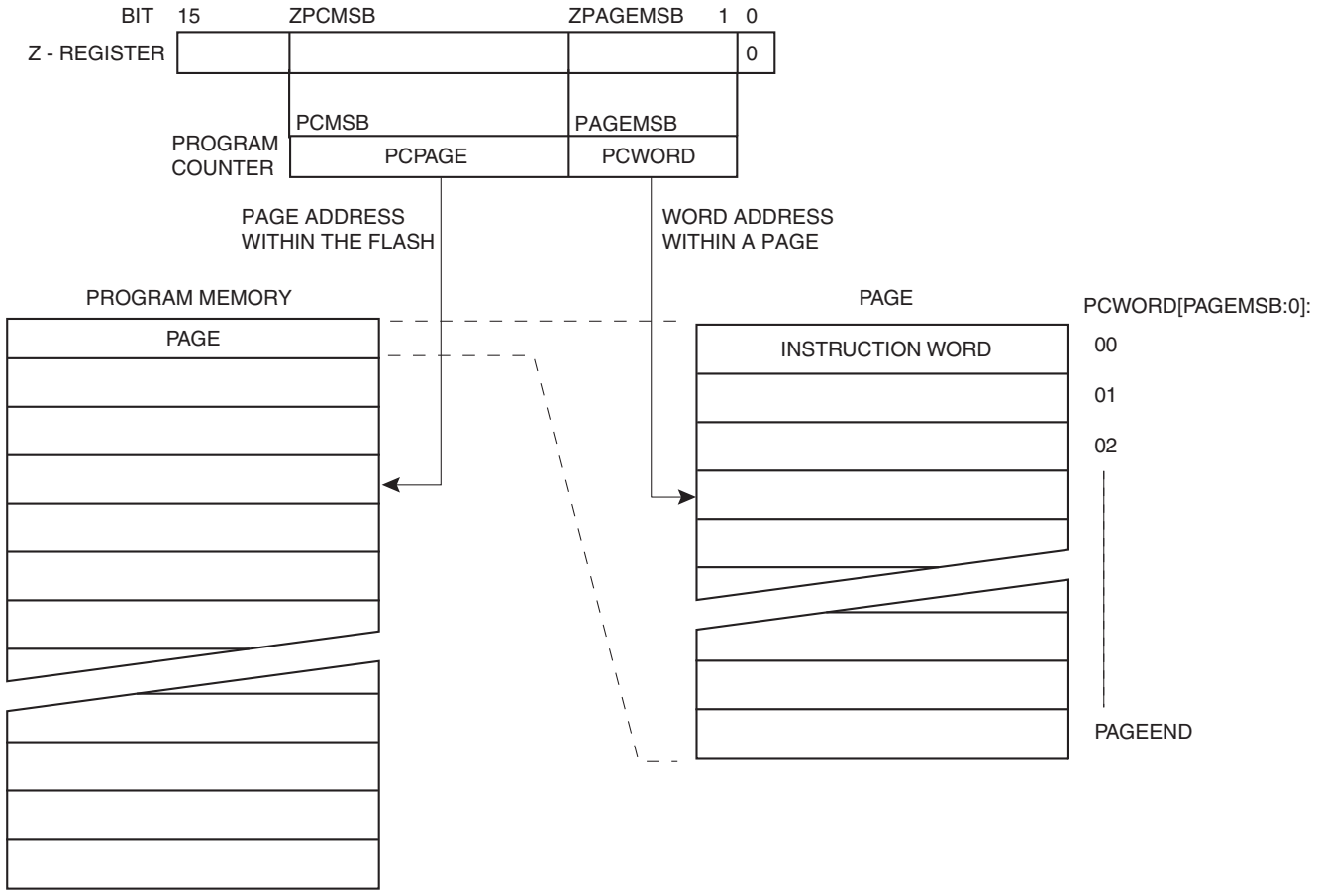


Figure 92. Addressing the Flash During SPM



Variables used in Figure 92 are explained in Table 83, below.

Table 83. Variables Used in Flash Addressing

Variable	Description
PCPAGE	Program Counter page address. Selects page of words and is used with Page Erase and Page Write operations. See Table 94 on page 232
PCMSB	The most significant bit of the Program Counter. See Table 94 on page 232
ZPCMSB	The bit in the Z register that is mapped to PCMSB. Because Z[0] is not used, ZPCMSB = PCMSB + 1. Z register bits above ZPCMSB are ignored
PCWORD	Program Counter word address. Selects the word within a page. This is used for filling the temporary buffer and must be zero during page write operations. See Table 94 on page 232
PAGEMSB	The most significant bit used to address the word within one page
ZPAGEMSB	The bit in the Z register that is mapped to PAGEMSB. Because Z[0] is not used, ZPAGEMSB = PAGEMSB + 1

Note that the Page Erase and Page Write operations are addressed independently. Therefore, it is very important that the boot loader addresses the same page in both Page Erase and Page Write operations.

Table 98. XA1 and XA0 Coding

XA1	XA0	Action when CLKI is Pulsed
0	0	Load Flash or EEPROM address (high or low address byte, determined by BS1)
0	1	Load data (high or low data byte for Flash, determined by BS1)
1	0	Load command
1	1	No action, idle

When pulsing $\overline{WR}$ or $\overline{OE}$, the command loaded determines the action executed. The different command options are shown in Table 99.

Table 99. Command Byte Bit Coding

Command Byte	Command
1000 0000	Chip Erase
0100 0000	Write fuse bits
0010 0000	Write lock bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read signature bytes and calibration byte
0000 0100	Read fuse and lock bits
0000 0010	Read Flash
0000 0011	Read EEPROM

23.2.1 Enter Programming Mode

The following algorithm puts the device in Parallel (High-voltage) Programming mode:

1. Set Prog_enable pins (see Table 97 on page 233) to “0000”, $\overline{RESET}$ pin to 0V and V_{CC} to 0V.
2. Apply 4.5 – 5.5V between V_{CC} and GND. Ensure that V_{CC} reaches at least 1.7V within the next 20 µs.
3. Wait 20 – 60 µs, and apply 11.5 – 12.5V to $\overline{RESET}$.
4. Keep the Prog_enable pins unchanged for at least 10µs after the high voltage has been applied to ensure Prog_enable signature has been latched.
5. Wait at least 300 µs before giving any parallel programming commands.
6. Exit programming mode by powering the device down or by bringing $\overline{RESET}$ pin to 0V.

If the rise time of the V_{CC} is unable to fulfill the requirements listed above, the following alternative algorithm can be used:

1. Set Prog_enable pins (Table 97 on page 233) to “0000”, $\overline{RESET}$ pin to 0V and V_{CC} to 0V.
2. Apply 4.5 – 5.5V between V_{CC} and GND.
3. Monitor V_{CC}, and as soon as V_{CC} reaches 0.9 – 1.1V, apply 11.5 – 12.5V to $\overline{RESET}$.
4. Keep the Prog_enable pins unchanged for at least 10µs after the high voltage has been applied to ensure Prog_enable signature has been latched.

24.9 Analog Comparator Characteristics

Table 113. Analog Comparator Characteristics, T = -40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{AIO}	Input Offset Voltage	V_{CC} = 5V, VIN = V_{CC} / 2		< 10	40	mV
I_{LAC}	Input Leakage Current	V_{CC} = 5V, VIN = V_{CC} / 2	-50		50	nA
t_{APD}	Analog Propagation Delay (from saturation to slight overdrive)	V_{CC} = 2.7V		750		ns
		V_{CC} = 4.0V		500		
	Analog Propagation Delay (large step change)	V_{CC} = 2.7V		100		
		V_{CC} = 4.0V		75		
t_{DPD}	Digital Propagation Delay	V_{CC} = 1.7V – 5.5		1	2	CLK

24.10 Parallel Programming Characteristics

Figure 104. Parallel Programming Timing, Including some General Timing Requirements

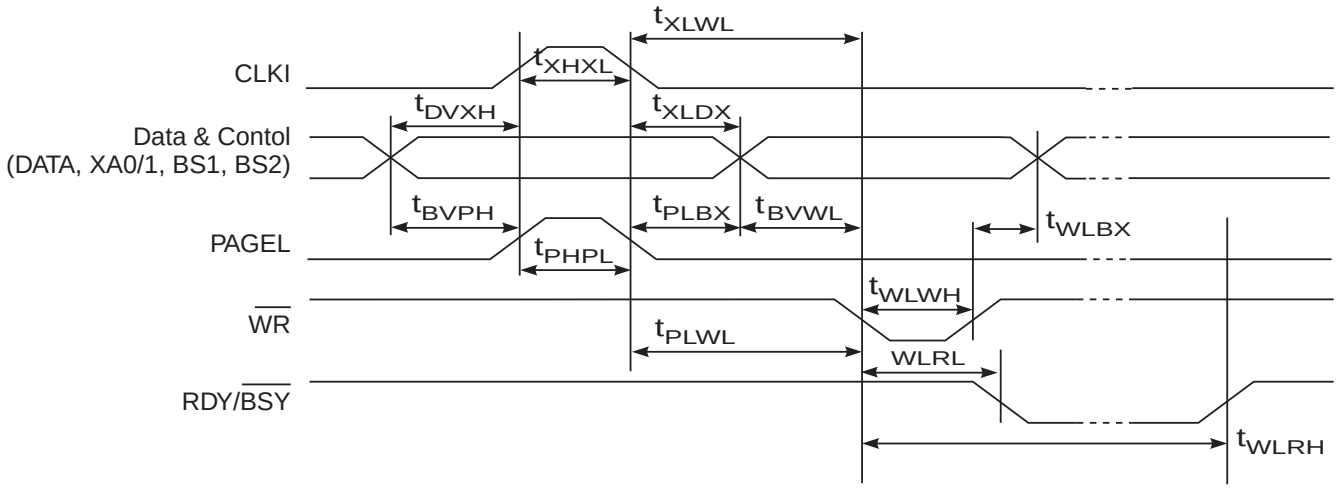
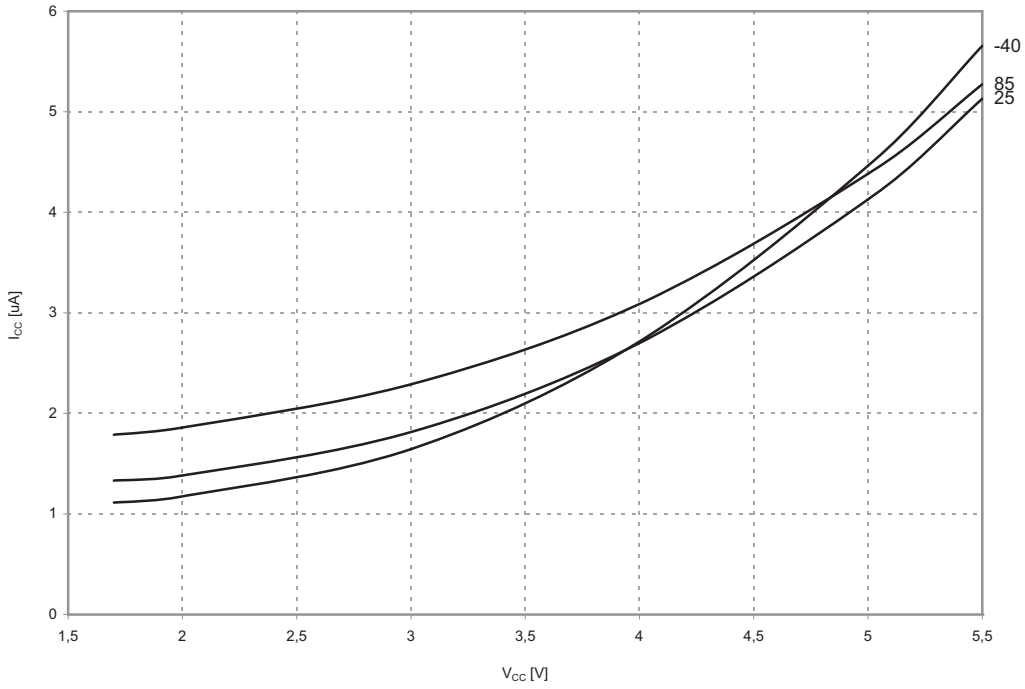
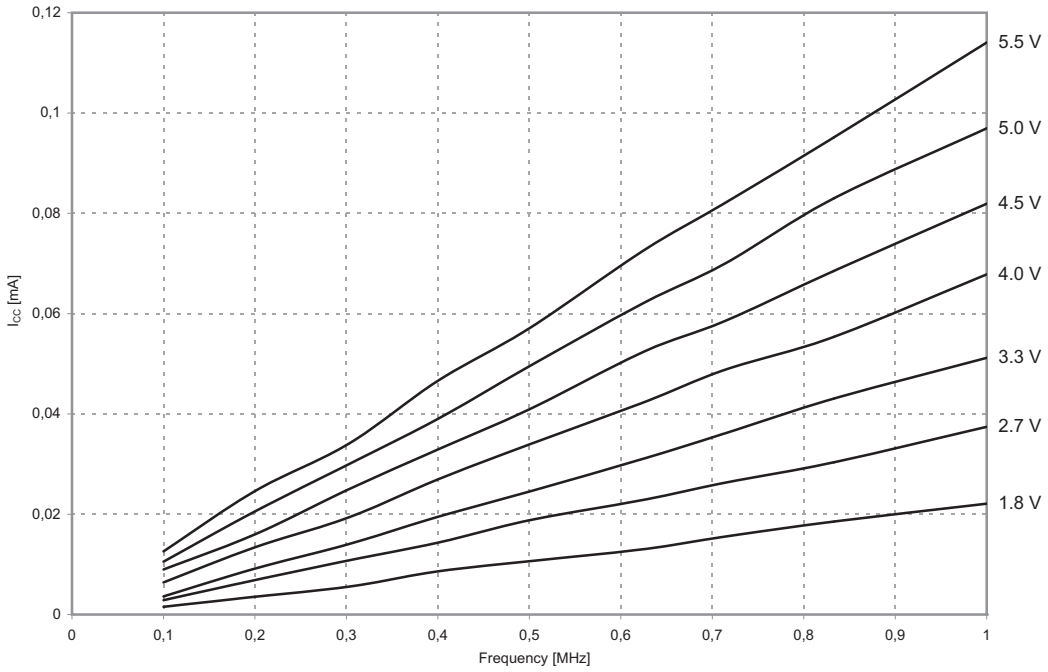


Figure 120. Power-down Supply Current vs. V_{CC} (Watchdog Timer Enabled)



25.4 Current Consumption in Reset

Figure 121. Reset Current vs. Frequency (0.1 – 1MHz, Excluding Pull-Up Current)



25.7.2 TWI Pins

Figure 138. V_{IH}: Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '1')

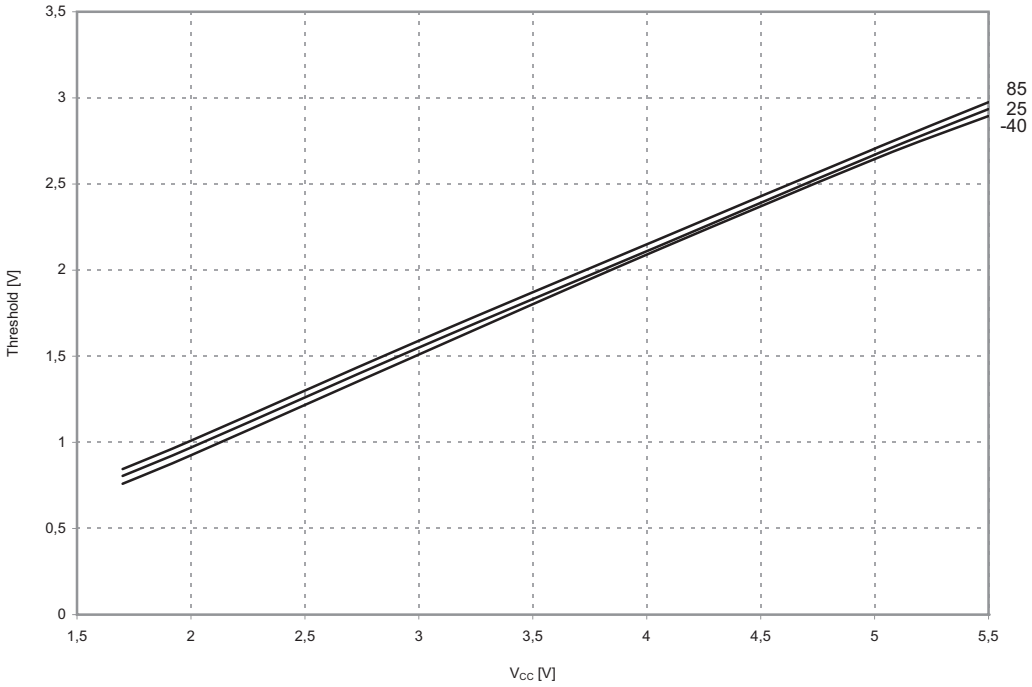


Figure 139. V_{IL}: Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '0')

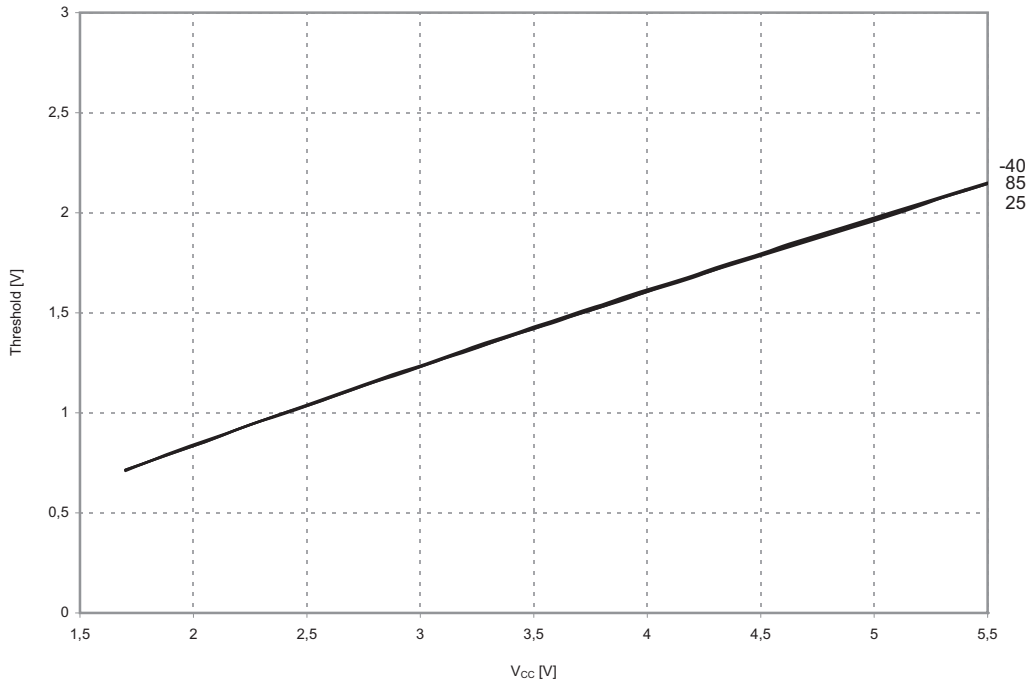
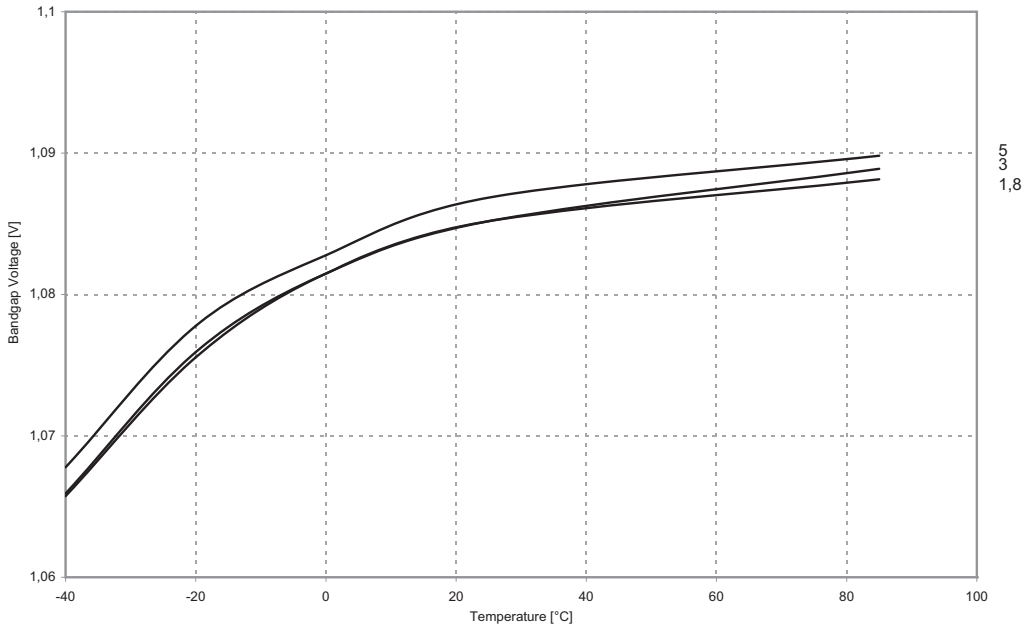
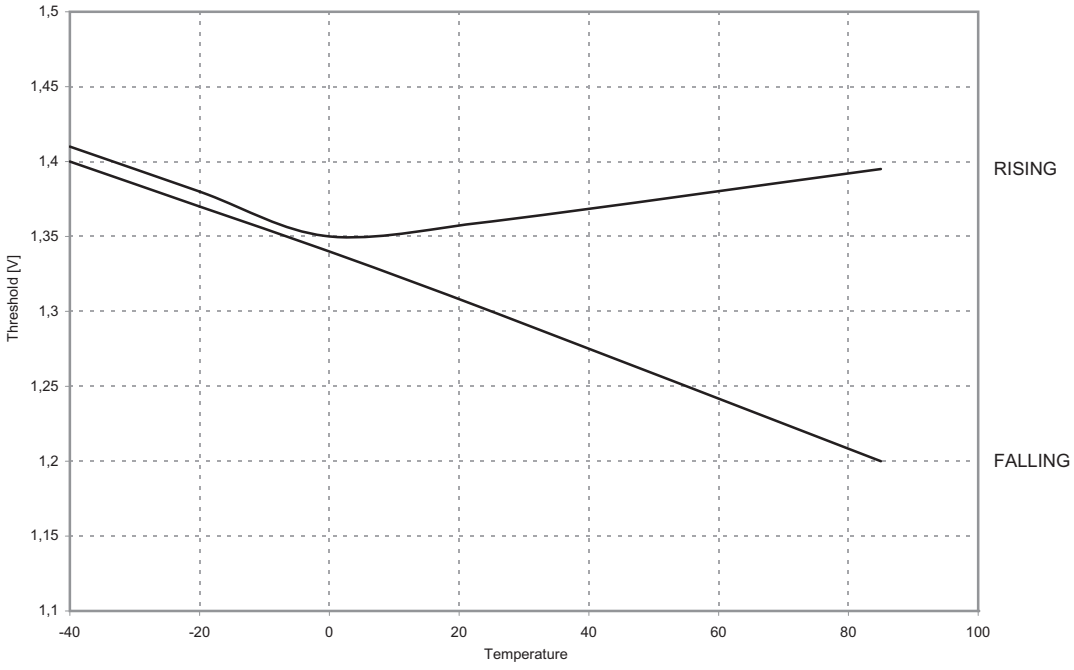


Figure 172. Bandgap Voltage vs. Temperature (V_{CC} = 3.3V)



25.12 Reset

Figure 173. POR Trigger Levels



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