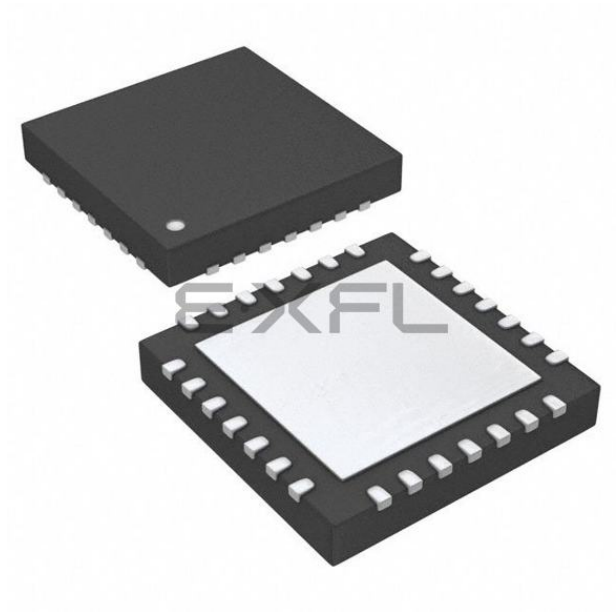

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f23k22-e-mv

2.6.1.1 OSCTUNE Register

The HFINTOSC/MFINTOSC oscillator circuits are factory calibrated but can be adjusted in software by writing to the TUN<5:0> bits of the OSCTUNE register (Register 2-3).

The default value of the TUN<5:0> is '000000'. The value is a 6-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC/MFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

The TUN<5:0> bits in OSCTUNE do not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

The OSCTUNE register also implements the INTSRC and PLLEN bits, which control certain features of the internal oscillator block.

The INTSRC bit allows users to select which internal oscillator provides the clock source when the 31.25 kHz frequency option is selected. This is covered in greater detail in **Section 2.2.3 "Low Frequency Selection"**.

The PLLEN bit controls the operation of the frequency multiplier, PLL, for all primary external clock sources and internal oscillator modes. However, the PLL is intended for operation with clock sources between 4 MHz and 16 MHz. For more details about the function of the PLLEN bit, see **Section 2.8.2 "PLL in HFINTOSC Modes"**

2.7 Register Definitions: Oscillator Tuning

REGISTER 2-3: OSCTUNE: OSCILLATOR TUNING REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTSRC	PLLEN(1)	TUN<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **INTSRC:** Internal Oscillator Low-Frequency Source Select bit
1 = 31.25 kHz device clock derived from the MFINTOSC or HFINTOSC source
0 = 31.25 kHz device clock derived directly from LFINTOSC internal oscillator

bit 6 **PLLEN:** Frequency Multiplier 4xPLL for HFINTOSC Enable bit(1)
1 = PLL enabled
0 = PLL disabled

bit 5-0 **TUN<5:0>:** Frequency Tuning bits – use to adjust MFINTOSC and HFINTOSC frequencies
011111 = Maximum frequency
011110 =
• • •
000001 =
000000 = Oscillator module (HFINTOSC and MFINTOSC) are running at the factory calibrated frequency.
111111 =
• • •
100000 = Minimum frequency

Note 1: The PLLEN bit is active for all the primary clock sources (internal or external) and is designed to operate with clock frequencies between 4 MHz and 16 MHz.

4.2 Register Definitions: Reset Control

REGISTER 4-1: RCON: RESET CONTROL REGISTER

R/W-0/0	R/W-q/u	U-0	R/W-1/q	R-1/q	R-1/q	R/W-q/u	R/W-0/q
IPEN	SBOREN(1)	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$(2)	$\overline{BOR}$
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets
x = Bit is unknown	u = unchanged	q = depends on condition

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6 **SBOREN:** BOR Software Enable bit(1)
If BOREN<1:0> = 01:
1 = BOR is enabled
0 = BOR is disabled
If BOREN<1:0> = 00, 10 or 11:
Bit is disabled and read as '0'.

bit 5 **Unimplemented:** Read as '0'

bit 4 $\overline{\textbf{RI}}$**:** RESET Instruction Flag bit
1 = The RESET instruction was not executed (set by firmware or Power-on Reset)
0 = The RESET instruction was executed causing a device Reset (must be set in firmware after a code-executed Reset occurs)

bit 3 $\overline{\textbf{TO}}$**:** Watchdog Time-out Flag bit
1 = Set by power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 2 $\overline{\textbf{PD}}$**:** Power-down Detection Flag bit
1 = Set by power-up or by the CLRWDT instruction
0 = Set by execution of the SLEEP instruction

bit 1 $\overline{\textbf{POR}}$**:** Power-on Reset Status bit(2)
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 $\overline{\textbf{BOR}}$**:** Brown-out Reset Status bit(3)
1 = A Brown-out Reset has not occurred (set by firmware only)
0 = A Brown-out Reset occurred (must be set by firmware after a POR or Brown-out Reset occurs)

Note 1: When CONFIG2L[2:1] = 01, then the SBOREN Reset state is '1'; otherwise, it is '0'.
2: The actual Reset value of $\overline{POR}$ is determined by the type of device Reset. See the notes following this register and **Section 4.7 "Reset State of Registers"** for additional information.
3: See Table 4-1.

Note 1: Brown-out Reset is indicated when $\overline{BOR}$ is '0' and POR is '1' (assuming that both $\overline{POR}$ and $\overline{BOR}$ were set to '1' by firmware immediately after POR).
2: It is recommended that the $\overline{POR}$ bit be set after a Power-on Reset has been detected so that subsequent Power-on Resets may be detected.

4.5 Brown-out Reset (BOR)

PIC18(L)F2X/4XK22 devices implement a BOR circuit that provides the user with a number of configuration and power-saving options. The BOR is controlled by the BORV<1:0> and BOREN<1:0> bits of the CONFIG2L Configuration register. There are a total of four BOR configurations which are summarized in Table 4-1.

The BOR threshold is set by the BORV<1:0> bits. If BOR is enabled (any values of BOREN<1:0>, except '00'), any drop of V_{DD} below V_{BOR} for greater than T_{BOR} will reset the device. A Reset may or may not occur if V_{DD} falls below V_{BOR} for less than T_{BOR}. The chip will remain in Brown-out Reset until V_{DD} rises above V_{BOR}.

If the Power-up Timer is enabled, it will be invoked after V_{DD} rises above V_{BOR}; it then will keep the chip in Reset for an additional time delay, T_{PWRT}. If V_{DD} drops below V_{BOR} while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once V_{DD} rises above V_{BOR}, the Power-up Timer will execute the additional time delay.

BOR and the Power-on Timer (PWRT) are independently configured. Enabling BOR Reset does not automatically enable the PWRT.

The BOR circuit has an output that feeds into the POR circuit and rearms the POR within the operating range of the BOR. This early rearming of the POR ensures that the device will remain in Reset in the event that V_{DD} falls below the operating range of the BOR circuitry.

4.5.1 DETECTING BOR

When BOR is enabled, the $\overline{BOR}$ bit always resets to '0' on any BOR or POR event. This makes it difficult to determine if a BOR event has occurred just by reading the state of $\overline{BOR}$ alone. A more reliable method is to simultaneously check the state of both $\overline{POR}$ and $\overline{BOR}$. This assumes that the $\overline{POR}$ and $\overline{BOR}$ bits are reset to '1' by software immediately after any POR event. If $\overline{BOR}$ is '0' while $\overline{POR}$ is '1', it can be reliably assumed that a BOR event has occurred.

4.5.2 SOFTWARE ENABLED BOR

When BOREN<1:0> = 01, the BOR can be enabled or disabled by the user in software. This is done with the SBOREN control bit of the RCON register. Setting SBOREN enables the BOR to function as previously described. Clearing SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise it is read as '0'.

Placing the BOR under software control gives the user the additional flexibility of tailoring the application to the environment without having to reprogram the device to change BOR configuration. It also allows the user to tailor device power consumption in software by eliminating the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

Note:	Even when BOR is under software control, the BOR Reset voltage level is still set by the BORV<1:0> Configuration bits. It cannot be changed by software.

4.5.3 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = 10, the BOR remains under hardware control and operates as previously described. Whenever the device enters Sleep mode, however, the BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

4.5.4 MINIMUM BOR ENABLE TIME

Enabling the BOR also enables the Fixed Voltage Reference (FVR) when no other peripheral requiring the FVR is active. The BOR becomes active only after the FVR stabilizes. Therefore, to ensure BOR protection, the FVR settling time must be considered when enabling the BOR in software or when the BOR is automatically enabled after waking from Sleep. If the BOR is disabled, in software or by reentering Sleep before the FVR stabilizes, the BOR circuit will not sense a BOR condition. The FVRST bit of the VREFCON0 register can be used to determine FVR stability.

TABLE 10-5: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RB6/KBI2/PGC	RB6	0	—	O	DIG	LATB<6> data output; not affected by analog input.
		1	—	I	TTL	PORTB<6> data input; disabled when analog input enabled.
	IOC2	1	—	I	TTL	Interrupt-on-change pin.
	TX2(3)	1	—	O	DIG	EUSART asynchronous transmit data output.
	CK2(3)	1	—	O	DIG	EUSART synchronous serial clock output.
		1	—	I	ST	EUSART synchronous serial clock input.
	PGC	x	—	I	ST	In-Circuit Debugger and ICSP™ programming clock input.
RB7/KBI3/PGD	RB7	0	—	O	DIG	LATB<7> data output; not affected by analog input.
		1	—	I	TTL	PORTB<7> data input; disabled when analog input enabled.
	IOC3	1	—	I	TTL	Interrupt-on-change pin.
	RX2(2), (3)	1	—	I	ST	EUSART asynchronous receive data input.
	DT2(2), (3)	1	—	O	DIG	EUSART synchronous serial data output.
		1	—	I	ST	EUSART synchronous serial data input.
	PGD	x	—	O	DIG	In-Circuit Debugger and ICSP™ programming data output.
		x	—	I	ST	In-Circuit Debugger and ICSP™ programming data input.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C.

Note 1: Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

3: Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

TABLE 10-12: REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELD(1)	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	150
BAUDCON2	ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN	271
CCP1CON	P1M<1:0>		DC1B<1:0>		CCP1M<3:0>				198
CCP2CON	P2M<1:0>		DC2B<1:0>		CCP2M<3:0>				198
CCP4CON	—	—	DC4B<1:0>		CCP4M<3:0>				198
LATD(1)	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	152
PORTD(1)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	148
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	270
SLRCON(1)	—	—	—	SLRE	SLRD	SLRC	SLRB	SLRA	153
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				253
TRISD(1)	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	151

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for PORTD.

Note 1: Available on PIC18(L)F4XK22 devices.

TABLE 10-13: CONFIGURATION REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONFIG3H	MCLRE	—	P2BMX	T3CMX	HFOFST	CCP3MX	PBADEN	CCP2MX	348

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for PORTD.

14.4.2 FULL-BRIDGE MODE

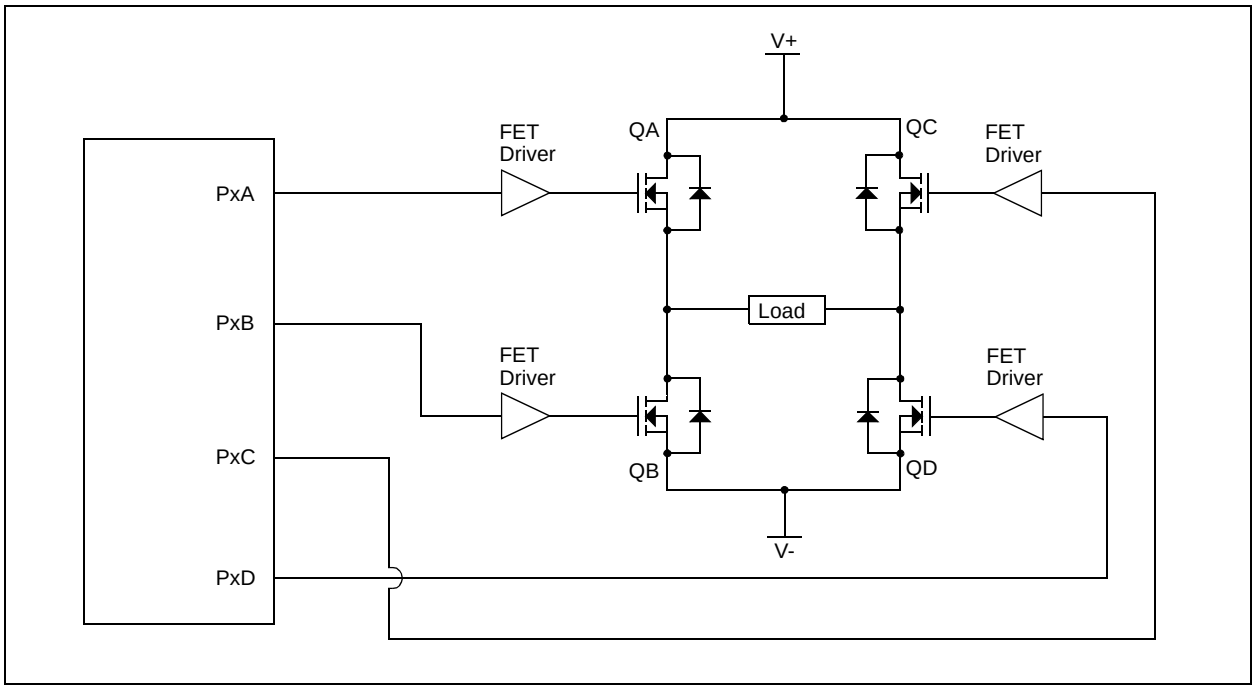
In Full-Bridge mode, all four pins are used as outputs. An example of full-bridge application is shown in Figure 14-10.

In the Forward mode, pin CCPx/PxA is driven to its active state, pin PxD is modulated, while PxB and PxC will be driven to their inactive state as shown in Figure 14-11.

In the Reverse mode, PxC is driven to its active state, pin PxB is modulated, while PxA and PxD will be driven to their inactive state as shown Figure 14-11.

PxA, PxB, PxC and PxD outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the PxA, PxB, PxC and PxD pins as outputs.

FIGURE 14-10: EXAMPLE OF FULL-BRIDGE APPLICATION



The I^2C interface supports the following modes and features:

- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- Limited Multi-master support
- 7-bit and 10-bit addressing
- Start and Stop interrupts
- Interrupt masking
- Clock stretching
- Bus collision detection
- General call address matching
- Address masking
- Address Hold and Data Hold modes
- Selectable SDAx hold times

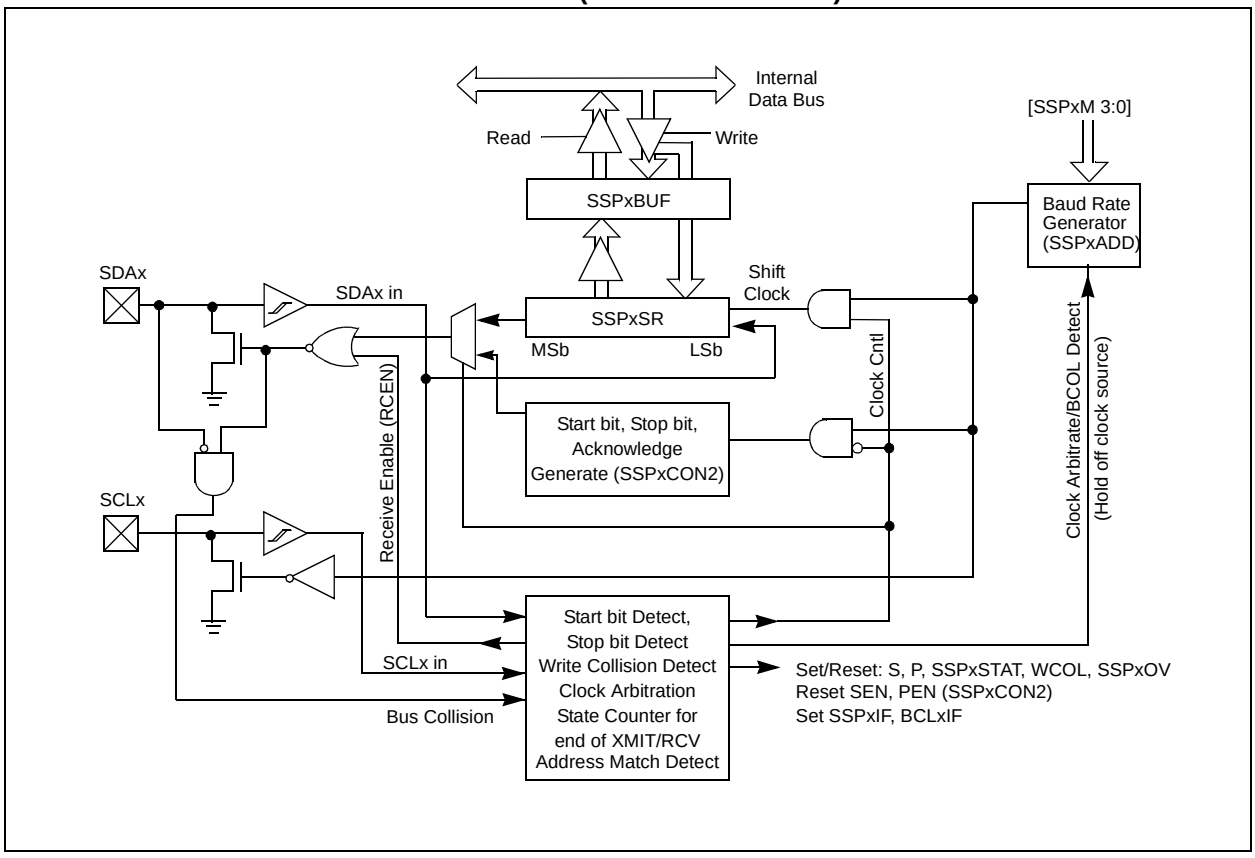
Figure 15-2 is a block diagram of the I^2C interface module in Master mode. Figure 15-3 is a diagram of the I^2C interface module in Slave mode.

The PIC18(L)F2X/4XK22 has two MSSP modules, MSSP1 and MSSP2, each module operating independently from the other.

Note 1: In devices with more than one MSSP module, it is very important to pay close attention to SSPxCONx register names. SSP1CON1 and SSP1CON2 registers control different operational aspects of the same module, while SSP1CON1 and SSP2CON1 control the same features for two different modules.

2: Throughout this section, generic references to an MSSP module in any of its operating modes may be interpreted as being equally applicable to MSSP1 or MSSP2. Register names, module I/O signals, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module when required.

FIGURE 15-2: MSSPx BLOCK DIAGRAM (I^2C MASTER MODE)



15.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDAx pin has been deasserted and allowed to float high, SDAx is sampled low after the BRG has timed out (Case 1).

b) After the SCLx pin is deasserted, SCLx is sampled low before SDAx goes high (Case 2).

The Stop condition begins with SDAx asserted low. When SDAx is sampled low, the SCLx pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD and counts down to zero. After the BRG times out, SDAx is sampled. If SDAx is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 15-38). If the SCLx pin is sampled low before SDAx is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 15-39).

FIGURE 15-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

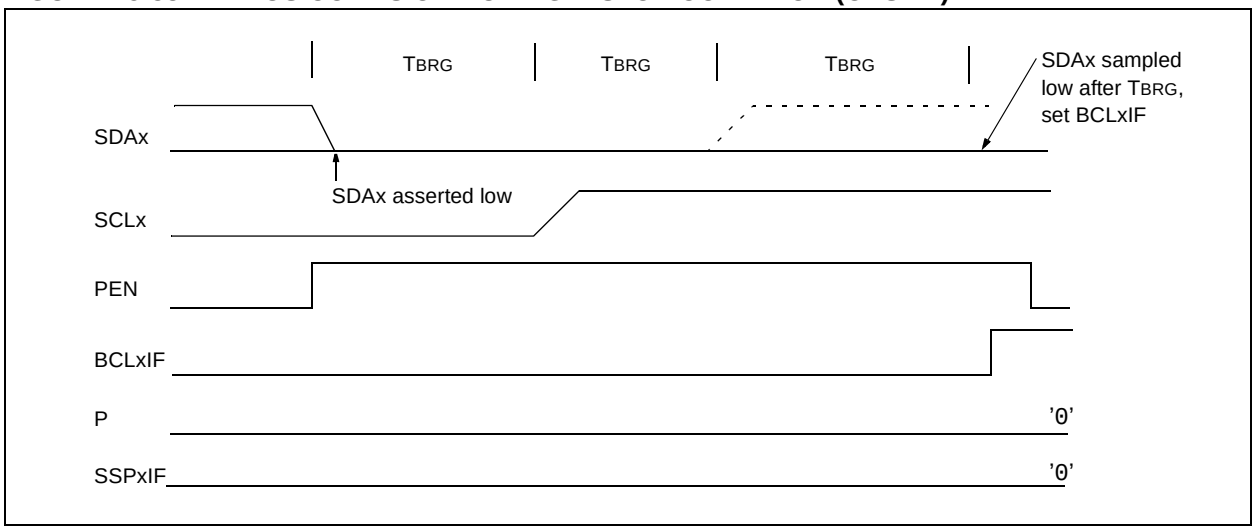


FIGURE 15-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)

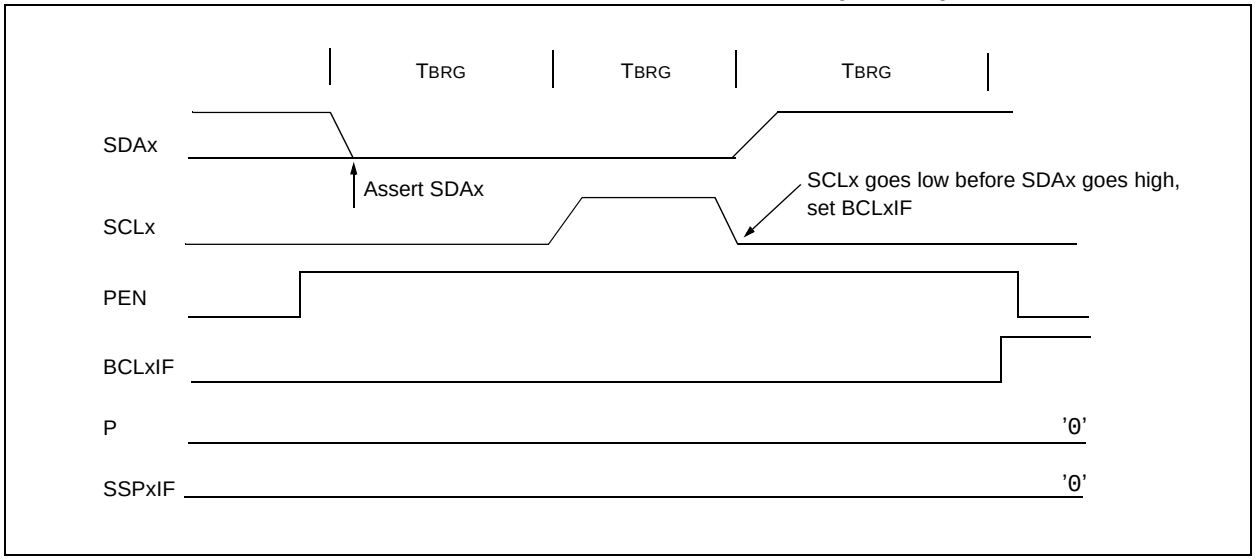
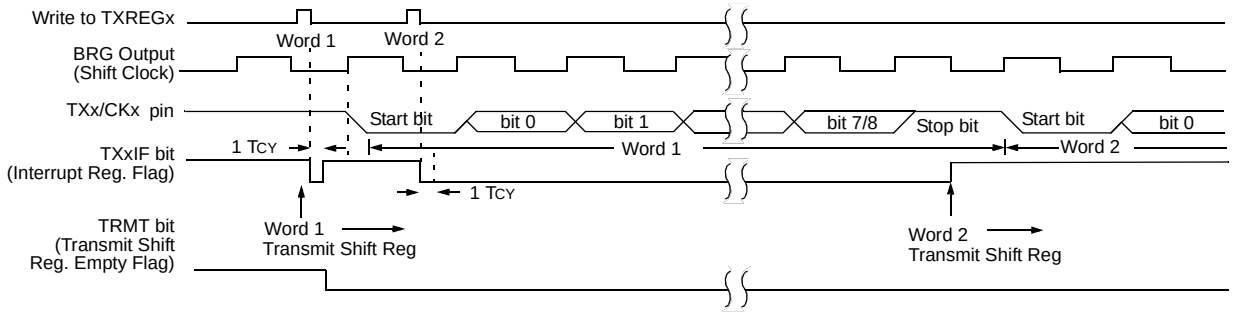


FIGURE 16-4: ASYNCHRONOUS TRANSMISSION (BACK-TO-BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 16-1: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
BAUDCON1	ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN	271
BAUDCON2	ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN	271
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	109
IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	121
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	CTMUIP	TMR5GIP	TMR3GIP	TMR1GIP	123
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	117
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	CTMUIE	TMR5GIE	TMR3GIE	TMR1GIE	119
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	112
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	CTMUIF	TMR5GIF	TMR3GIF	TMR1GIF	114
PMD0	UART2MD	UART1MD	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	52
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	270
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	270
SPBRG1	EUSART1 Baud Rate Generator, Low Byte								—
SPBRGH1	EUSART1 Baud Rate Generator, High Byte								—
SPBRG2	EUSART2 Baud Rate Generator, Low Byte								—
SPBRGH2	EUSART2 Baud Rate Generator, High Byte								—
TXREG1	EUSART1 Transmit Register								—
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	269
TXREG2	EUSART2 Transmit Register								—
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	269

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for asynchronous transmission.

16.1.2.4 Receive Interrupts

The RCxIF interrupt flag bit of the PIR1/PIR3 register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RCxIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCxIF interrupts are enabled by setting the following bits:

- RCxIE interrupt enable bit of the PIE1/PIE3 register
- PEIE/GIEL peripheral interrupt enable bit of the INTCON register
- GIE/GIEH global interrupt enable bit of the INTCON register

The RCxIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

16.1.2.5 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTAx register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.x

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTAx register which resets the EUSART. Clearing the CREN bit of the RCSTAx register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive FIFO have framing errors, repeated reads of the RCREGx will not clear the FERR bit.

16.1.2.6 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTAx register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTAx register or by resetting the EUSART by clearing the SPEN bit of the RCSTAx register.

16.1.2.7 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTAx register is set, the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTAx register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREGx.

16.1.2.8 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTAx register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCxIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

REGISTER 22-2: VREFCON2: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DACR<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **DACR<4:0>:** DAC Voltage Output Select bits

$V_{OUT} = ((V_{SRC}+) - (V_{SRC}-))*(DACR<4:0>/(2^5)) + V_{SRC}-$

TABLE 22-1: REGISTERS ASSOCIATED WITH DAC MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
VREFCON0	FVREN	FVRST	FVRS<1:0>		—	—	—	—	332
VREFCON1	DACEN	DACLPS	DACOE	—	DACPSS<1:0>		—	DACNSS	335
VREFCON2	—	—	—	DACR<4:0>					336

Legend: — = Unimplemented locations, read as '0'. Shaded bits are not used by the DAC module.

24.3.1 CONTROL REGISTER

Register 24-14 shows the WDTCON register. This is a readable and writable register which contains a control bit that allows software to control the WDT when the SWDTEN configuration bits select the software control mode.

24.4 Register Definitions: WDT Control

REGISTER 24-14: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SWDTEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SWDTEN:** Software Enable or Disable the Watchdog Timer bit(1)

1 = WDT is turned on
0 = WDT is turned off (Reset value)

Note 1: This bit has no effect if the Configuration bits WDTEN <1,0> are not equal to '10'.

TABLE 24-3: REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
RCON	IPEN	SBOREN	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	56
WDTCON	—	—	—	—	—	—	—	SWDTEN	355

Legend: — = unimplemented, read as '0'. Shaded bits are not used by the Watchdog Timer.

TABLE 24-4: CONFIGURATION REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
CONFIG2H	—	—	WDPS<3:0>				WDTEN<1:0>		347

Legend: — = unimplemented, read as '0'. Shaded bits are not used by the Watchdog Timer.

27.9 Memory Programming Requirements

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Internal Program Memory Programming Specifications(1)					
D170	VPP	Voltage on $\overline{MCLR}$/VPP pin	8	—	9	V	**(Note 3), (Note 4)**
D171	IDDP	Supply Current during Programming	—	—	10	mA	
		Data EEPROM Memory					
D172	ED	Byte Endurance	100K	—	—	E/W	-40°C to +85°C
D173	VDRW	VDD for Read/Write	VDDMIN	—	VDDMAX	V	Using EECON to read/ write
D175	TDEW	Erase/Write Cycle Time	—	3	4	ms	
D176	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
D177	TREF	Number of Total Erase/Write Cycles before Refresh(2)	1M	10M	—	E/W	-40°C to +85°C
		Program Flash Memory					
D178	EP	Cell Endurance	10K	—	—	E/W	-40°C to +85°C **(Note 5)**
D179	VPR	VDD for Read	VDDMIN	—	VDDMAX	V	
D181	VIW	VDD for Row Erase or Write	2.2	—	VDDMAX	V	PIC18LF24K22
D182	VIW		VDDMIN	—	VDDMAX	V	PIC18(L)F26K22
D183	TIW	Self-timed Write Cycle Time	—	2	—	ms	
D184	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications are for programming the on-chip program memory through the use of table write instructions.

2: Refer to **Section 7.8 “Using the Data EEPROM”** for a more detailed discussion on data EEPROM endurance.

3: Required only if single-supply programming is disabled.

4: The MPLAB ICD 2 does not support variable VPP output. Circuitry to limit the MPLAB ICD 2 VPP voltage must be placed between the MPLAB ICD 2 and target system when programming or debugging with the MPLAB ICD 2.

5: Self-write and Block Erase.

27.11.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 27-7: EXTERNAL CLOCK TIMING (ALL MODES EXCEPT PLL)

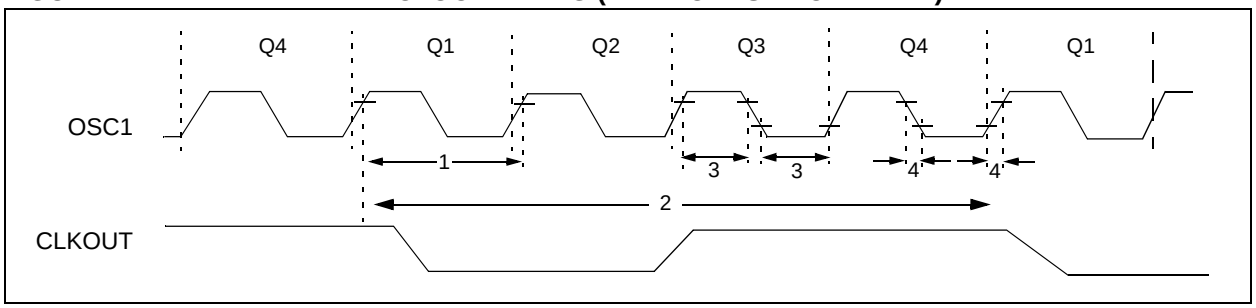


TABLE 27-7: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency(1)	DC	0.5	MHz	EC, ECIO Oscillator mode (low power)
			DC	16	MHz	EC, ECIO Oscillator mode (medium power)
			DC	64	MHz	EC, ECIO Oscillator mode (high power)
		Oscillator Frequency(1)	DC	4	MHz	RC Oscillator mode
			5	200	kHz	LP Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			4	4	MHz	HS Oscillator mode, VDD < 2.7V
			4	16	MHz	HS Oscillator mode, VDD ≥ 2.7V, Medium-Power mode (HSMP)
			4	20	MHz	HS Oscillator mode, VDD ≥ 2.7V, High-Power mode (HSHP)
1	TOSC	External CLKIN Period(1)	2.0	—	µs	EC, ECIO Oscillator mode (low power)
			62.5	—	ns	EC, ECIO Oscillator mode (medium power)
			15.6	—	ns	EC, ECIO Oscillator mode (high power)
		Oscillator Period(1)	250	—	ns	RC Oscillator mode
			5	200	µs	LP Oscillator mode
			0.25	10	µs	XT Oscillator mode
			250	250	ns	HS Oscillator mode, VDD < 2.7V
			62.5	250	ns	HS Oscillator mode, VDD ≥ 2.7V, Medium-Power mode (HSMP)
			50	250	ns	HS Oscillator mode, VDD ≥ 2.7V, High-Power mode (HSHP)
2	TCY	Instruction Cycle Time(1)	62.5	—	ns	TCY = 4/FOSC
3	TOSL, TOSH	External Clock in (OSC1) High or Low Time	2.5	—	µs	LP Oscillator mode
			30	—	ns	XT Oscillator mode
			10	—	ns	HS Oscillator mode
4	TOSR, TOSF	External Clock in (OSC1) Rise or Fall Time	—	50	ns	LP Oscillator mode
			—	20	ns	XT Oscillator mode
			—	7.5	ns	HS Oscillator mode

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

FIGURE 28-3: PIC18LF2X/4XK22 DELTA IPD WATCHDOG TIMER (WDT)

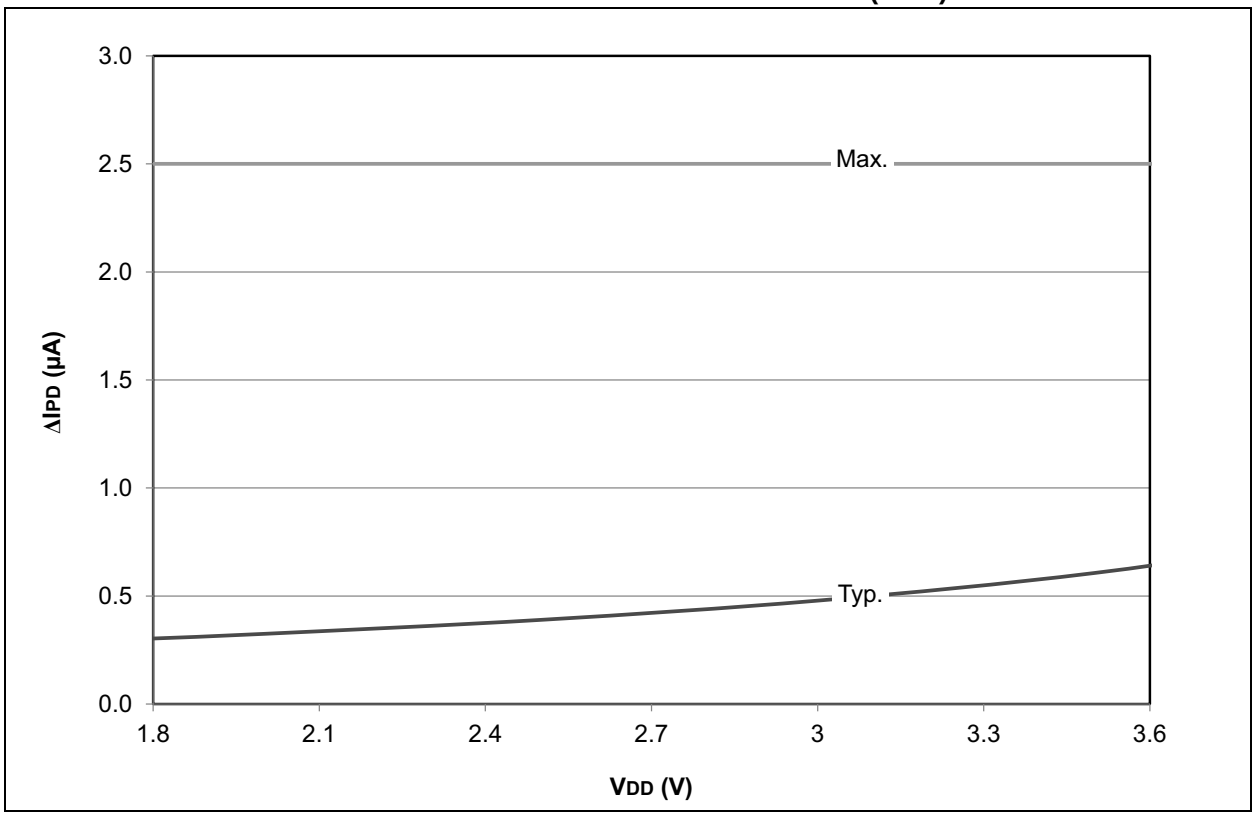


FIGURE 28-4: PIC18F2X/4XK22 DELTA IPD WATCHDOG TIMER (WDT)

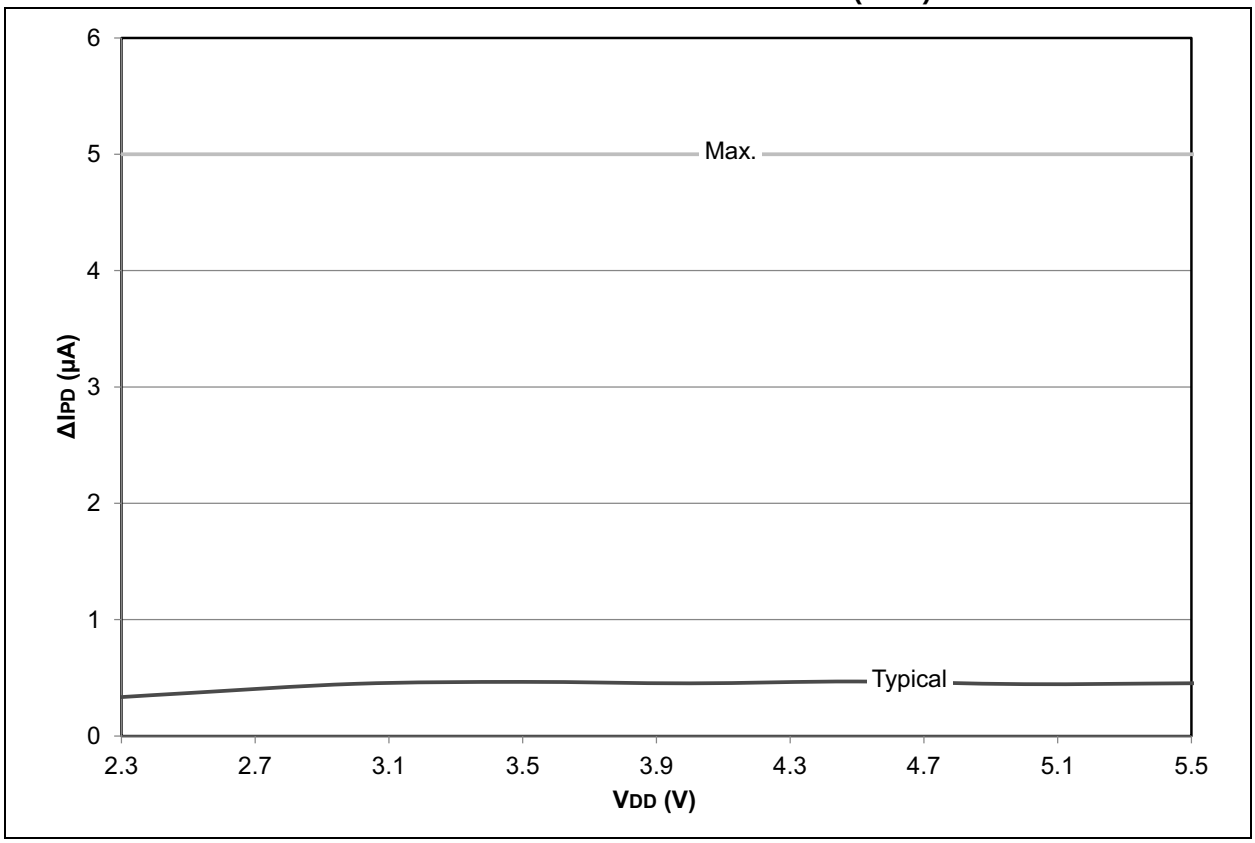


FIGURE 28-30: PIC18LF2X/4XK22 TYPICAL IDD: RC_RUN HF-INTOSC with PLL

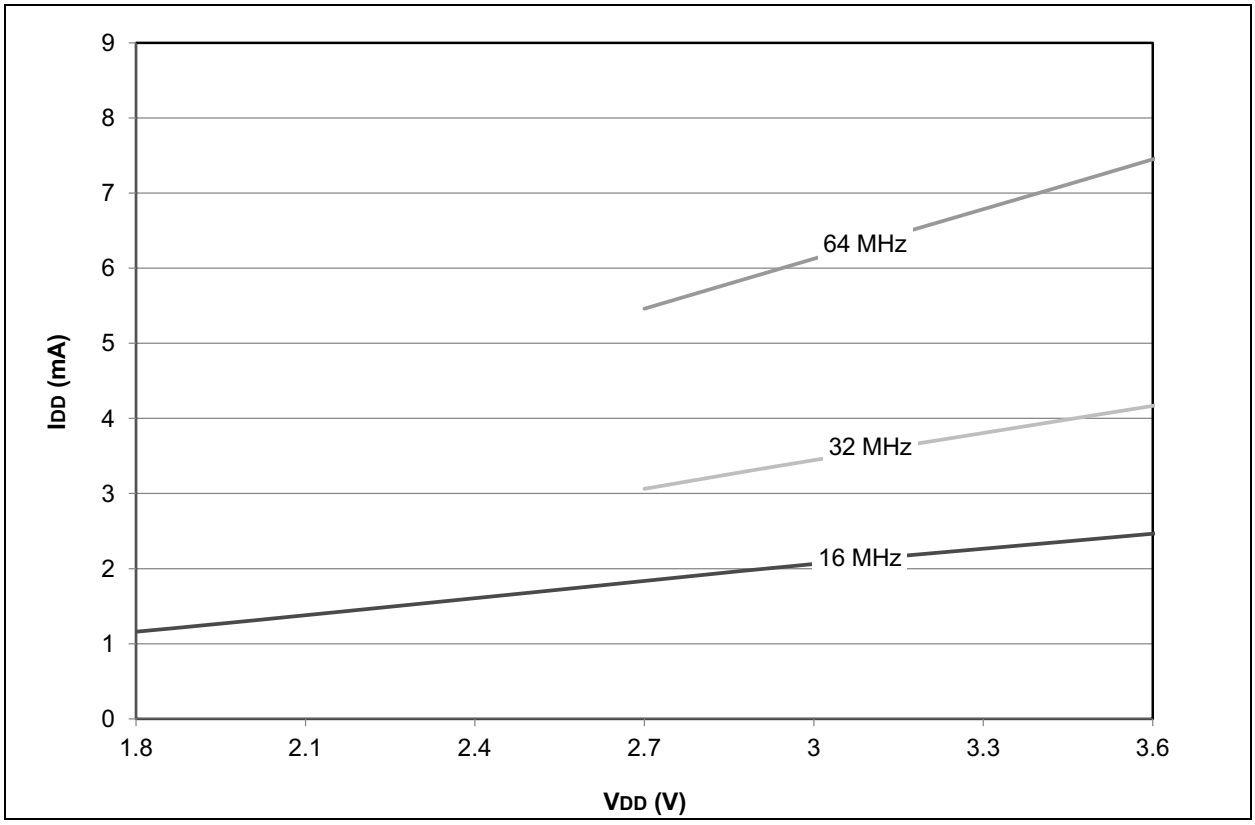


FIGURE 28-31: PIC18LF2X/4XK22 MAXIMUM IDD: RC_RUN HF-INTOSC with PLL

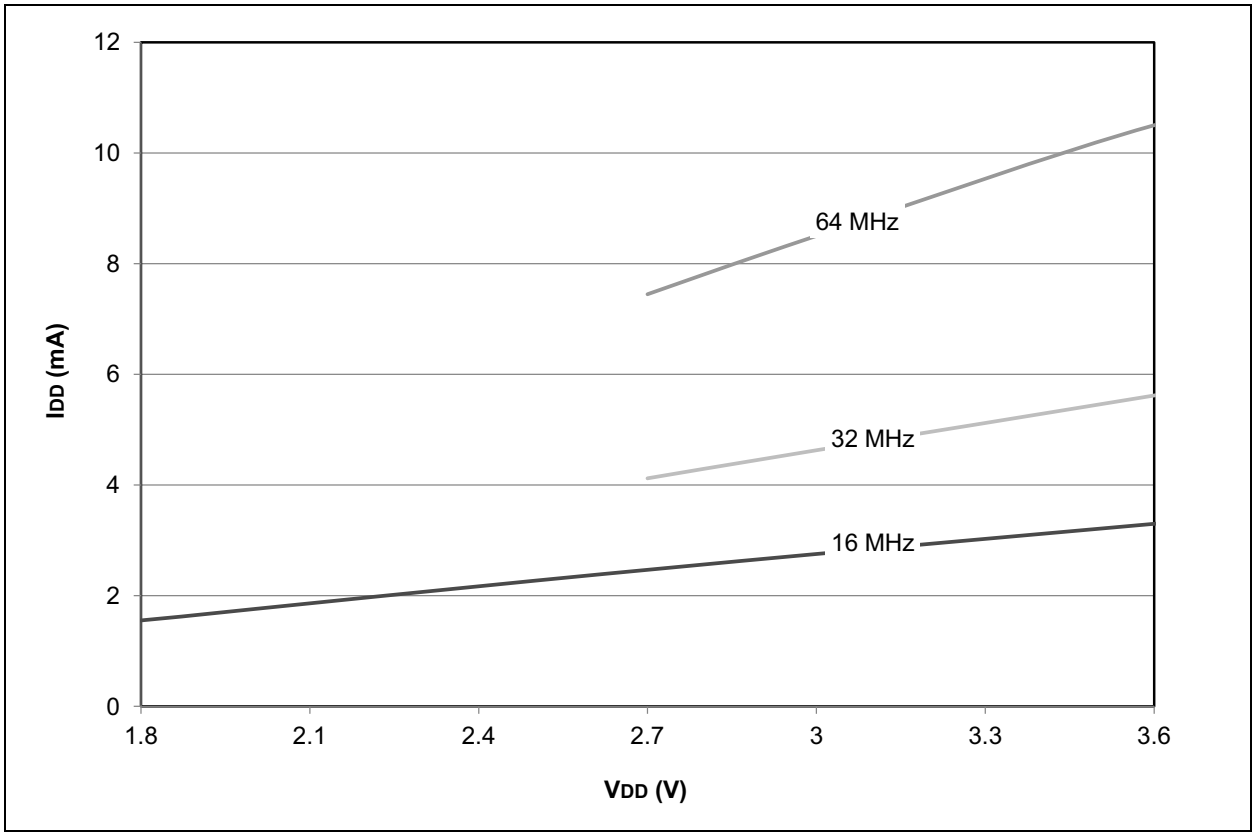


FIGURE 28-58: PIC18F2X/4XK22 TYPICAL IDD: PRI_RUN EC with PLL

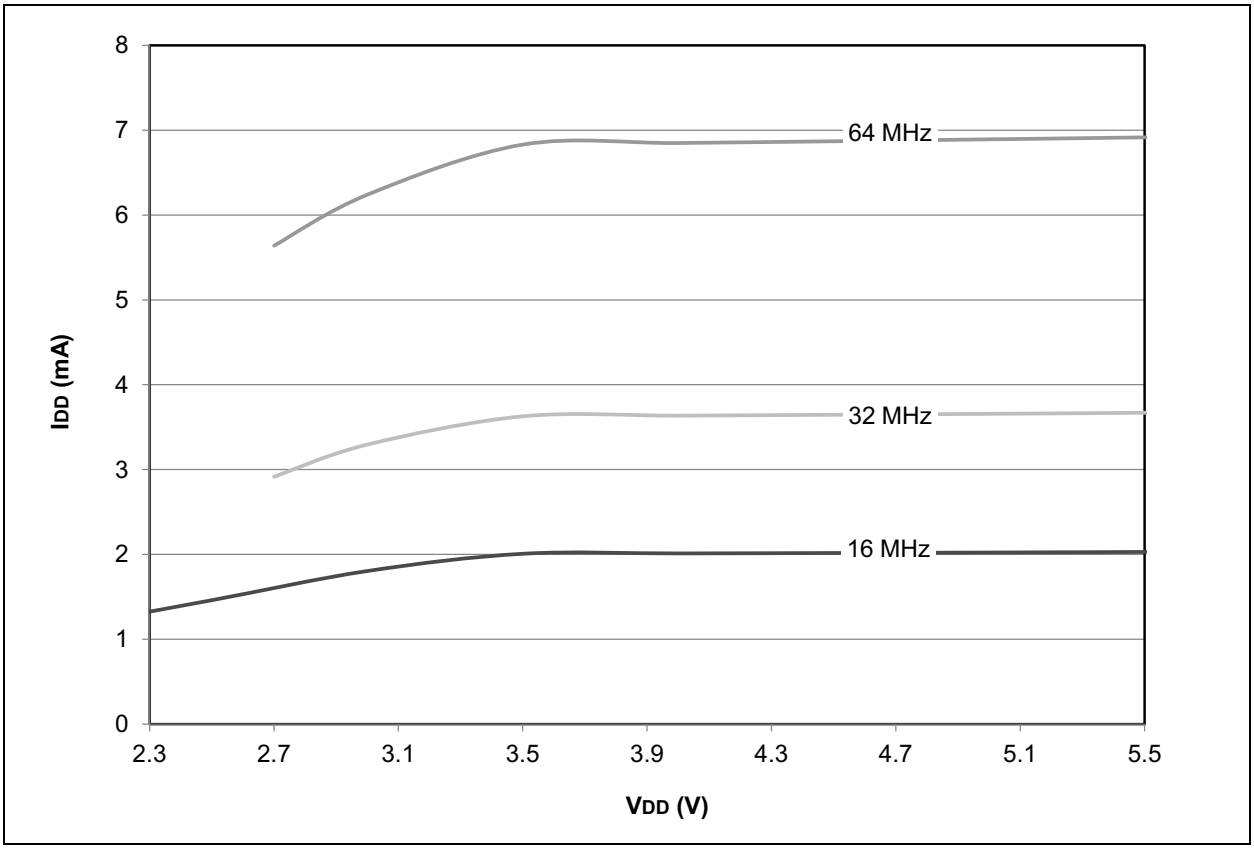


FIGURE 28-59: PIC18F2X/4XK22 MAXIMUM IDD: PRI_RUN EC with PLL

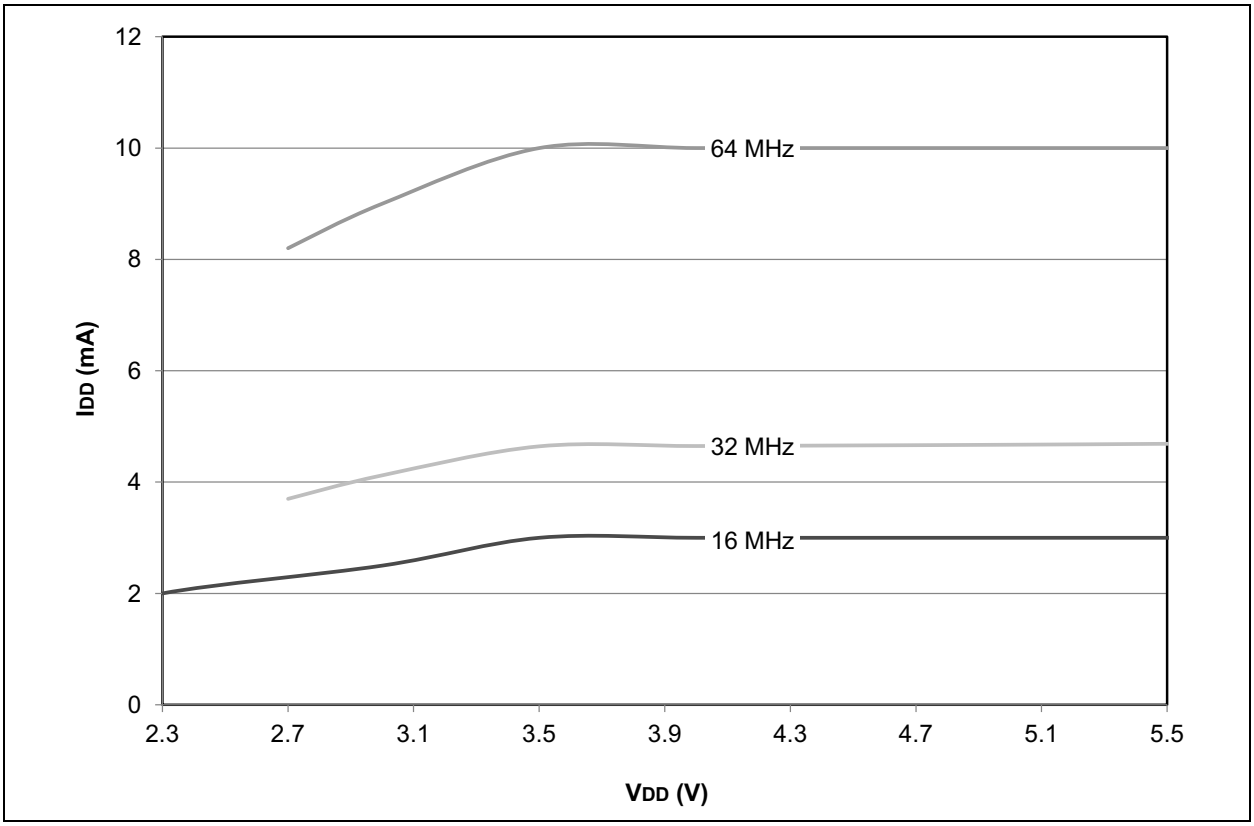


FIGURE 28-98: PIC18F2X/4XK22 TYPICAL FIXED VOLTAGE REFERENCE 4x OUTPUT

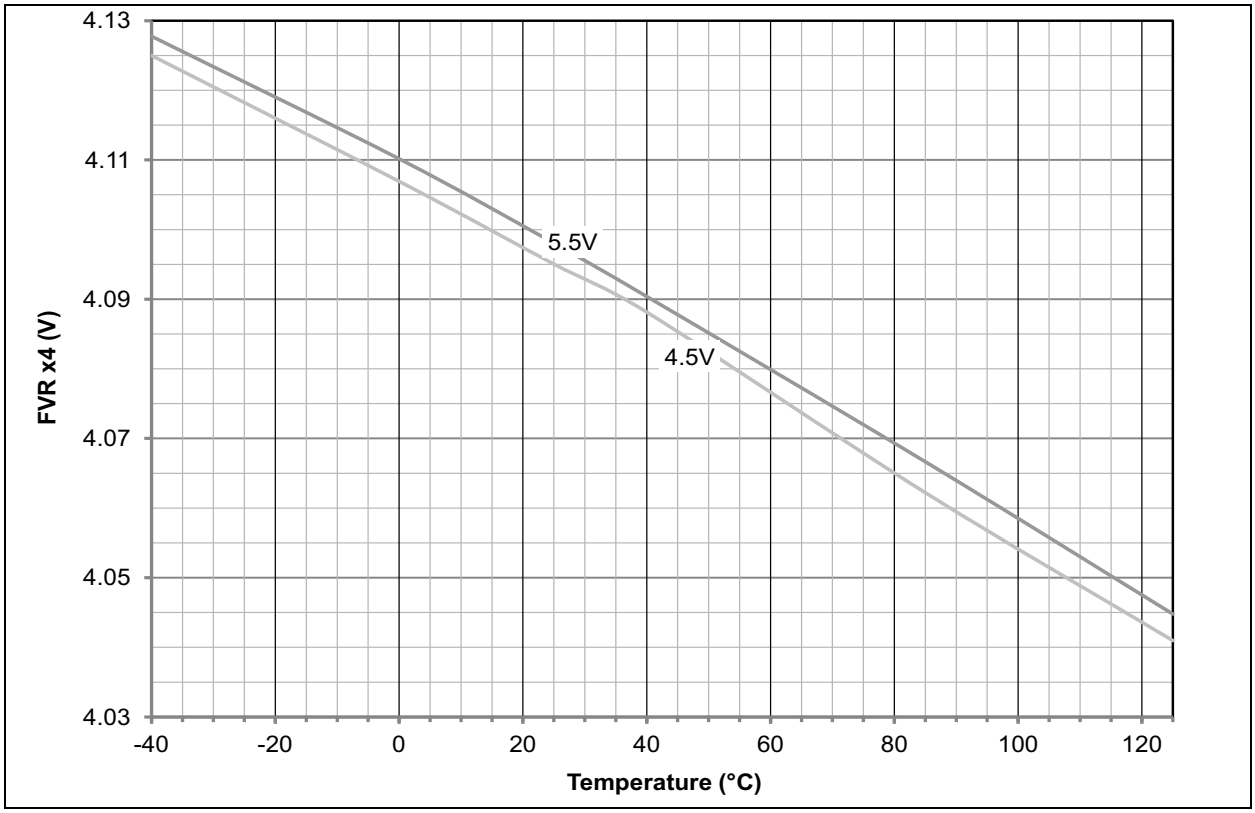
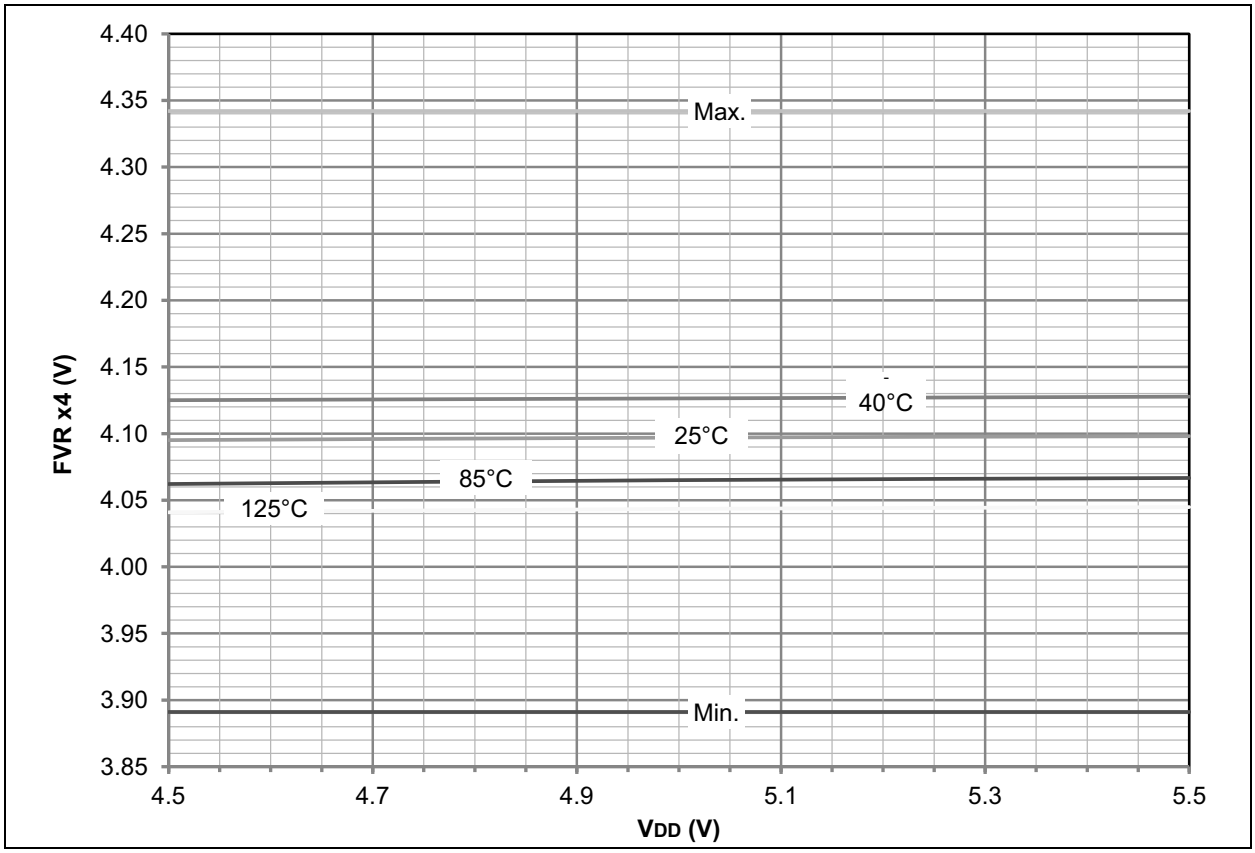
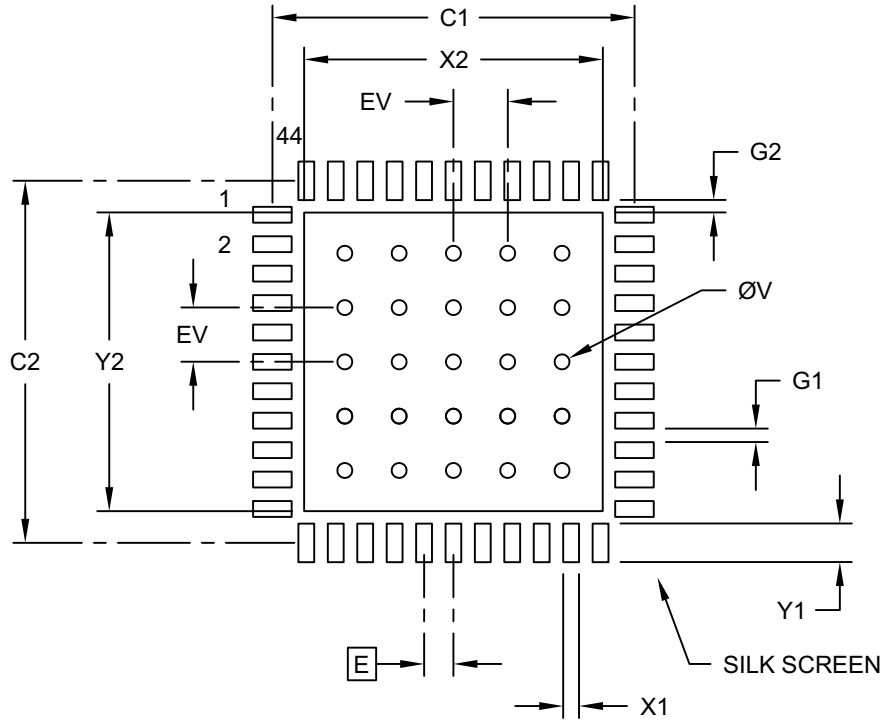


FIGURE 28-99: PIC18F2X/4XK22 TYPICAL FIXED VOLTAGE REFERENCE 4x OUTPUT



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Contact Pad to Contact Pad (X40)	G1	0.30		
Contact Pad to Center Pad (X44)	G2	0.28		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2103C

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ISBN: 978-1-5224-0907-6