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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f23k22t-i-mv

PIC18(L)F2X/4XK22

TABLE 3: PIC18(L)F4XK22 PIN SUMMARY (CONTINUED)

40-PDIP	40-UQFN	44-TQFP	44-QFN	I/O	Analog	Comparator	CTMU	SR Latch	Reference	(E)CCP	EUSART	MSSP	Timers	Interrupts	Pull-up	Basic
9	24	26	26	RE1	AN6					P3B						
10	25	27	27	RE2	AN7					CCP5						
1	16	18	18	RE3											Y	MCLR VPP
11, 32	7, 26	7, 28	7,8 28, 29	VDD												VDD
12, 31	6, 27	6, 29	6, 30, 31	VSS												VSS
—	—	12, 13 33, 34	13	NC												

- Note**
- 1: CCP2 multiplexed in fuses.
 - 2: T3CKI multiplexed in fuses.
 - 3: CCP3/P3A multiplexed in fuses.
 - 4: P2B multiplexed in fuses.

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TABLE 1-3: PIC18(L)F4XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Number				Pin Name	Pin Type	Buffer Type	Description
PDIP	TQFP	QFN	UQFN				
7	24	24	22	RA5/C2OUT/SRNQ/SS1/HLVDIN/AN4			
				RA5	I/O	TTL	Digital I/O.
				C2OUT	O	CMOS	Comparator C2 output.
				SRNQ	O	TTL	SR latch \bar{Q} output.
				$\overline{SS1}$	I	TTL	SPI slave select input (MSSP1).
				HLVDIN	I	Analog	High/Low-Voltage Detect input.
AN4	I	Analog	Analog input 4.				
14	31	33	29	RA6/CLKO/OSC2			
				RA6	I/O	TTL	Digital I/O.
				CLKO	O	—	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
				OSC2	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
13	30	32	28	RA7/CLKI/OSC1			
				RA7	I/O	TTL	Digital I/O.
				CLKI	I	CMOS	External clock source input. Always associated with pin function OSC1.
				OSC1	I	ST	Oscillator crystal input or external clock source input ST buffer when configured in RC mode; CMOS otherwise.
33	8	9	8	RB0/INT0/FLT0/SRI/AN12			
				RB0	I/O	TTL	Digital I/O.
				INT0	I	ST	External interrupt 0.
				FLT0	I	ST	PWM Fault input for ECCP Auto-Shutdown.
				SRI	I	ST	SR latch input.
				AN12	I	Analog	Analog input 12.
34	9	10	9	RB1/INT1/C12IN3-/AN10			
				RB1	I/O	TTL	Digital I/O.
				INT1	I	ST	External interrupt 1.
				C12IN3-	I	Analog	Comparators C1 and C2 inverting input.
				AN10	I	Analog	Analog input 10.
35	10	11	10	RB2/INT2/CTED1/AN8			
				RB2	I/O	TTL	Digital I/O.
				INT2	I	ST	External interrupt 2.
				CTED1	I	ST	CTMU Edge 1 input.
				AN8	I	Analog	Analog input 8.
36	11	12	11	RB3/CTED2/P2A/CCP2/C12IN2-/AN9			
				RB3	I/O	TTL	Digital I/O.
				CTED2	I	ST	CTMU Edge 2 input.
				P2A ⁽²⁾	O	CMOS	Enhanced CCP2 PWM output.
				CCP2 ⁽²⁾	I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
				C12IN2-	I	Analog	Comparators C1 and C2 inverting input.
				AN9	I	Analog	Analog input 9.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power.

Note 1: Default pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

Note 2: Alternate pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

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2.4 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Clock modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC mode) circuits.
- Internal clock sources are contained internally within the Oscillator block. The Oscillator block has three internal oscillators: the 16 MHz High-Frequency Internal Oscillator (HFINTOSC), 500 kHz Medium-Frequency Internal Oscillator (MFINTOSC) and the 31.25 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS<1:0>) bits of the OSCCON register. See **Section 2.11 “Clock Switching”** for additional information.

2.5 External Clock Modes

2.5.1 OSCILLATOR START-UP TIMER (OST)

When the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 2-2.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 2.12 “Two-Speed Clock Start-up Mode”**).

TABLE 2-2: OSCILLATOR DELAY EXAMPLES

Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR/BOR	LFINTOSC MFINTOSC HFINTOSC	31.25 kHz 31.25 kHz to 500 kHz 31.25 kHz to 16 MHz	Oscillator Start-up Delay (T _{OSC_ST})
Sleep/POR/BOR	EC, RC	DC – 64 MHz	2 instruction cycles
LFINTOSC (31.25 kHz)	EC, RC	DC – 64 MHz	1 cycle of each
Sleep/POR/BOR	LP, XT, HS	32 kHz to 40 MHz	1024 Clock Cycles (OST)
Sleep/POR/BOR	4xPLL	32 MHz to 64 MHz	1024 Clock Cycles (OST) + 2 ms
LFINTOSC (31.25 kHz)	LFINTOSC HFINTOSC	31.25 kHz to 16 MHz	1 μs (approx.)

2.5.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 2-5 shows the pin connections for EC mode.

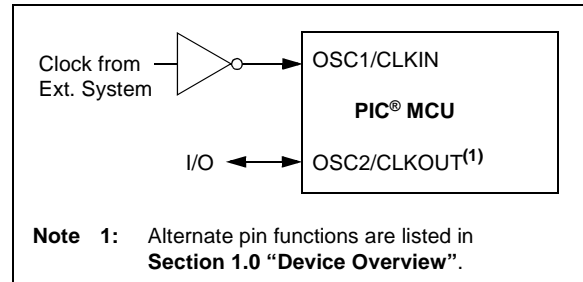
The External Clock (EC) offers different power modes, Low Power (ECLP), Medium Power (ECMP) and High Power (ECHP), selectable by the FOSC<3:0> bits. Each mode is best suited for a certain range of frequencies. The ranges are:

- ECLP – below 500 kHz
- ECMP – between 500 kHz and 16 MHz
- ECHP – above 16 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep.

Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 2-5: EXTERNAL CLOCK (EC) MODE OPERATION



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3.3 Sleep Mode

The Power-Managed Sleep mode in the PIC18(L)F2X/4XK22 devices is identical to the legacy Sleep mode offered in all other PIC microcontroller devices. It is entered by clearing the IDLEN bit of the OSCCON register and executing the `SLEEP` instruction. This shuts down the selected oscillator (Figure 3-4) and all clock source Status bits are cleared.

Entering the Sleep mode from either Run or Idle mode does not require a clock switch. This is because no clocks are needed once the controller has entered Sleep. If the WDT is selected, the LFINTOSC source will continue to operate. If the SOSC oscillator is enabled, it will also continue to run.

When a wake event occurs in Sleep mode (by interrupt, Reset or WDT time-out), the device will not be clocked until the clock source selected by the `SCS<1:0>` bits becomes ready (see Figure 3-5), or it will be clocked from the internal oscillator block if either the Two-Speed Start-up or the Fail-Safe Clock Monitor are enabled (see Section 24.0 “Special Features of the CPU”). In either case, the OSTS bit is set when the primary clock is providing the device clocks. The IDLEN and SCS bits are not affected by the wake-up.

3.4 Idle Modes

The Idle modes allow the controller’s CPU to be selectively shut down while the peripherals continue to operate. Selecting a particular Idle mode allows users to further manage power consumption.

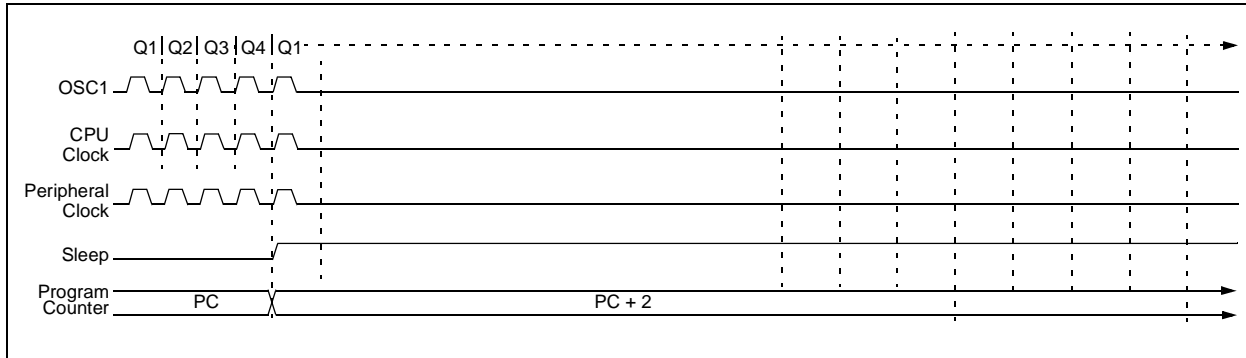
If the IDLEN bit is set to a ‘1’ when a `SLEEP` instruction is executed, the peripherals will be clocked from the clock source selected by the `SCS<1:0>` bits; however, the CPU will not be clocked. The clock source status bits are not affected. Setting IDLEN and executing a `SLEEP` instruction provides a quick method of switching from a given Run mode to its corresponding Idle mode.

If the WDT is selected, the LFINTOSC source will continue to operate. If the SOSC oscillator is enabled, it will also continue to run.

Since the CPU is not executing instructions, the only exits from any of the Idle modes are by interrupt, WDT time-out, or a Reset. When a wake event occurs, CPU execution is delayed by an interval of `TCSD` while it becomes ready to execute code. When the CPU begins executing code, it resumes with the same clock source for the current Idle mode. For example, when waking from `RC_IDLE` mode, the internal oscillator block will clock the CPU and peripherals (in other words, `RC_RUN` mode). The IDLEN and SCS bits are not affected by the wake-up.

While in any Idle mode or the Sleep mode, a WDT time-out will result in a WDT wake-up to the Run mode currently specified by the `SCS<1:0>` bits.

FIGURE 3-4: TRANSITION TIMING FOR ENTRY TO SLEEP MODE



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5.6.3.1 FSR Registers and the INDF Operand

At the core of indirect addressing are three sets of registers: FSR0, FSR1 and FSR2. Each represents a pair of 8-bit registers, FSRnH and FSRnL. Each FSR pair holds a 12-bit value, therefore, the four upper bits of the FSRnH register are not used. The 12-bit FSR value can address the entire range of the data memory in a linear fashion. The FSR register pairs, then, serve as pointers to data memory locations.

Indirect addressing is accomplished with a set of Indirect File Operands, INDF0 through INDF2. These can be thought of as “virtual” registers: they are mapped in the SFR space but are not physically implemented. Reading or writing to a particular INDF register actually accesses its corresponding FSR register pair. A read from INDF1, for example, reads the data at the address indicated by FSR1H:FSR1L. Instructions that use the INDF registers as operands actually use the contents of their corresponding FSR as a pointer to the instruction’s target. The INDF operand is just a convenient way of using the pointer.

Because indirect addressing uses a full 12-bit address, data RAM banking is not necessary. Thus, the current contents of the BSR and the Access RAM bit have no effect on determining the target address.

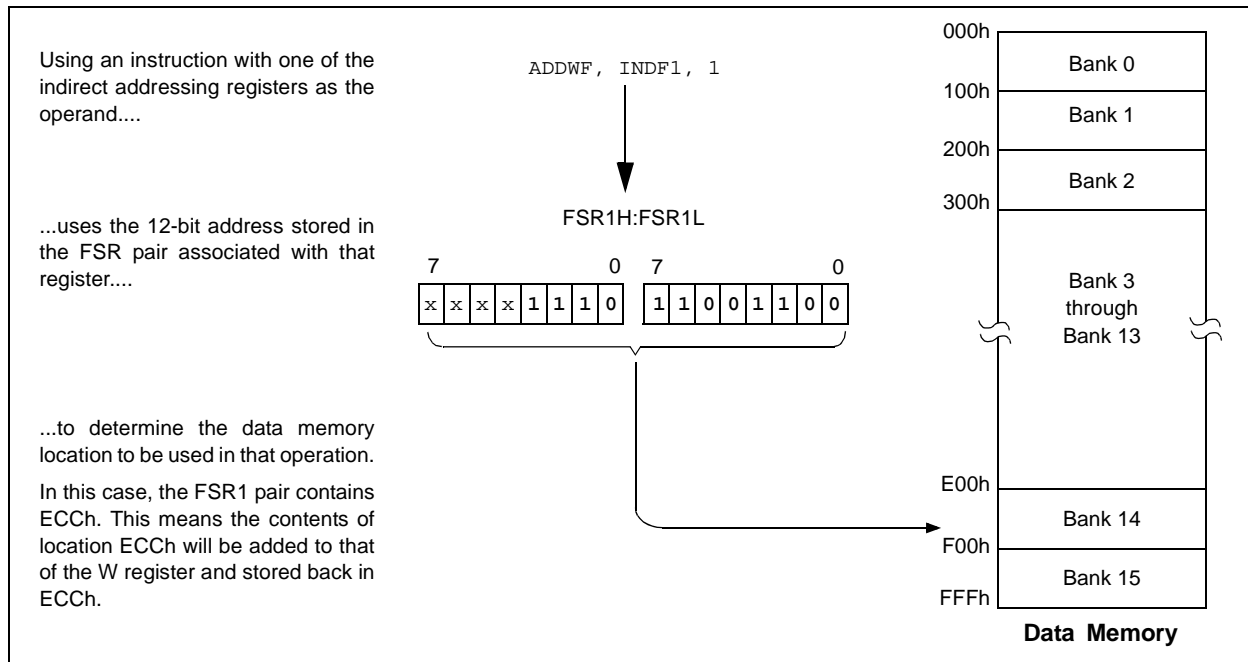
5.6.3.2 FSR Registers and POSTINC, POSTDEC, PREINC and PLUSW

In addition to the INDF operand, each FSR register pair also has four additional indirect operands. Like INDF, these are “virtual” registers which cannot be directly read or written. Accessing these registers actually accesses the location to which the associated FSR register pair points, and also performs a specific action on the FSR value. They are:

- **POSTDEC:** accesses the location to which the FSR points, then automatically decrements the FSR by 1 afterwards
- **POSTINC:** accesses the location to which the FSR points, then automatically increments the FSR by 1 afterwards
- **PREINC:** automatically increments the FSR by one, then uses the location to which the FSR points in the operation
- **PLUSW:** adds the signed value of the W register (range of -127 to 128) to that of the FSR and uses the location to which the result points in the operation.

In this context, accessing an INDF register uses the value in the associated FSR register without changing it. Similarly, accessing a PLUSW register gives the FSR value an offset by that in the W register; however, neither W nor the FSR is actually changed in the operation. Accessing the other virtual registers changes the value of the FSR register.

FIGURE 5-10: INDIRECT ADDRESSING



7.0 DATA EEPROM MEMORY

The data EEPROM is a nonvolatile memory array, separate from the data RAM and program memory, which is used for long-term storage of program data. It is not directly mapped in either the register file or program memory space but is indirectly addressed through the Special Function Registers (SFRs). The EEPROM is readable and writable during normal operation over the entire VDD range.

Four SFRs are used to read and write to the data EEPROM as well as the program memory. They are:

- EECON1
- EECON2
- EEDATA
- EEADR
- EEADRH

The data EEPROM allows byte read and write. When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write and the EEADR:EEADRH register pair hold the address of the EEPROM location being accessed.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an on-chip timer; it will vary with voltage and temperature as well as from chip-to-chip. Please refer to the Data EEPROM Memory parameters in **Section 27.0 “Electrical Specifications”** for limits.

7.1 EEADR and EEADRH Registers

The EEADR register is used to address the data EEPROM for read and write operations. The 8-bit range of the register can address a memory range of 256 bytes (00h to FFh). The EEADRH register expands the range to 1024 bytes by adding an additional two address bits.

7.2 EECON1 and EECON2 Registers

Access to the data EEPROM is controlled by two registers: EECON1 and EECON2. These are the same registers which control access to the program memory and are used in a similar manner for the data EEPROM.

The EECON1 register (Register 7-1) is the control register for data and program memory access. Control bit EEPGD determines if the access will be to program or data EEPROM memory. When the EEPGD bit is clear, operations will access the data EEPROM memory. When the EEPGD bit is set, program memory is accessed.

Control bit, CFGS, determines if the access will be to the Configuration registers or to program memory/data EEPROM memory. When the CFGS bit is set, subsequent operations access Configuration registers. When the CFGS bit is clear, the EEPGD bit selects either program Flash or data EEPROM memory.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

The WRERR bit is set by hardware when the WR bit is set and cleared when the internal programming timer expires and the write operation is complete.

Note: During normal operation, the WRERR may read as '1'. This can indicate that a write operation was prematurely terminated by a Reset, or a write operation was attempted improperly.

The WR control bit initiates write operations. The bit can be set but not cleared by software. It is cleared only by hardware at the completion of the write operation.

Note: The EEIF interrupt flag bit of the PIR2 register is set when the write is complete. It must be cleared by software.

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (EEPGD = 1). Program memory is read using table read instructions. See **Section 6.1 “Table Reads and Table Writes”** regarding table reads.

The EECON2 register is not a physical register. It is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

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A mismatch condition will continue to set the RBIF flag bit. Reading or writing PORTB will end the mismatch condition and allow the RBIF bit to be cleared. The latch holding the last read value is not affected by a MCLR nor Brown-out Reset. After either one of these Resets, the RBIF flag will continue to be set if a mismatch is present.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RBIF interrupt flag may not get set. Furthermore, since a read or write on a port affects all bits of that port, care must be taken when using multiple pins in Interrupt-on-change mode. Changes on one pin may not be seen while servicing changes on another pin.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

10.3.3 ALTERNATE FUNCTIONS

PORTB is multiplexed with several peripheral functions (Table 10-5). The pins have TTL input buffers. Some of these pin functions can be relocated to alternate pins using the Control fuse bits in CONFIG3H. RB5 is the default pin for P2B (28-pin devices). Clearing the P2BMX bit moves the pin function to RC0. RB5 is also the default pin for the CCP3/P3A peripheral pin. Clearing the CCP3MX bit moves the pin function to the RC6 pin (28-pin devices) or RE0 (40/44-pin devices).

Two other pin functions, T3CKI and CCP2/P2A, can be relocated from their default pins to PORTB pins by clearing the control fuses in CONFIG3H. Clearing T3CMX and CCP2MX moves the pin functions to RB5 and RB3, respectively.

TABLE 10-5: PORTB I/O SUMMARY

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RB0/INT0/CCP4/ FLT0/SRI/SS2/ AN12	RB0	0	0	O	DIG	LATB<0> data output; not affected by analog input.
		1	0	I	TTL	PORTB<0> data input; disabled when analog input enabled.
	INT0	1	0	I	ST	External interrupt 0.
	CCP4 ⁽³⁾	0	0	O	DIG	Compare 4 output/PWM 4 output.
		1	0	I	ST	Capture 4 input.
	FLT0	1	0	I	ST	PWM Fault input for ECCP auto-shutdown.
	SRI	1	0	I	ST	SR latch input.
	SS2 ⁽³⁾	1	0	I	TTL	SPI slave select input (MSSP2).
AN12	1	1	I	AN	Analog input 12.	
RB1/INT1/P1C/ SCK2/SCL2/ C12IN3-/AN10	RB1	0	0	O	DIG	LATB<1> data output; not affected by analog input.
		1	0	I	TTL	PORTB<1> data input; disabled when analog input enabled.
	INT1	1	0	I	ST	External Interrupt 1.
	P1C ⁽³⁾	0	0	O	DIG	Enhanced CCP1 PWM output 3.
	SCK2 ⁽³⁾	0	0	O	DIG	MSSP2 SPI Clock output.
		1	0	I	ST	MSSP2 SPI Clock input.
	SCL2 ⁽³⁾	0	0	O	DIG	MSSP2 I ² C Clock output.
		1	0	I	I ² C	MSSP2 I ² C Clock input.
	C12IN3-	1	1	I	AN	Comparators C1 and C2 inverting input.
	AN10	1	1	I	AN	Analog input 10.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I²C = Schmitt Trigger input with I²C.

- Note 1:** Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.
- 2:** Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.
- 3:** Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

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13.1 Timer2/4/6 Operation

The clock input to the Timer2/4/6 module is the system instruction clock ($F_{osc}/4$).

TMRx increments from 00h on each clock edge.

A 4-bit counter/prescaler on the clock input allows direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, TxCKPS<1:0> of the TxCON register. The value of TMRx is compared to that of the Period register, PRx, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMRx to 00h on the next cycle and drives the output counter/postscaler (see **Section 13.2 “Timer2/4/6 Interrupt”**).

The TMRx and PRx registers are both directly readable and writable. The TMRx register is cleared on any device Reset, whereas the PRx register initializes to FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMRx register
- a write to the TxCON register
- Power-on Reset (POR)
- Brown-out Reset (BOR)
- MCLR Reset
- Watchdog Timer (WDT) Reset
- Stack Overflow Reset
- Stack Underflow Reset
- RESET Instruction

Note: TMRx is not cleared when TxCON is written.

13.2 Timer2/4/6 Interrupt

Timer2/4/6 can also generate an optional device interrupt. The Timer2/4/6 output signal (TMRx-to-PRx match) provides the input for the 4-bit counter/postscaler. This counter generates the TMRx match interrupt flag which is latched in TMRxIF of the PIR1/PIR5 registers. The interrupt is enabled by setting the TMRx Match Interrupt Enable bit, TMRxIE of the PIE1/PIE5 registers. Interrupt Priority is selected with the TMRxIP bit in the IPR1/IPR5 registers.

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, TxOUTPS<3:0>, of the TxCON register.

13.3 Timer2/4/6 Output

The unscaled output of TMRx is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode. The timer to be used with a specific CCP module is selected using the CxTSEL<1:0> bits in the CCPTMRS0 and CCPTMRS1 registers.

Timer2 can be optionally used as the shift clock source for the MSSPx modules operating in SPI mode by setting SSPM<3:0> = 0011 in the SSPxCON1 register. Additional information is provided in **Section 15.0 “Master Synchronous Serial Port (MSSP1 and MSSP2) Module”**.

13.4 Timer2/4/6 Operation During Sleep

The Timer2/4/6 timers cannot be operated while the processor is in Sleep mode. The contents of the TMRx and PRx registers will remain unchanged while the processor is in Sleep mode.

13.5 Peripheral Module Disable

When a peripheral module is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module's clock source. The Module Disable bits for Timer2 (TMR2MD), Timer4 (TMR4MD) and Timer6 (TMR6MD) are in the PMD0 Register. See **Section 3.0 “Power-Managed Modes”** for more information.

PIC18(L)F2X/4XK22

15.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

- A low level is sampled on SDAx when SCLx goes from low level to high level (Case 1).
- SCLx goes low before SDAx is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDAx and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCLx pin is then deasserted and when sampled high, the SDAx pin is sampled.

If SDAx is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 15-36). If SDAx is sampled high, the BRG is reloaded and begins counting. If SDAx goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDAx at exactly the same time.

If SCLx goes from high-to-low before the BRG times out and SDAx has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 15-37.

If, at the end of the BRG time-out, both SCLx and SDAx are still high, the SDAx pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCLx pin, the SCLx pin is driven low and the Repeated Start condition is complete.

FIGURE 15-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

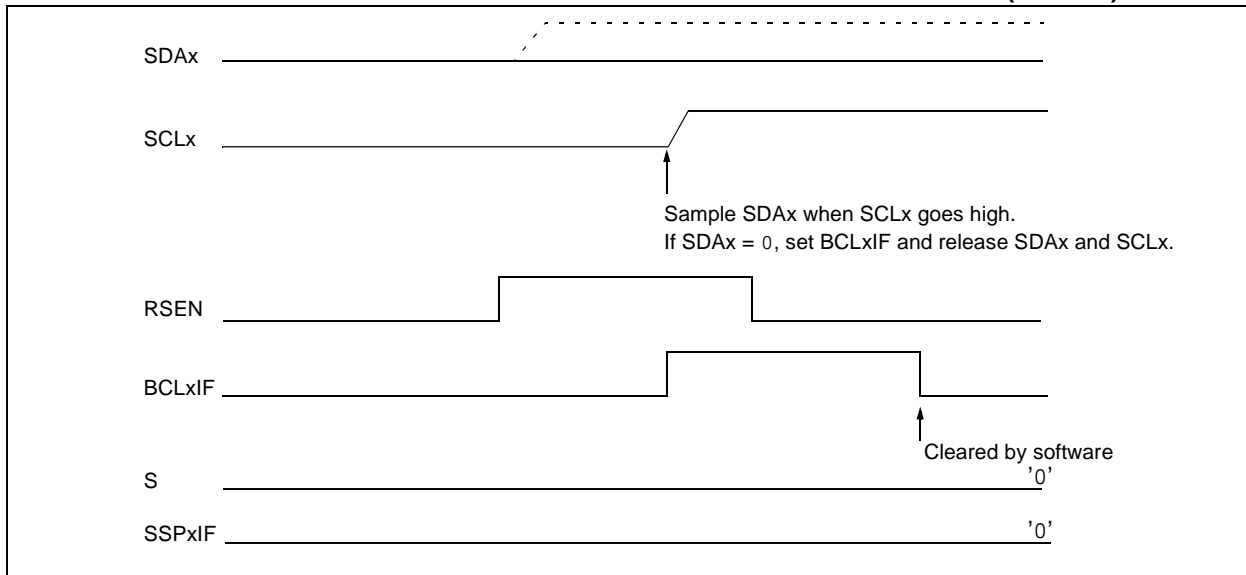
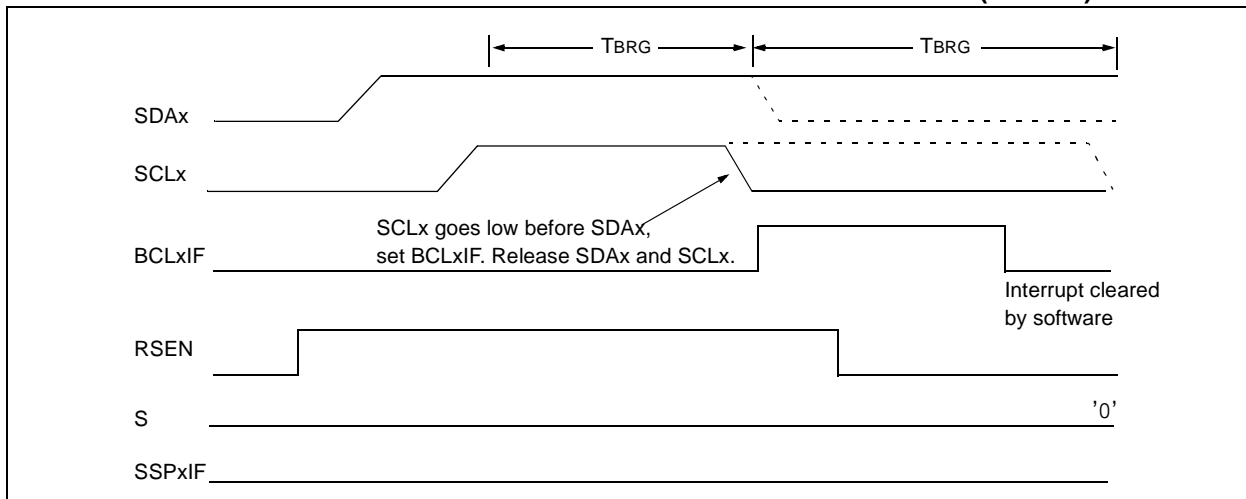


FIGURE 15-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



16.5.1.5 Synchronous Master Transmission Setup:

1. Initialize the SPBRGHx, SPBRGx register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 16.4 “EUSART Baud Rate Generator (BRG)”**).
2. Set the RXx/DTx and TXx/CKx TRIS controls to '1'.
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC. Set the TRIS bits corresponding to the RXx/DTx and TXx/CKx I/O pins.
4. Disable Receive mode by clearing bits SREN and CREN.
5. Enable Transmit mode by setting the TXEN bit.
6. If 9-bit transmission is desired, set the TX9 bit.
7. If interrupts are desired, set the TXxIE, GIE/GIEH and PEIE/GIEL interrupt enable bits.
8. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
9. Start transmission by loading data to the TXREGx register.

FIGURE 16-10: SYNCHRONOUS TRANSMISSION

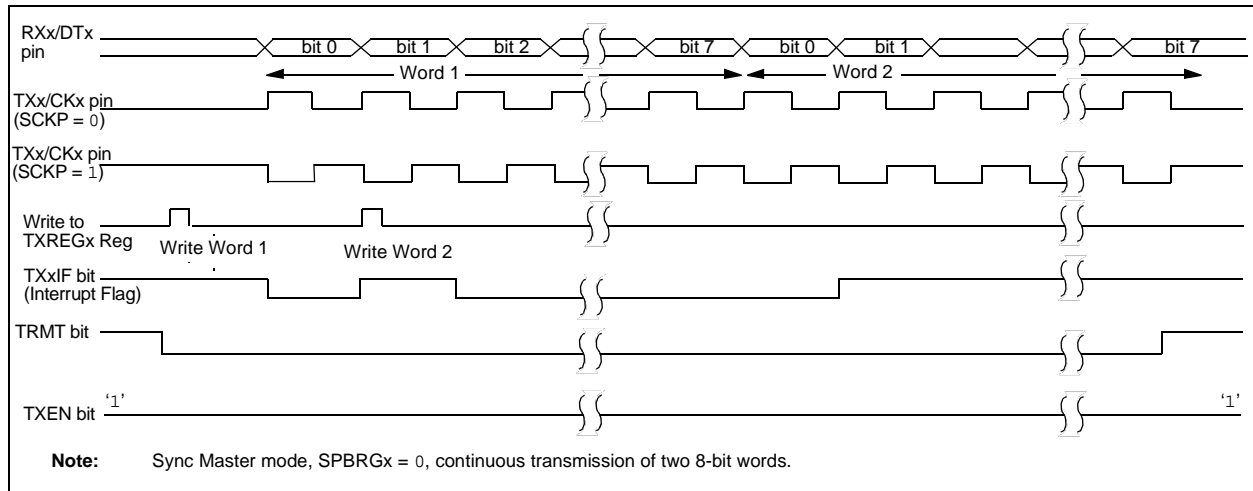
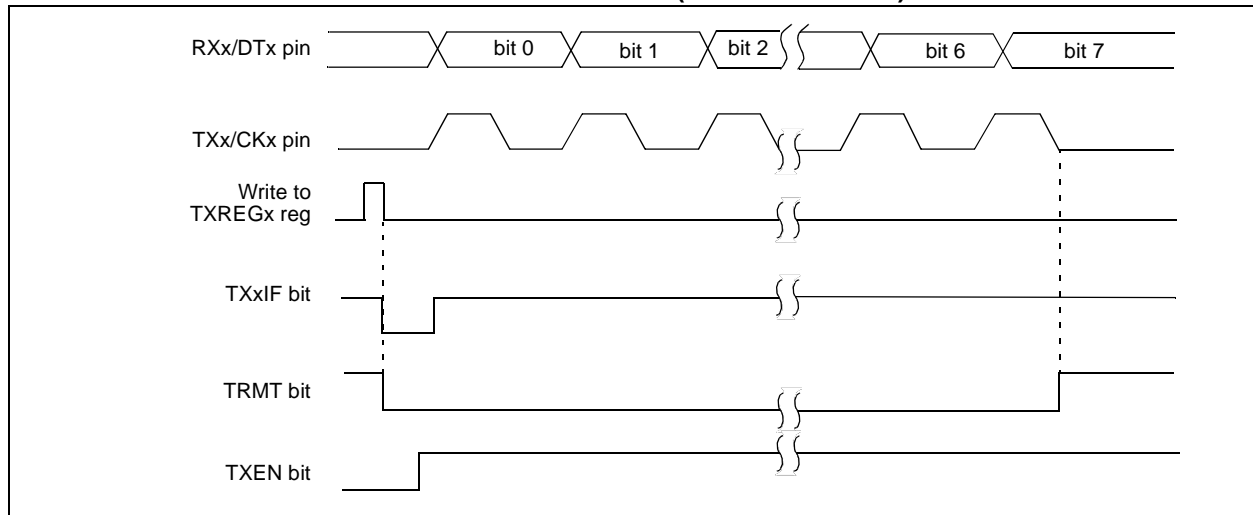


FIGURE 16-11: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



18.4 Comparator Interrupt Operation

The comparator interrupt flag will be set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 18-2). The first latch is updated with the comparator output value, when the CMxCON0 register is read or written. The value is latched on the third cycle of the system clock, also known as Q3. This first latch retains the comparator value until another read or write of the CMxCON0 register occurs or a Reset takes place. The second latch is updated with the comparator output value on every first cycle of the system clock, also known as Q1. When the output value of the comparator changes, the second latch is updated and the output values of both latches no longer match one another, resulting in a mismatch condition. The latch outputs are fed directly into the inputs of an exclusive-or gate. This mismatch condition is detected by the exclusive-or gate and sent to the interrupt circuitry. The mismatch condition will persist until the first latch value is updated by performing a read of the CMxCON0 register or the comparator output returns to the previous state.

Note 1: A write operation to the CMxCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

2: Comparator interrupts will operate correctly regardless of the state of CxOE.

When the mismatch condition occurs, the comparator interrupt flag is set. The interrupt flag is triggered by the edge of the changing value coming from the exclusive-or gate. This means that the interrupt flag can be reset once it is triggered without the additional step of reading or writing the CMxCON0 register to clear the mismatch latches. When the mismatch registers are cleared, an interrupt will occur upon the comparator's return to the previous state, otherwise no interrupt will be generated.

Software will need to maintain information about the status of the comparator output, as read from the CMxCON0 register, or CM2CON1 register, to determine the actual change that has occurred. See Figures 18-3 and 18-4.

The CxIF bit of the PIR2 register is the comparator interrupt flag. This bit must be reset by software by clearing it to '0'. Since it is also possible to write a '1' to this register, an interrupt can be generated.

In mid-range Compatibility mode the CxIE bit of the PIE2 register and the PEIE/GIE and GIE/GIEH bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR2 register will still be set if an interrupt condition occurs.

18.4.1 PRESETTING THE MISMATCH LATCHES

The comparator mismatch latches can be preset to the desired state before the comparators are enabled. When the comparator is off the CxPOL bit controls the CxOUT level. Set the CxPOL bit to the desired CxOUT non-interrupt level while the CxON bit is cleared. Then, configure the desired CxPOL level in the same instruction that the CxON bit is set. Since all register writes are performed as a read-modify-write, the mismatch latches will be cleared during the instruction read phase and the actual configuration of the CxON and CxPOL bits will occur in the final write phase.

FIGURE 18-3: COMPARATOR INTERRUPT TIMING W/O CMxCON0 READ

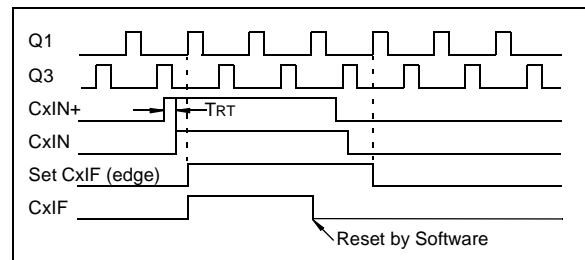
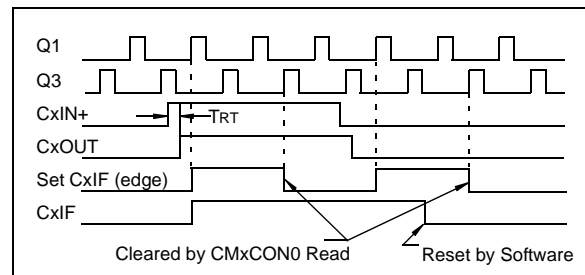


FIGURE 18-4: COMPARATOR INTERRUPT TIMING WITH CMxCON0 READ



Note 1: If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF interrupt flag of the PIR2 register may not get set.

2: When either comparator is first enabled, bias circuitry in the comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μ s for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

PIC18(L)F2X/4XK22

REGISTER 24-4: CONFIG3H: CONFIGURATION REGISTER 3 HIGH

R/P-1	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
MCLRE	—	P2BMX	T3CMX	HFOFST	CCP3MX	PBADEN	CCP2MX
bit 7							bit 0

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed x = Bit is unknown

- bit 7 **MCLRE:** $\overline{\text{MCLR}}$ Pin Enable bit
1 = $\overline{\text{MCLR}}$ pin enabled; RE3 input pin disabled
0 = RE3 input pin enabled; $\overline{\text{MCLR}}$ disabled
- bit 6 **Unimplemented:** Read as '0'
- bit 5 **P2BMX:** P2B Input MUX bit
1 = P2B is on RB5⁽¹⁾
 P2B is on RD2⁽²⁾
0 = P2B is on RC0
- bit 4 **T3CMX:** Timer3 Clock Input MUX bit
1 = T3CKI is on RC0
0 = T3CKI is on RB5
- bit 3 **HFOFST:** HFINTOSC Fast Start-up bit
1 = HFINTOSC starts clocking the CPU without waiting for the oscillator to stabilize
0 = The system clock is held off until the HFINTOSC is stable
- bit 2 **CCP3MX:** CCP3 MUX bit
1 = CCP3 input/output is multiplexed with RB5
0 = CCP3 input/output is multiplexed with RC6⁽¹⁾
 CCP3 input/output is multiplexed with RE0⁽²⁾
- bit 1 **PBADEN:** PORTB A/D Enable bit
1 = ANSELB<5:0> resets to 1, PORTB<5:0> pins are configured as analog inputs on Reset
0 = ANSELB<5:0> resets to 0, PORTB<4:0> pins are configured as digital I/O on Reset
- bit 0 **CCP2MX:** CCP2 MUX bit
1 = CCP2 input/output is multiplexed with RC1
0 = CCP2 input/output is multiplexed with RB3

Note 1: PIC18(L)F2XK22 devices only.

Note 2: PIC18(L)F4XK22 devices only.

PIC18(L)F2X/4XK22

BNC Branch if Not Carry

Syntax: BNC n

Operands: $-128 \leq n \leq 127$

Operation: if CARRY bit is '0'
 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding:

1110	0011	nnnn	nnnn
------	------	------	------

Description: If the CARRY bit is '0', then the program will branch.
 The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $PC + 2 + 2n$. This instruction is then a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
 If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNC Jump

Before Instruction
 PC = address (HERE)

After Instruction
 If CARRY = 0;
 PC = address (Jump)
 If CARRY = 1;
 PC = address (HERE + 2)

BNN Branch if Not Negative

Syntax: BNN n

Operands: $-128 \leq n \leq 127$

Operation: if NEGATIVE bit is '0'
 $(PC) + 2 + 2n \rightarrow PC$

Status Affected: None

Encoding:

1110	0111	nnnn	nnnn
------	------	------	------

Description: If the NEGATIVE bit is '0', then the program will branch.
 The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $PC + 2 + 2n$. This instruction is then a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
 If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNN Jump

Before Instruction
 PC = address (HERE)

After Instruction
 If NEGATIVE = 0;
 PC = address (Jump)
 If NEGATIVE = 1;
 PC = address (HERE + 2)

PIC18(L)F2X/4XK22

CLRF **Clear f**

Syntax: CLRF f{,a}

Operands: $0 \leq f \leq 255$
 $a \in [0,1]$

Operation: 000h → f
1 → Z

Status Affected: Z

Encoding:

0110	101a	ffff	ffff
------	------	------	------

Description: Clears the contents of the specified register.
If 'a' is '0', the Access Bank is selected.
If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: CLRF FLAG_REG, 1

Before Instruction
FLAG_REG = 5Ah

After Instruction
FLAG_REG = 00h

CLRWDT **Clear Watchdog Timer**

Syntax: CLRWDT

Operands: None

Operation: 000h → WDT,
000h → WDT postscaler,
1 → \overline{TO} ,
1 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Encoding:

0000	0000	0000	0100
------	------	------	------

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the postscaler of the WDT. Status bits, \overline{TO} and \overline{PD} , are set.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	No operation

Example: CLRWDT

Before Instruction
WDT Counter = ?

After Instruction
WDT Counter = 00h
WDT Postscaler = 0
 \overline{TO} = 1
 \overline{PD} = 1

PIC18(L)F2X/4XK22

27.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ^(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to V _{SS} (except V _{DD} , and $\overline{\text{MCLR}}$).....	-0.3V to (V _{DD} + 0.3V)
Voltage on V _{DD} with respect to V _{SS}	
PIC18LF24K22	-0.3V to +4.5V
PIC18(L)F26K22	-0.3V to +6.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS} (Note 2)	0V to +11.0V
Total power dissipation (Note 1).....	1.0W
Maximum current out of V _{SS} pin (-40°C to +85°C).....	300 mA
Maximum current out of V _{SS} pin (+85°C to +125°C).....	125 mA
Maximum current into V _{DD} pin (-40°C to +85°C).....	200 mA
Maximum current into V _{DD} pin (+85°C to +125°C)	85 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}).....	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin.....	25 mA
Maximum current sunk by all ports (-40°C to +85°C).....	200 mA
Maximum current sunk by all ports (+85°C to +125°C).....	110 mA
Maximum current sourced by all ports (-40°C to +85°C).....	185 mA
Maximum current sourced by all ports (+85°C to +125°C).....	70 mA

Note 1: Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

2: Voltage spikes below V_{SS} at the $\overline{\text{MCLR}}$ /V_{PP}/RE3 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ /V_{PP}/RE3 pin, rather than pulling this pin directly to V_{SS}.

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC18(L)F2X/4XK22

27.7 DC Characteristics: Secondary Oscillator Supply Current, PIC18(L)F2X/4XK22

PIC18LF2X/4XK22		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
PIC18F2X/4XK22		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$					
Param No.	Device Characteristics	Typ	Max	Units	Conditions		
D130	Supply Current (I_{DD}) ^{(1),(2)}	3.5	23	μA	-40°C	$V_{DD} = 1.8\text{V}$	Fosc = 32 kHz (SEC_RUN mode, SOSC source)
		3.7	25	μA	$+25^{\circ}\text{C}$		
		3.8	—	μA	$+60^{\circ}\text{C}$		
		4.0	28	μA	$+85^{\circ}\text{C}$		
		5.1	30	μA	$+125^{\circ}\text{C}$		
D131		6.2	26	μA	-40°C	$V_{DD} = 3.0\text{V}$	
		6.4	30	μA	$+25^{\circ}\text{C}$		
		6.5	—	μA	$+60^{\circ}\text{C}$		
		6.8	35	μA	$+85^{\circ}\text{C}$		
		7.8	40	μA	$+125^{\circ}\text{C}$		
D132		15	35	μA	-40°C	$V_{DD} = 2.3\text{V}$	Fosc = 32 kHz (SEC_RUN mode, SOSC source)
		16	35	μA	$+25^{\circ}\text{C}$		
		17	35	μA	$+85^{\circ}\text{C}$		
		19	50	μA	$+125^{\circ}\text{C}$		
D133		18	50	μA	-40°C	$V_{DD} = 3.0\text{V}$	
		19	50	μA	$+25^{\circ}\text{C}$		
		21	50	μA	$+85^{\circ}\text{C}$		
		22	60	μA	$+125^{\circ}\text{C}$		
D134		19	55	μA	-40°C	$V_{DD} = 5.0\text{V}$	
		20	55	μA	$+25^{\circ}\text{C}$		
		22	55	μA	$+85^{\circ}\text{C}$		
		23	70	μA	$+125^{\circ}\text{C}$		

Note 1: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

Test condition: All Peripheral Module Control bits in PMD0, PMD1 and PMD2 set to '1'.

Note 2: The test conditions for all I_{DD} measurements in active operation mode are:

All I/O pins set as outputs driven to V_{SS} ;

MCLR = V_{DD} ;

SOSCI / SOSCO = complementary external square wave, from rail-to-rail.

PIC18(L)F2X/4XK22

TABLE 27-3: FIXED VOLTAGE REFERENCE (FVR) SPECIFICATIONS

Operating Conditions: $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ (unless otherwise stated)							
Param No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
VR01	VROUT	VR voltage output to ADC	0.973	1.024	1.085	V	1x output, $V_{DD} \geq 2.5\text{V}$
			1.946	2.048	2.171	V	2x output, $V_{DD} \geq 2.5\text{V}$
			3.891	4.096	4.342	V	4x output, $V_{DD} \geq 4.75\text{V}$ (PIC18F2X/4XK22)
VR02	VROUT	VR voltage output all other modules	0.942	1.024	1.096	V	1x output, $V_{DD} \geq 2.5\text{V}$
			1.884	2.048	2.191	V	2x output, $V_{DD} \geq 2.5\text{V}$
			3.768	4.096	4.383	V	4x output, $V_{DD} \geq 4.75\text{V}$ (PIC18F2X/4XK22)
VR04*	TSTABLE	Settling Time	—	25	100	μs	0 to 125°C

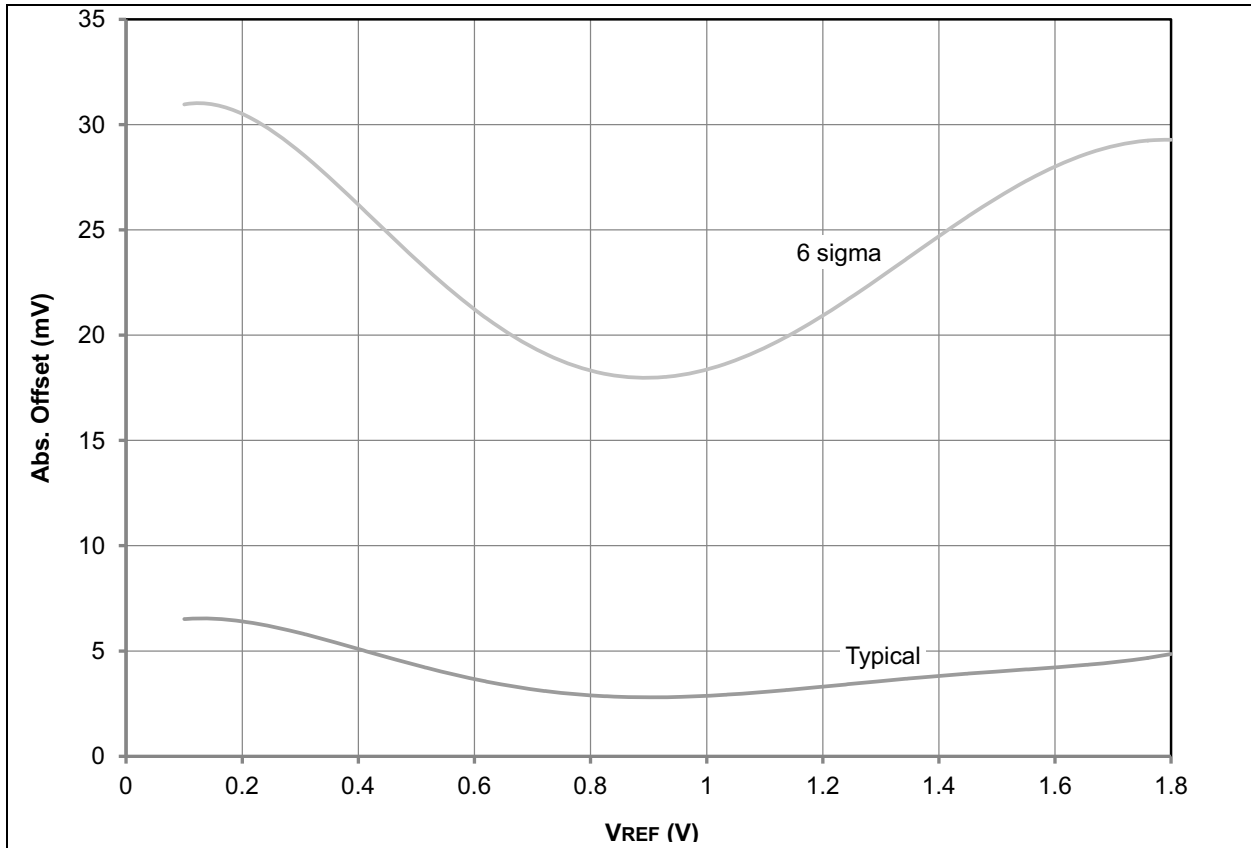
* These parameters are characterized but not tested.

TABLE 27-4: CHARGE TIME MEASUREMENT UNIT (CTMU) SPECIFICATIONS

Operating Conditions: $1.8\text{V} < V_{DD} < 5.5\text{V}$, $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ (unless otherwise stated)							
Param No.	Sym	Characteristics	Min	Typ ⁽¹⁾	Max	Units	Comments
CT01	IOUT1	CTMU Current Source, Base Range	—	0.55	—	μA	IRNG<1:0>=01
CT02	IOUT2	CTMU Current Source, 10X Range	—	5.5	—	μA	IRNG<1:0>=10
CT03	IOUT3	CTMU Current Source, 100X Range	—	55	—	μA	IRNG<1:0>=11 $V_{DD} \geq 3.0\text{V}$

Note 1: Nominal value at center point of current trim range (CTMUICON<7:2>=000000).

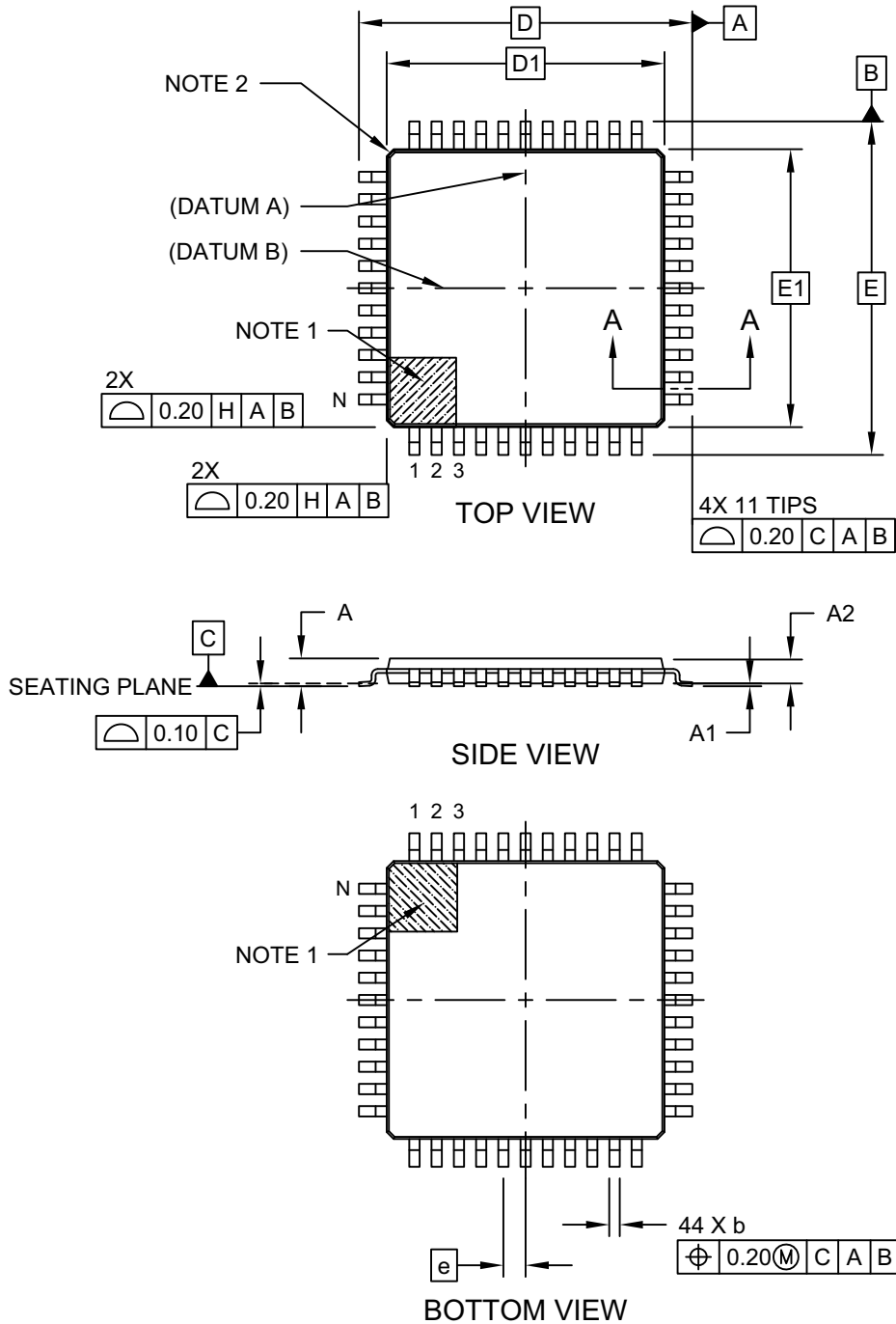
FIGURE 28-89: PIC18LF2X/4XK22 COMPARATOR OFFSET VOLTAGE, NORMAL-POWER MODE; $V_{DD}=1.8V$



PIC18(L)F2X/4XK22

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

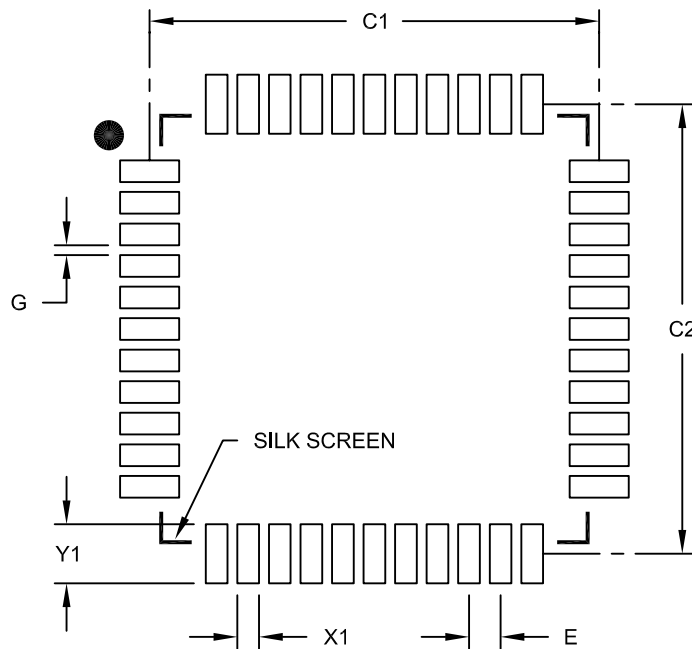


Microchip Technology Drawing C04-076C Sheet 1 of 2

PIC18(L)F2X/4XK22

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B