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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f23k22t-i-so

PIC18(L)F2X/4XK22

1.2 Other Special Features

- **Memory Endurance:** The Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 10K for program memory and 100K for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18(L)F2X/4XK22 family introduces an optional extension to the PIC18 instruction set, which adds eight new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.
- **Enhanced CCP module:** In PWM mode, this module provides one, two or four modulated outputs for controlling half-bridge and full-bridge drivers. Other features include:
 - Auto-Shutdown, for disabling PWM outputs on interrupt or other select conditions
 - Auto-Restart, to reactivate outputs once the condition has cleared
 - Output steering to selectively enable one or more of four outputs to provide the PWM signal.
- **Enhanced Addressable EUSART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **10-bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit postscaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 27.0 “Electrical Specifications”** for time-out periods.
- **Charge Time Measurement Unit (CTMU)**
- **SR Latch Output:**

1.3 Details on Individual Family Members

Devices in the PIC18(L)F2X/4XK22 family are available in 28-pin and 40/44-pin packages. The block diagram for the device family is shown in Figure 1-1.

The devices have the following differences:

1. Flash program memory
2. Data Memory SRAM
3. Data Memory EEPROM
4. A/D channels
5. I/O ports
6. ECCP modules (Full/Half Bridge)
7. Input Voltage Range/Power Consumption

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in the pin summary tables: Table 2 and Table 3, and I/O description tables: Table 1-2 and Table 1-3.

2.2 Oscillator Control

The OSCCON, OSCCON2 and OSCTUNE registers (Register 2-1 to Register 2-3) control several aspects of the device clock's operation, both in full-power operation and in power-managed modes.

- Main System Clock Selection (SCS)
- Primary Oscillator Circuit Shutdown (PRISD)
- Secondary Oscillator Enable (SOSCGO)
- Primary Clock Frequency 4x multiplier (PLLEN)
- Internal Frequency selection bits (IRCF, INTSRC)
- Clock Status bits (OSTS, HFIOFS, MFIOFS, LFIOFS, SOSCRUN, PLLRDY)
- Power management selection (IDLEN)

2.2.1 MAIN SYSTEM CLOCK SELECTION

The System Clock Select bits, SCS<1:0>, select the main clock source. The available clock sources are

- Primary clock defined by the FOSC<3:0> bits of CONFIG1H. The primary clock can be the primary oscillator, an external clock, or the internal oscillator block.
- Secondary clock (secondary oscillator)
- Internal oscillator block (HFINTOSC, MFINTOSC and LFINTOSC).

The clock source changes immediately after one or more of the bits is written to, following a brief clock transition interval. The SCS bits are cleared to select the primary clock on all forms of Reset.

2.2.2 INTERNAL FREQUENCY SELECTION

The Internal Oscillator Frequency Select bits (IRCF<2:0>) select the frequency output of the internal oscillator block. The choices are the LFINTOSC source (31.25 kHz), the MFINTOSC source (31.25 kHz, 250 kHz or 500 kHz) and the HFINTOSC source (16 MHz) or one of the frequencies derived from the HFINTOSC postscaler (31.25 kHz to 8 MHz). If the internal oscillator block is supplying the main clock, changing the states of these bits will have an immediate change on the internal oscillator's output. On device Resets, the output frequency of the internal oscillator is set to the default frequency of 1 MHz.

2.2.3 LOW FREQUENCY SELECTION

When a nominal output frequency of 31.25 kHz is selected (IRCF<2:0> = 000), users may choose which internal oscillator acts as the source. This is done with the INTSRC bit of the OSCTUNE register and MFIOSEL bit of the OSCCON2 register. See Figure 2-2 and Register 2-1 for specific 31.25 kHz selection. This option allows users to select a 31.25 kHz clock (MFINTOSC or HFINTOSC) that can be tuned using the TUN<5:0> bits in OSCTUNE register, while maintaining power savings with a very low clock speed. LFINTOSC always remains the clock source for features such as the Watchdog Timer and the Fail-Safe Clock Monitor, regardless of the setting of INTSRC and MFIOSEL bits

This option allows users to select the tunable and more precise HFINTOSC as a clock source, while maintaining power savings with a very low clock speed.

2.2.4 POWER MANAGEMENT

The IDLEN bit of the OSCCON register determines whether the device goes into Sleep mode or one of the Idle modes when the SLEEP instruction is executed.

FIGURE 2-11: FSCM TIMING DIAGRAM

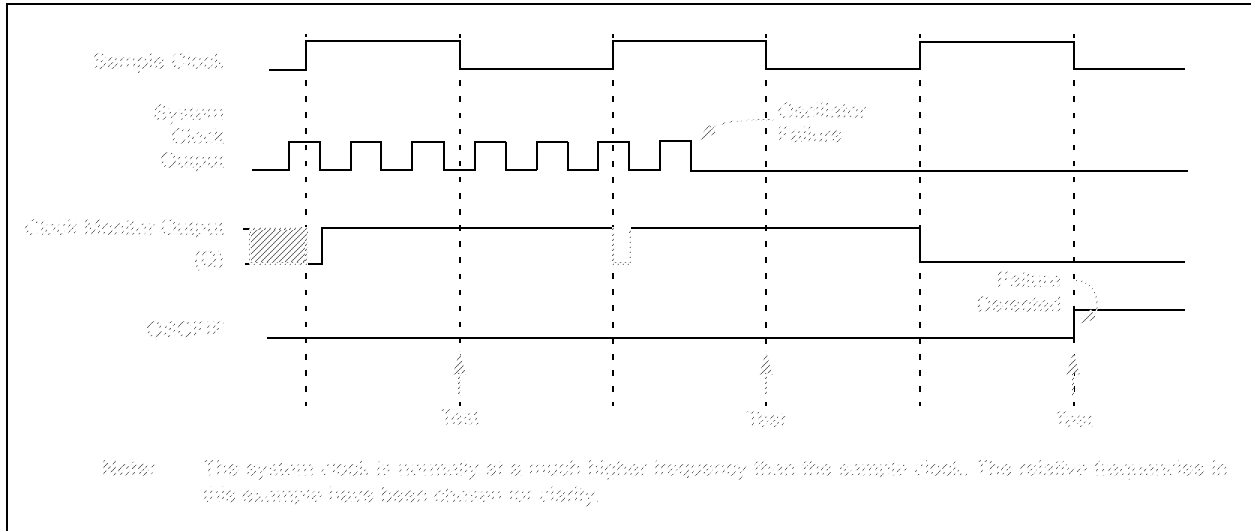


TABLE 2-4: REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	109
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	122
OSCCON	IDLEN	IRCF<2:0>			OSTS	HFIOFS	SCS<1:0>		30
OSCCON2	PLLRDY	SOSCRUN	—	MFIOSEL	SOSCGO	PRISD	MFIOFS	LFIOFS	31
OSCTUNE	INTSRC	PLEN	TUN<5:0>						35
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	118
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	113

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used by clock sources.

TABLE 2-5: CONFIGURATION REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONFIG1H	IESO	FCMEN	PRICLKEN	PLLCFG	FOSC<3:0>				345
CONFIG2L	—	—	—	BORV<1:0>		BOREN<1:0>		PWRTEN	346
CONFIG3H	MCLRE	—	P2BMX	T3CMX	HFOFST	CCP3MX	PBADEN	CCP2MX	348

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for clock sources.

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REGISTER 3-2: PMD1: PERIPHERAL MODULE DISABLE REGISTER 1

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MSSP2MD	MSSP1MD	—	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 7 **MSSP2MD:** MSSP2 Peripheral Module Disable Control bit
 1 = Module is disabled, Clock Source is disconnected, module does not draw digital power
 0 = Module is enabled, Clock Source is connected, module draws digital power
- bit 6 **MSSP1MD:** MSSP1 Peripheral Module Disable Control bit
 1 = Module is disabled, Clock Source is disconnected, module does not draw digital power
 0 = Module is enabled, Clock Source is connected, module draws digital power
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **CCP5MD:** CCP5 Peripheral Module Disable Control bit
 1 = Module is disabled, Clock Source is disconnected, module does not draw digital power
 0 = Module is enabled, Clock Source is connected, module draws digital power
- bit 3 **CCP4MD:** CCP4 Peripheral Module Disable Control bit
 1 = Module is disabled, Clock Source is disconnected, module does not draw digital power
 0 = Module is enabled, Clock Source is connected, module draws digital power
- bit 2 **CCP3MD:** CCP3 Peripheral Module Disable Control bit
 1 = Module is disabled, Clock Source is disconnected, module does not draw digital power
 0 = Module is enabled, Clock Source is connected, module draws digital power
- bit 1 **CCP2MD:** CCP2 Peripheral Module Disable Control bit
 1 = Module is disabled, Clock Source is disconnected, module does not draw digital power
 0 = Module is enabled, Clock Source is connected, module draws digital power
- bit 0 **CCP1MD:** CCP1 Peripheral Module Disable Control bit
 1 = Module is disabled, Clock Source is disconnected, module does not draw digital power
 0 = Module is enabled, Clock Source is connected, module draws digital power

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REGISTER 9-15: IPR2: PERIPHERAL INTERRUPT PRIORITY REGISTER 2

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
OSCFIP	C1IP	C2IP	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **OSCFIP:** Oscillator Fail Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 6 **C1IP:** Comparator C1 Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 5 **C2IP:** Comparator C2 Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 4 **EEIP:** Data EEPROM/Flash Write Operation Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 3 **BCL1IP:** MSSP1 Bus Collision Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 2 **HLVDIP:** Low-Voltage Detect Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 1 **TMR3IP:** TMR3 Overflow Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 0 **CCP2IP:** CCP2 Interrupt Priority bit
 1 = High priority
 0 = Low priority

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TABLE 10-14: PORTE I/O SUMMARY

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RE0/P3A/CCP3/AN5	RE0	0	0	O	DIG	LATE<0> data output; not affected by analog input.
		1	0	I	ST	PORTE<0> data input; disabled when analog input enabled.
	P3A ⁽¹⁾	0	0	O	DIG	Enhanced CCP3 PWM output.
	CCP3 ⁽¹⁾	0	0	O	DIG	Compare 3 output/PWM 3 output.
		1	0	I	ST	Capture 3 input.
AN5	1	1	I	AN	Analog input 5.	
RE1/P3B/AN6	RE1	0	0	O	DIG	LATE<1> data output; not affected by analog input.
		1	0	I	ST	PORTE<1> data input; disabled when analog input enabled.
	P3B	0	0	O	DIG	Enhanced CCP3 PWM output.
RE2/CCP5/AN7	RE2	0	0	O	DIG	LATE<2> data output; not affected by analog input.
		1	0	I	ST	PORTE<2> data input; disabled when analog input enabled.
	CCP5	0	0	O	DIG	Compare 5 output/PWM 5 output.
		1	0	I	ST	Capture 5 input.
	AN7	1	1	I	AN	Analog input 7.
RE3/VPP/MCLR	RE3	—	—	I	ST	PORTE<3> data input; enabled when Configuration bit MCLRE = 0.
	VPP	—	—	P	AN	Programming voltage input; always available
	MCLR	—	—	I	ST	Active-low Master Clear (device Reset) input; enabled when configuration bit MCLRE = 1.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I²C = Schmitt Trigger input with I²C.

Note 1: Alternate pin assignment for P3A/CCP3 when Configuration bit CCP3MX is clear.

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TABLE 14-5: REGISTERS ASSOCIATED WITH COMPARE (CONTINUED)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	122
IPR4	—	—	—	—	—	CCP5IP	CCP4IP	CCP3IP	124
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	117
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	118
PIE4	—	—	—	—	—	CCP5IE	CCP4IE	CCP3IE	120
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	112
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	113
PIR4	—	—	—	—	—	CCP5IF	CCP4IF	CCP3IF	115
PMD0	UART2MD	UART1MD	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	52
PMD1	MSSP2MD	MSSP1MD	—	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD	53
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1SOSCEN	T1SYNC	T1RD16	TMR1ON	166
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/DONE	T1GVAL	T1GSS<1:0>		167
T3CON	TMR3CS<1:0>		T3CKPS<1:0>		T3SOSCEN	T3SYNC	T3RD16	TMR3ON	166
T3GCON	TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/DONE	T3GVAL	T3GSS<1:0>		167
T5CON	TMR5CS<1:0>		T5CKPS<1:0>		T5SOSCEN	T5SYNC	T5RD16	TMR5ON	166
T5GCON	TMR5GE	T5GPOL	T5GTM	T5GSPM	T5GGO/DONE	T5GVAL	T5GSS<1:0>		167
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								—
TMR1L	Least Significant Byte of the 16-bit TMR1 Register								—
TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								—
TMR3L	Least Significant Byte of the 16-bit TMR3 Register								—
TMR5H	Holding Register for the Most Significant Byte of the 16-bit TMR5 Register								—
TMR5L	Least Significant Byte of the 16-bit TMR5 Register								—
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	151
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	151
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	151
TRISD ⁽¹⁾	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	151
TRISE	WPUE3	—	—	—	—	TRISE2 ⁽¹⁾	TRISE1 ⁽¹⁾	TRISE0 ⁽¹⁾	151

Legend: — = Unimplemented location, read as '0'. Shaded bits are not used by Compare mode.

Note 1: These registers/bits are available on PIC18(L)F4XK22 devices.

TABLE 14-6: CONFIGURATION REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONFIG3H	MCLRE	—	P2BMX	T3CMX	HFOFST	CCP3MX	PBADEN	CCP2MX	348

Legend: — = Unimplemented location, read as '0'. Shaded bits are not used by Compare mode.

6. Configure and start the 8-bit TimerX resource:
 - Clear the TMRxIF interrupt flag bit of the PIR2 or PIR4 register. See Note 1 below.
 - Configure the TxCKPS bits of the TxCON register with the Timer prescale value.
 - Enable the Timer by setting the TMRxON bit of the TxCON register.
7. Enable PWM output pin:
 - Wait until the Timer overflows and the TMRxIF bit of the PIR2 or PIR4 register is set. See Note 1 below.
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.

Note 1: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

14.3.3 PWM TIMER RESOURCE

The PWM standard mode makes use of one of the 8-bit Timer2/4/6 timer resources to specify the PWM period.

Configuring the CxTSEL<1:0> bits in the CCPTMRS0 or CCPTMRS1 register selects which Timer2/4/6 timer is used.

14.3.4 PWM PERIOD

The PWM period is specified by the PRx register of 8-bit TimerX. The PWM period can be calculated using the formula of Equation 14-1.

EQUATION 14-1: PWM PERIOD

$$PWM\ Period = [(PRx) + 1] \cdot 4 \cdot TOSC \cdot (TMRx\ Prescale\ Value)$$

Note 1: $TOSC = 1/FOSC$

When TMRx is equal to PRx, the following three events occur on the next increment cycle:

- TMRx is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer postscaler (see **Section 13.0 “Timer2/4/6 Module”**) is not used in the determination of the PWM frequency.

14.3.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSBs and the DCxB<1:0> bits of the CCPxCON register contain the two LSBs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PRx and TMRx registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 14-2 is used to calculate the PWM pulse width.

Equation 14-3 is used to calculate the PWM duty cycle ratio.

EQUATION 14-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxL:CCPxCON<5:4>) \cdot TOSC \cdot (TMRx\ Prescale\ Value)$$

EQUATION 14-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxL:CCPxCON<5:4>)}{4(PRx + 1)}$$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMRx register is concatenated with either the 2-bit internal system clock (Fosc), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the TimerX prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 14-4).

14.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCPx/PxA pin, while the complementary PWM output signal is output on the PxB pin (see Figure 14-9). This mode can be used for half-bridge applications, as shown in Figure 14-9, or for full-bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in half-bridge power devices. The value of the PDC<6:0> bits of the PWMxCON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 14.4.5 “Programmable Dead-Band Delay Mode”** for more details of the dead-band delay operations.

Since the PxA and PxB outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure PxA and PxB as outputs.

FIGURE 14-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

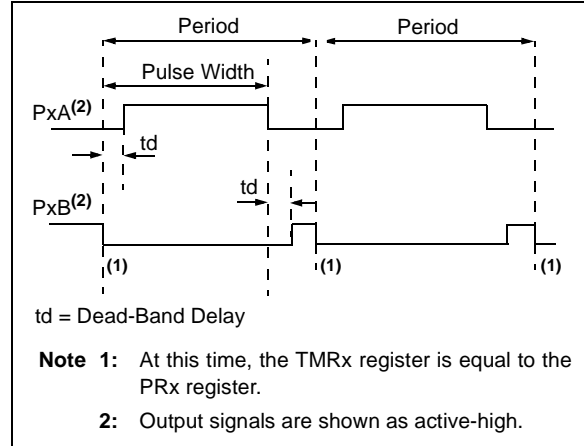
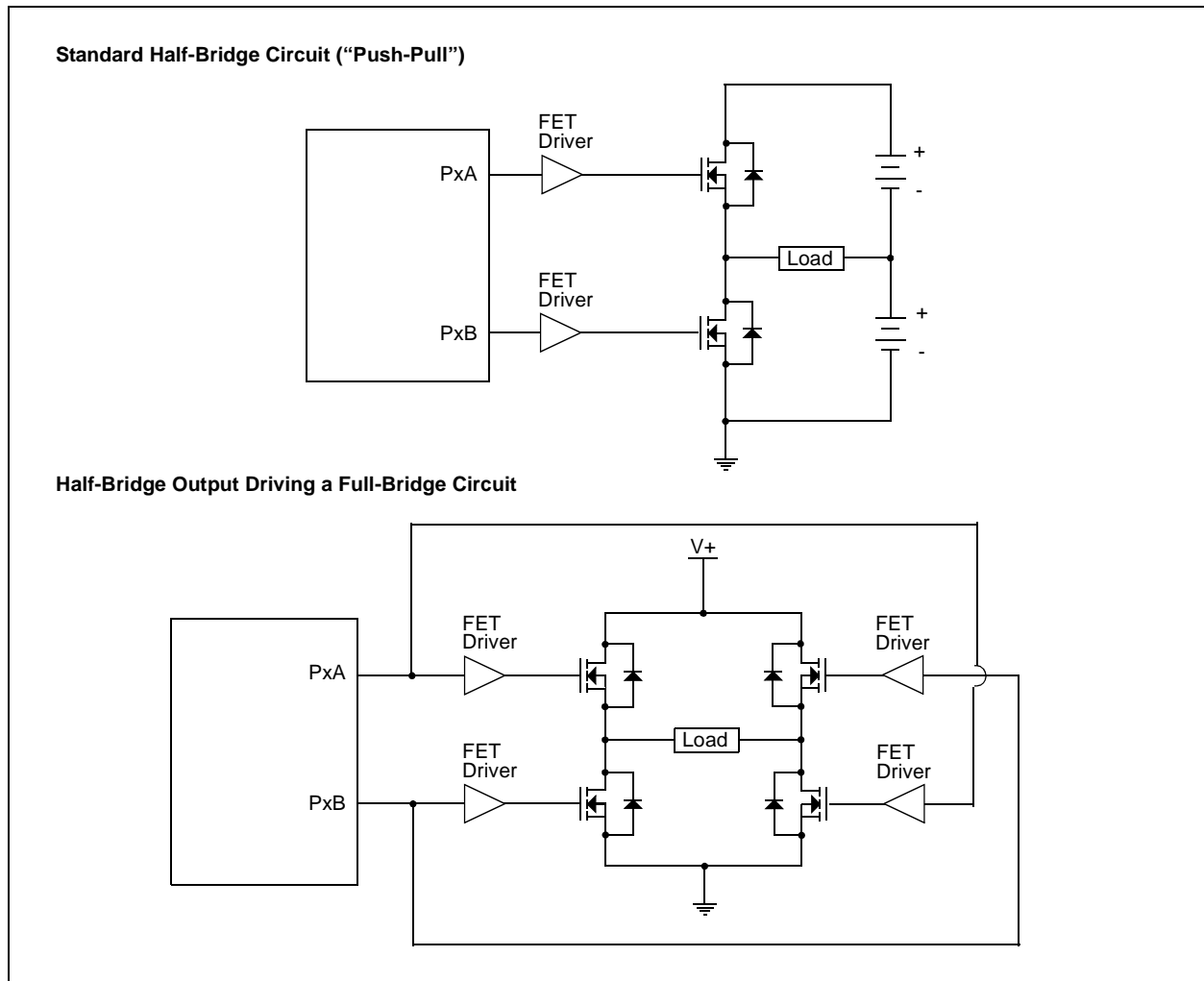


FIGURE 14-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS



16.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a V_{OH} Mark state which represents a '1' data bit, and a V_{OL} Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 16-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

16.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 16-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREGx register.

16.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTAx register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTAx register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTAx register enables the EUSART and automatically configures the TXx/CKx I/O pin as an output. If the TXx/CKx pin is shared with an analog peripheral the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note: The TXxIF transmitter interrupt flag is set when the TXEN enable bit is set.

16.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREGx register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREGx is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREGx until the Stop bit of the previous character has been transmitted. The pending character in the TXREGx is then transferred to the TSR in one T_{cy} immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREGx.

16.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the CKTXP bit of the BAUDCONx register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the CKTXP bit to '1' will invert the transmit data resulting in low true idle and data bits. The CKTXP bit controls transmit data polarity only in Asynchronous mode. In Synchronous mode the CKTXP bit has a different function.

16.1.1.4 Transmit Interrupt Flag

The TXxIF interrupt flag bit of the PIR1/PIR3 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREGx. In other words, the TXxIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREGx. The TXxIF flag bit is not cleared immediately upon writing TXREGx. TXxIF becomes valid in the second instruction cycle following the write execution. Polling TXxIF immediately following the TXREGx write will return invalid results. The TXxIF bit is read-only, it cannot be set or cleared by software.

The TXxIF interrupt can be enabled by setting the TXxIE interrupt enable bit of the PIE1/PIE3 register. However, the TXxIF flag bit will be set whenever the TXREGx is empty, regardless of the state of TXxIE enable bit.

To use interrupts when transmitting data, set the TXxIE bit only when there is more data to send. Clear the TXxIE interrupt enable bit upon writing the last character of the transmission to the TXREGx.

PIC18(L)F2X/4XK22

REGISTER 16-3: BAUDCONx: BAUD RATE CONTROL REGISTER

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN
bit 7						bit 0	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7 **ABDOVF:** Auto-Baud Detect Overflow bit
Asynchronous mode:
 1 = Auto-baud timer overflowed
 0 = Auto-baud timer did not overflow
Synchronous mode:
 Don't care
- bit 6 **RCIDL:** Receive Idle Flag bit
Asynchronous mode:
 1 = Receiver is Idle
 0 = Start bit has been detected and the receiver is active
Synchronous mode:
 Don't care
- bit 5 **DTRXP:** Data/Receive Polarity Select bit
Asynchronous mode:
 1 = Receive data (RXx) is inverted (active-low)
 0 = Receive data (RXx) is not inverted (active-high)
Synchronous mode:
 1 = Data (DTx) is inverted (active-low)
 0 = Data (DTx) is not inverted (active-high)
- bit 4 **CKTXP:** Clock/Transmit Polarity Select bit
Asynchronous mode:
 1 = Idle state for transmit (TXx) is low
 0 = Idle state for transmit (TXx) is high
Synchronous mode:
 1 = Data changes on the falling edge of the clock and is sampled on the rising edge of the clock
 0 = Data changes on the rising edge of the clock and is sampled on the falling edge of the clock
- bit 3 **BRG16:** 16-bit Baud Rate Generator bit
 1 = 16-bit Baud Rate Generator is used (SPBRGHx:SPBRGx)
 0 = 8-bit Baud Rate Generator is used (SPBRGx)
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
 1 = Receiver is waiting for a falling edge. No character will be received but RCxIF will be set on the falling edge. WUE will automatically clear on the rising edge.
 0 = Receiver is operating normally
Synchronous mode:
 Don't care
- bit 0 **ABDEN:** Auto-Baud Detect Enable bit
Asynchronous mode:
 1 = Auto-Baud Detect mode is enabled (clears when auto-baud is complete)
 0 = Auto-Baud Detect mode is disabled
Synchronous mode:
 Don't care

18.8 Additional Comparator Features

There are four additional comparator features:

- Simultaneous read of comparator outputs
- Internal reference selection
- Hysteresis selection
- Output Synchronization

18.8.1 SIMULTANEOUS COMPARATOR OUTPUT READ

The MC1OUT and MC2OUT bits of the CM2CON1 register are mirror copies of both comparator outputs. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note 1: Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

18.8.2 INTERNAL REFERENCE SELECTION

There are two internal voltage references available to the non-inverting input of each comparator. One of these is the Fixed Voltage Reference (FVR) and the other is the variable Digital-to-Analog Converter (DAC). The CxRSEL bit of the CM2CON1 register determines which of these references is routed to the Comparator Voltage reference output (CxVREF). Further routing to the comparator is accomplished by the CxR bit of the CMxCON0 register. See **Section 21.0 “Fixed Voltage Reference (FVR)”** and Figure 18-2 for more detail.

18.8.3 COMPARATOR HYSTERESIS

Each Comparator has a selectable hysteresis feature. The hysteresis can be enabled by setting the CxHYS bit of the CM2CON1 register. See **Section 27.0 “Electrical Specifications”** for more details.

18.8.4 SYNCHRONIZING COMPARATOR OUTPUT TO TIMER1

The Comparator Cx output can be synchronized with Timer1 by setting the CxSYNC bit of the CM2CON1 register. When enabled, the Cx output is latched on the falling edge of the Timer1 source clock. To prevent a race condition when gating Timer1 clock with the comparator output, Timer1 increments on the rising edge of its clock source, and the falling edge latches the comparator output. See the Comparator Block Diagram (Figure 18-2) and the Timer1 Block Diagram (Figure 12-1) for more information.

Note 1: The comparator synchronized output should not be used to gate the external Timer1 clock when the Timer1 synchronizer is enabled.

- 2:** The Timer1 prescale should be set to 1:1 when synchronizing the comparator output as unexpected results may occur with other prescale values.

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20.0 SR LATCH

The module consists of a single SR latch with multiple Set and Reset inputs as well as separate latch outputs. The SR latch module includes the following features:

- Programmable input selection
- SR latch output is available internally/externally
- Selectable Q and \bar{Q} output
- Firmware Set and Reset

The SR latch can be used in a variety of analog applications, including oscillator circuits, one-shot circuit, hysteretic controllers, and analog timing applications.

20.1 Latch Operation

The latch is a Set-Reset latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. The latch can be set or reset by:

- Software control (SRPS and SRPR bits)
- Comparator C1 output (sync_C1OUT)
- Comparator C2 output (sync_C2OUT)
- SRI Pin
- Programmable clock (DIVSRCLK)

The SRPS and the SRPR bits of the SRCON0 register may be used to set or reset the SR latch, respectively. The latch is Reset-dominant. Therefore, if both Set and Reset inputs are high, the latch will go to the Reset state. Both the SRPS and SRPR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

The output from Comparator C1 or C2 can be used as the Set or Reset inputs of the SR latch. The output of either Comparator can be synchronized to the Timer1 clock source. See **Section 18.0 “Comparator Module”** and **Section 12.0 “Timer1/3/5 Module with Gate Control”** for more information.

An external source on the SRI pin can be used as the Set or Reset inputs of the SR latch.

An internal clock source, DIVSRCLK, is available and it can periodically set or reset the SR latch. The SRCLK<2:0> bits in the SRCON0 register are used to select the clock source period. The SRSCKE and SRRCKE bits of the SRCON1 register enable the clock source to set or reset the SR latch, respectively.

20.2 Latch Output

The SRQEN and SRNQEN bits of the SRCON0 register control the Q and \bar{Q} latch outputs. Both of the SR latch outputs may be directly output to I/O pins at the same time. Control is determined by the state of bits SRQEN and SRNQEN in the SRCON0 register.

The applicable TRIS bit of the corresponding port must be cleared to enable the port pin output driver.

20.3 DIVSRCLK Clock Generation

The DIVSRCLK clock signal is generated from the peripheral clock which is pre-scaled by a value determined by the SRCLK<2:0> bits. See Figure 20-2 and Table 20-1 for additional detail.

20.4 Effects of a Reset

Upon any device Reset, the SR latch is not initialized, and the SRQ and SRNQ outputs are unknown. The user's firmware is responsible to initialize the latch output before enabling it to the output pins.

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REGISTER 22-2: VREFCON2: VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DACR<4:0>				
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-5 **Unimplemented:** Read as '0'
bit 4-0 **DACR<4:0>:** DAC Voltage Output Select bits
 $V_{OUT} = ((V_{SRC+}) - (V_{SRC-})) * (DACR<4:0> / (2^5)) + V_{SRC-}$

TABLE 22-1: REGISTERS ASSOCIATED WITH DAC MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
VREFCON0	FVREN	FVRST	FVRS<1:0>		—	—	—	—	332
VREFCON1	DACEN	DACLPS	DACOE	—	DACPSS<1:0>		—	DACNSS	335
VREFCON2	—	—	—	DACR<4:0>					336

Legend: — = Unimplemented locations, read as '0'. Shaded bits are not used by the DAC module.

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REGISTER 24-11: CONFIG7H: CONFIGURATION REGISTER 7 HIGH

U-0	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
—	EBTRB	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

C = Clearable only bit

bit 7 **Unimplemented:** Read as '0'

bit 6 **EBTRB:** Boot Block Table Read Protection bit

1 = Boot Block not protected from table reads executed in other blocks

0 = Boot Block protected from table reads executed in other blocks

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 24-12: DEVID1: DEVICE ID REGISTER 1

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:

R = Readable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

C = Clearable only bit

bit 7-5 **DEV<2:0>:** Device ID bits

These bits, together with DEV<10:3> in DEVID2, determine the device ID.
See Table 24-2 for complete Device ID list.

bit 4-0 **REV<4:0>:** Revision ID bits

These bits indicate the device revision.

REGISTER 24-13: DEVID2: DEVICE ID REGISTER 2

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

Legend:

R = Readable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

C = Clearable only bit

bit 7-0 **DEV<10:3>:** Device ID bits

These bits, together with DEV<2:0> in DEVID1, determine the device ID.
See Table 24-2 for complete Device ID list.

26.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

26.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

26.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

26.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

PIC18(L)F2X/4XK22

FIGURE 28-30: PIC18LF2X/4XK22 TYPICAL I_{DD} : RC_RUN HF-INTOSC with PLL

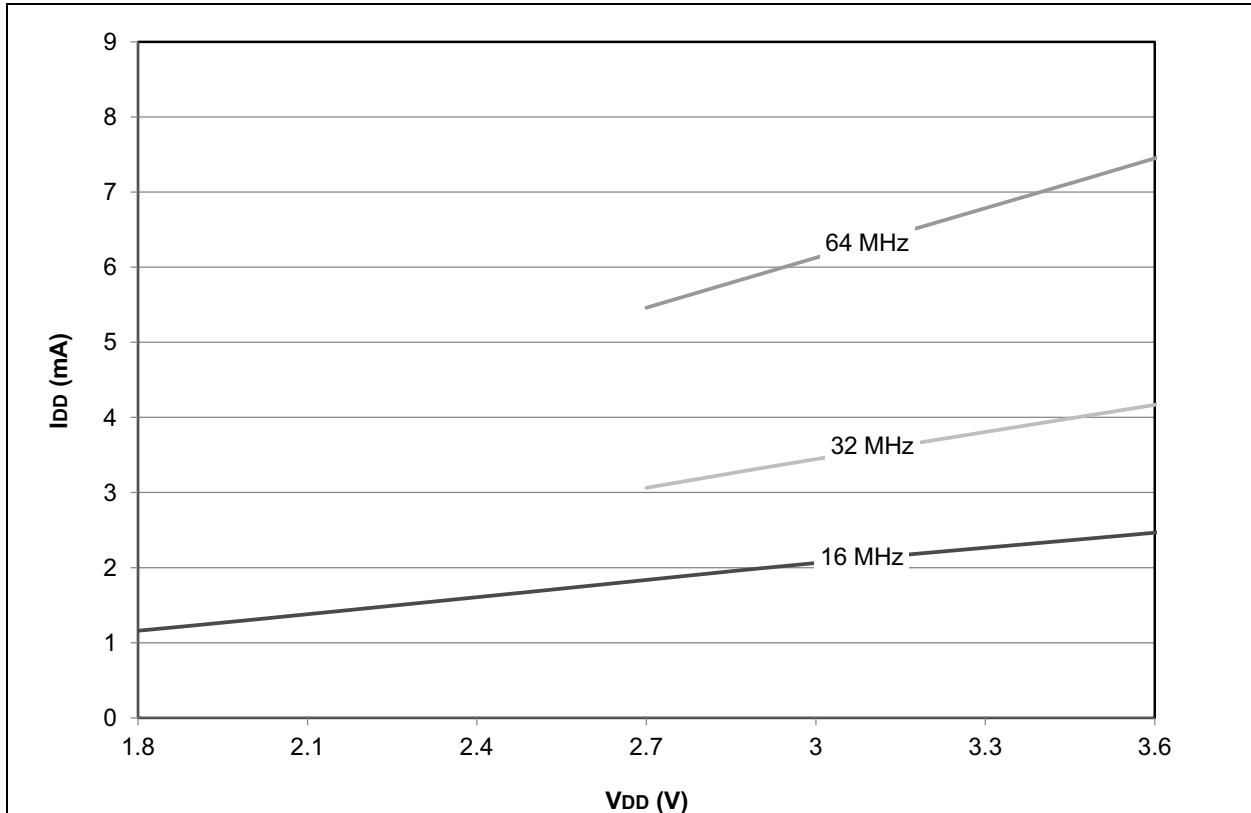
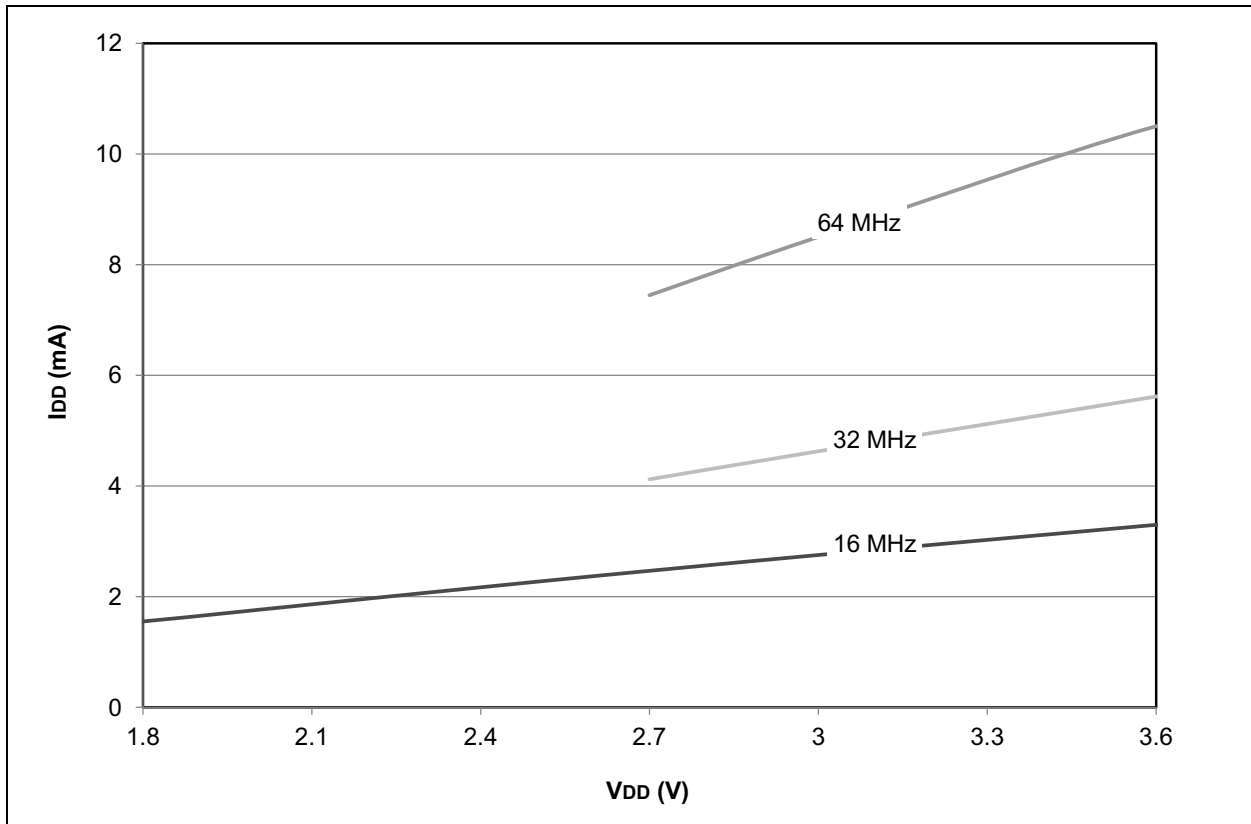


FIGURE 28-31: PIC18LF2X/4XK22 MAXIMUM I_{DD} : RC_RUN HF-INTOSC with PLL



PIC18(L)F2X/4XK22

FIGURE 28-42: PIC18F2X/4XK22 TYPICAL I_{DD} : RC_IDLE HF-INTOSC

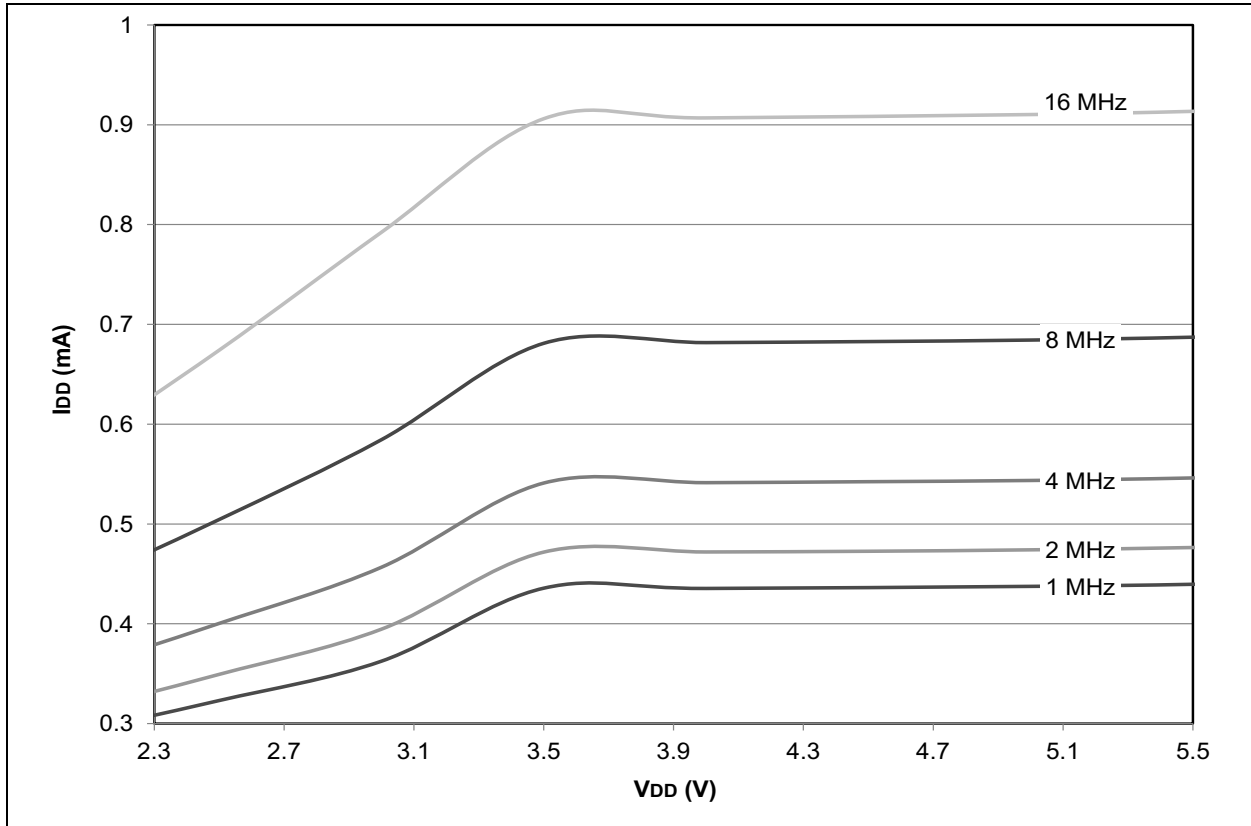
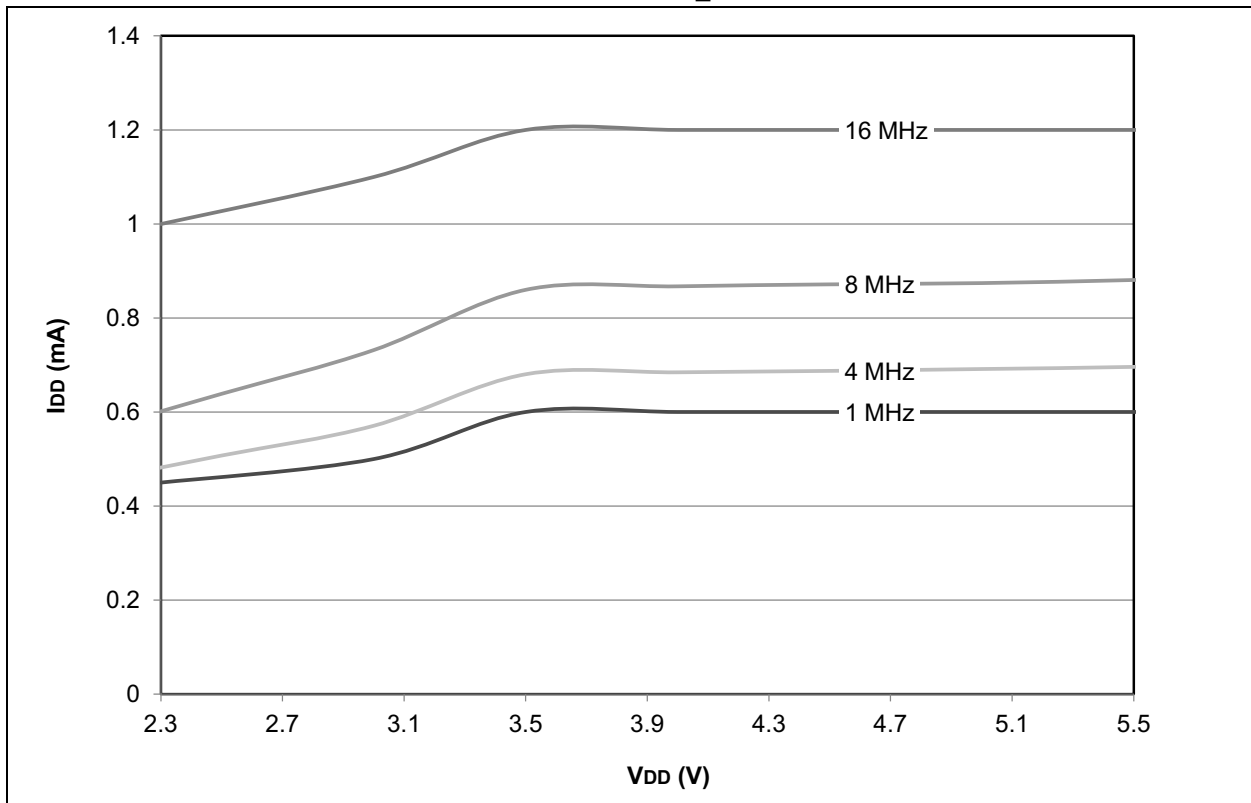


FIGURE 28-43: PIC18F2X/4XK22 MAXIMUM I_{DD} : RC_IDLE HF-INTOSC



PIC18(L)F2X/4XK22

FIGURE 28-72: PIC18LF2X/4XK22 TYPICAL I_{DD} : SEC_RUN 32.768 kHz

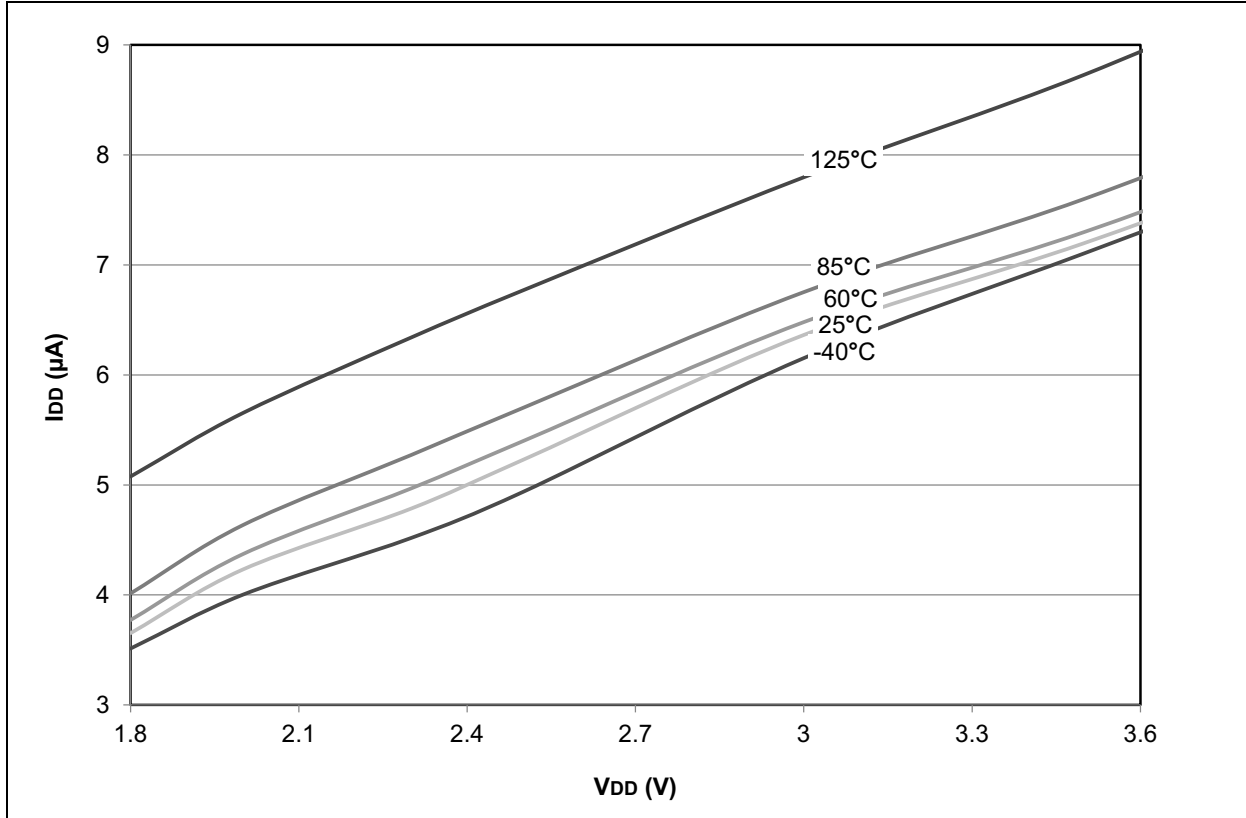


FIGURE 28-73: PIC18LF2X/4XK22 MAXIMUM I_{DD} : SEC_RUN 32.768 kHz

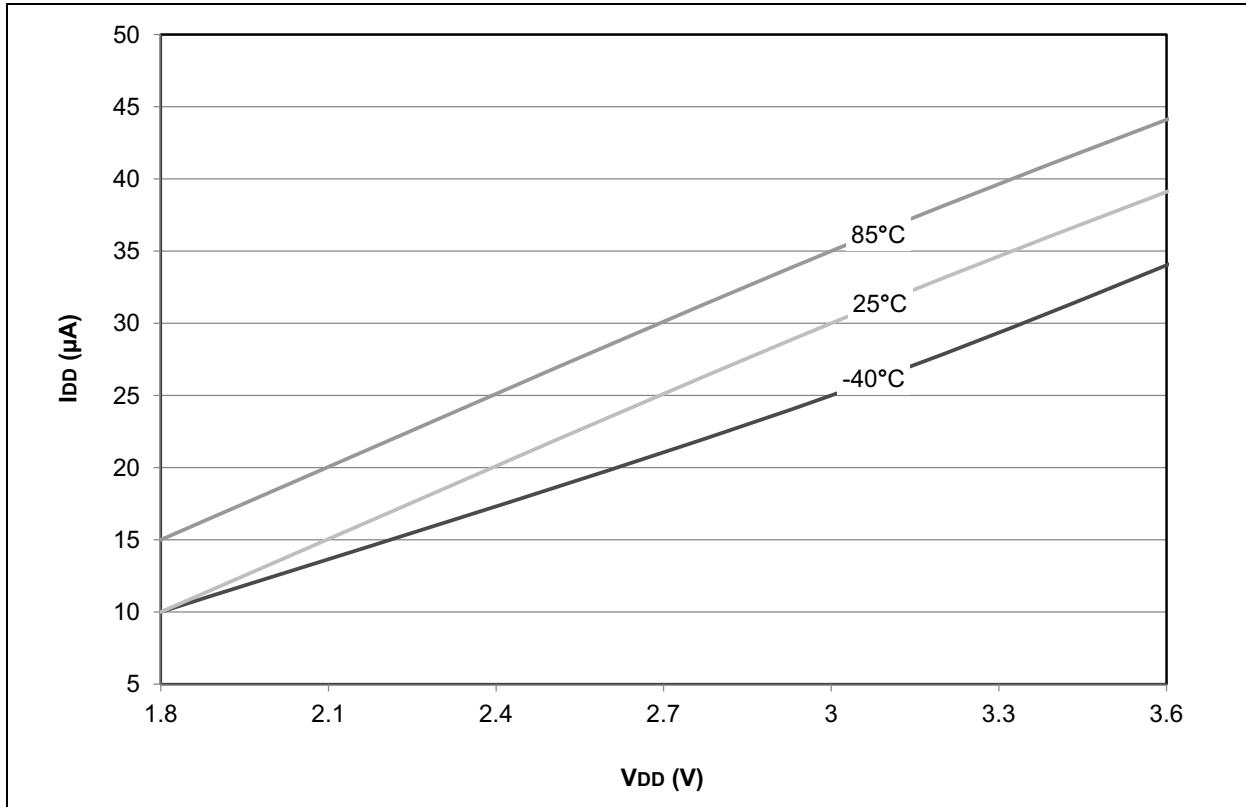


FIGURE 28-82: PIC18(L)F2X/4XK22 TTL BUFFER INPUT HIGH VOLTAGE

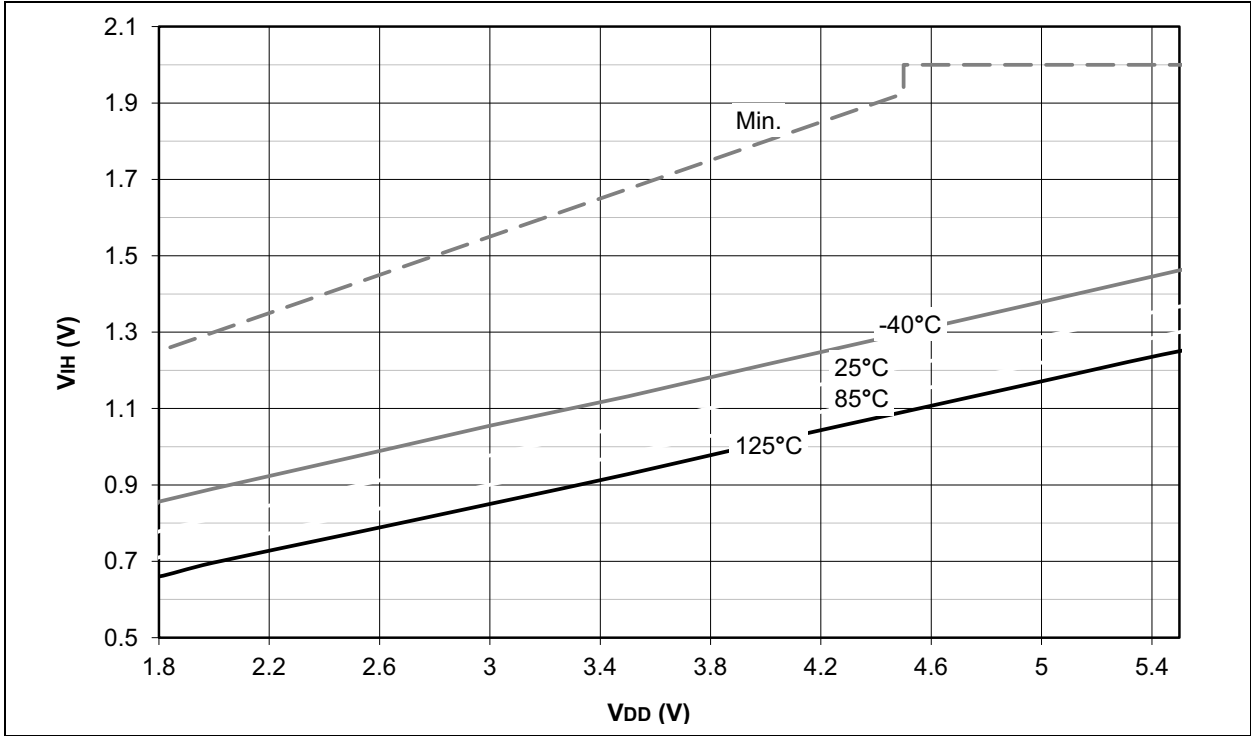


FIGURE 28-83: PIC18(L)F2X/4XK22 SCHMITT TRIGGER BUFFER INPUT HIGH VOLTAGE

