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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f25k22-i-ss

FIGURE 3: 40-PIN PDIP DIAGRAM

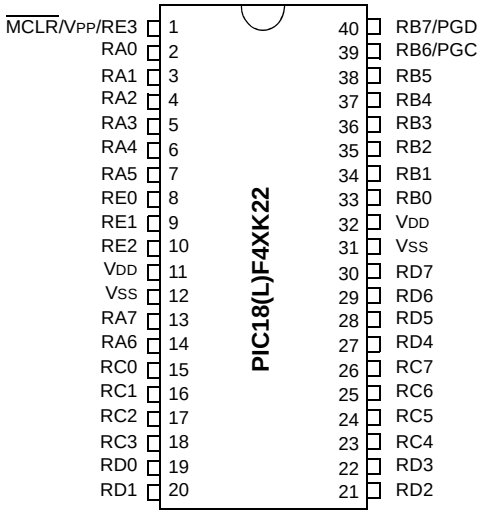


FIGURE 4: 40-PIN UQFN DIAGRAM

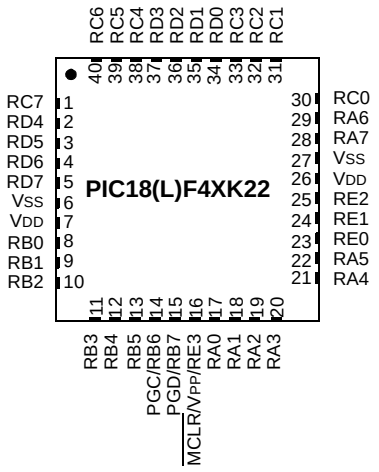


TABLE 3: PIC18(L)F4XK22 PIN SUMMARY (CONTINUED)

40-PDIP	40-UQFN	44-TQFP	44-QFN	I/O	Analog	Comparator	CTMU	SR Latch	Reference	(E)CCP	EUSART	MSSP	Timers	Interrupts	Pull-up	Basic
9	24	26	26	RE1	AN6					P3B						
10	25	27	27	RE2	AN7					CCP5						
1	16	18	18	RE3											Y	$\overline{MCLR}$ V_{PP}
11, 32	7, 26	7, 28	7,8 28, 29	V_{DD}												V_{DD}
12, 31	6, 27	6, 29	6, 30, 31	V_{SS}												V_{SS}
—	—	12, 13 33, 34	13	NC												

Note 1: CCP2 multiplexed in fuses.
2: T3CKI multiplexed in fuses.
3: CCP3/P3A multiplexed in fuses.
4: P2B multiplexed in fuses.

TABLE 1-3: PIC18(L)F4XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Number				Pin Name	Pin Type	Buffer Type	Description
PDIP	TQFP	QFN	UQFN				
7	24	24	22	RA5/C2OUT/SRNQ/$\overline{SS1}$/HLVDIN/AN4			
				RA5	I/O	TTL	Digital I/O.
				C2OUT	O	CMOS	Comparator C2 output.
				SRNQ	O	TTL	SR latch $\overline{Q}$ output.
				$\overline{SS1}$	I	TTL	SPI slave select input (MSSP1).
				HLVDIN	I	Analog	High/Low-Voltage Detect input.
				AN4	I	Analog	Analog input 4.
14	31	33	29	RA6/CLKO/OSC2			
				RA6	I/O	TTL	Digital I/O.
				CLKO	O	—	In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
				OSC2	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
13	30	32	28	RA7/CLKI/OSC1			
				RA7	I/O	TTL	Digital I/O.
				CLKI	I	CMOS	External clock source input. Always associated with pin function OSC1.
				OSC1	I	ST	Oscillator crystal input or external clock source input ST buffer when configured in RC mode; CMOS otherwise.
33	8	9	8	RB0/INT0/FLT0/SRI/AN12			
				RB0	I/O	TTL	Digital I/O.
				INT0	I	ST	External interrupt 0.
				FLT0	I	ST	PWM Fault input for ECCP Auto-Shutdown.
				SRI	I	ST	SR latch input.
				AN12	I	Analog	Analog input 12.
34	9	10	9	RB1/INT1/C12IN3-/AN10			
				RB1	I/O	TTL	Digital I/O.
				INT1	I	ST	External interrupt 1.
				C12IN3-	I	Analog	Comparators C1 and C2 inverting input.
				AN10	I	Analog	Analog input 10.
35	10	11	10	RB2/INT2/CTED1/AN8			
				RB2	I/O	TTL	Digital I/O.
				INT2	I	ST	External interrupt 2.
				CTED1	I	ST	CTMU Edge 1 input.
				AN8	I	Analog	Analog input 8.
36	11	12	11	RB3/CTED2/P2A/CCP2/C12IN2-/AN9			
				RB3	I/O	TTL	Digital I/O.
				CTED2	I	ST	CTMU Edge 2 input.
				P2A(2)	O	CMOS	Enhanced CCP2 PWM output.
				CCP2(2)	I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
				C12IN2-	I	Analog	Comparators C1 and C2 inverting input.
				AN9	I	Analog	Analog input 9.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power.

Note 1: Default pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

TABLE 2-3: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

OSC Mode	OSC1 Pin	OSC2 Pin
RC, INTOSC with CLKOUT	Floating, external resistor should pull high	At logic low (clock/4 output)
RC with IO	Floating, external resistor should pull high	Configured as PORTA, bit 6
INTOSC with IO	Configured as PORTA, bit 7	Configured as PORTA, bit 6
EC with IO	Floating, pulled by external clock	Configured as PORTA, bit 6
EC with CLKOUT	Floating, pulled by external clock	At logic low (clock/4 output)
LP, XT, HS	Feedback inverter disabled at quiescent voltage level	Feedback inverter disabled at quiescent voltage level

Note: See Table 4-2 in **Section 4.0 "Reset"** for time-outs due to Sleep and $\overline{\text{MCLR}}$ Reset.

2.11 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS<1:0>) bits of the OSCCON register.

PIC18(L)F2X/4XK22 devices contain circuitry to prevent clock "glitches" when switching between clock sources. A short pause in the device clock occurs during the clock switch. The length of this pause is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Clock transitions are discussed in greater detail in **Section 3.1.2 "Entering Power-Managed Modes"**.

2.11.1 SYSTEM CLOCK SELECT (SCS<1:0>) BITS

The System Clock Select (SCS<1:0>) bits of the OSCCON register select the system clock source that is used for the CPU and peripherals.

- When SCS<1:0> = 00, the system clock source is determined by configuration of the FOSC<3:0> bits in the CONFIG1H Configuration register.
- When SCS<1:0> = 10, the system clock source is chosen by the internal oscillator frequency selected by the INTSRC bit of the OSCTUNE register, the MFIOSEL bit of the OSCCON2 register and the IRCF<2:0> bits of the OSCCON register.
- When SCS<1:0> = 01, the system clock source is the 32.768 kHz secondary oscillator shared with Timer1, Timer3 and Timer5.

After a Reset, the SCS<1:0> bits of the OSCCON register are always cleared.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS<1:0> bits of the OSCCON register. The user can monitor the SOSCRUN, MFIOFS and LFIOFS bits of the OSCCON2 register, and the HFIOFS and OSTS bits of the OSCCON register to determine the current system clock source.

2.11.2 OSCILLATOR START-UP TIME-OUT STATUS (OSTS) BIT

The Oscillator Start-up Time-out Status (OSTS) bit of the OSCCON register indicates whether the system clock is running from the external clock source, as defined by the FOSC<3:0> bits in the CONFIG1H Configuration register, or from the internal clock source. In particular, when the primary oscillator is the source of the primary clock, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

8.0 8 x 8 HARDWARE MULTIPLIER

8.1 Introduction

All PIC18 devices include an 8 x 8 hardware multiplier as part of the ALU. The multiplier performs an unsigned operation and yields a 16-bit result that is stored in the product register pair, PRODH:PRODL. The multiplier's operation does not affect any flags in the STATUS register.

Making multiplication a hardware operation allows it to be completed in a single instruction cycle. This has the advantages of higher computational throughput and reduced code size for multiplication algorithms and allows the PIC18 devices to be used in many applications previously reserved for digital signal processors. A comparison of various hardware and software multiply operations, along with the savings in memory and execution time, is shown in Table 8-1.

8.2 Operation

Example 8-1 shows the instruction sequence for an 8 x 8 unsigned multiplication. Only one instruction is required when one of the arguments is already loaded in the WREG register.

Example 8-2 shows the sequence to do an 8 x 8 signed multiplication. To account for the sign bits of the arguments, each argument's Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 8-1: 8 x 8 UNSIGNED MULTIPLY ROUTINE

```
MOVF    ARG1, W     ;
MULWF   ARG2        ; ARG1 * ARG2 ->
                    ; PRODH:PRODL
```

EXAMPLE 8-2: 8 x 8 SIGNED MULTIPLY ROUTINE

```
MOVF    ARG1, W
MULWF   ARG2        ; ARG1 * ARG2 ->
                    ; PRODH:PRODL
BTFSC   ARG2, SB    ; Test Sign Bit
SUBWF   PRODH, F    ; PRODH = PRODH
                    ;         - ARG1
MOVF    ARG2, W
BTFSC   ARG1, SB    ; Test Sign Bit
SUBWF   PRODH, F    ; PRODH = PRODH
                    ;         - ARG2
```

TABLE 8-1: PERFORMANCE COMPARISON FOR VARIOUS MULTIPLY OPERATIONS

Routine	Multiply Method	Program Memory (Words)	Cycles (Max)	Time			
				@ 64 MHz	@ 40 MHz	@ 10 MHz	@ 4 MHz
8 x 8 unsigned	Without hardware multiply	13	69	4.3 μs	6.9 μs	27.6 μs	69 μs
	Hardware multiply	1	1	62.5 ns	100 ns	400 ns	1 μs
8 x 8 signed	Without hardware multiply	33	91	5.7 μs	9.1 μs	36.4 μs	91 μs
	Hardware multiply	6	6	375 ns	600 ns	2.4 μs	6 μs
16 x 16 unsigned	Without hardware multiply	21	242	15.1 μs	24.2 μs	96.8 μs	242 μs
	Hardware multiply	28	28	1.8 μs	2.8 μs	11.2 μs	28 μs
16 x 16 signed	Without hardware multiply	52	254	15.9 μs	25.4 μs	102.6 μs	254 μs
	Hardware multiply	35	40	2.5 μs	4.0 μs	16.0 μs	40 μs

13.6 Register Definitions: Timer2/4/6 Control

REGISTER 13-1: TxCON: TIMER2/TIMER4/TIMER6 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TxOUTPS<3:0>				TMRxON	TxCKPS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented:** Read as ‘0’

bit 6-3 **TxOUTPS<3:0>:** TimerX Output Postscaler Select bits

0000 = 1:1 Postscaler
0001 = 1:2 Postscaler
0010 = 1:3 Postscaler
0011 = 1:4 Postscaler
0100 = 1:5 Postscaler
0101 = 1:6 Postscaler
0110 = 1:7 Postscaler
0111 = 1:8 Postscaler
1000 = 1:9 Postscaler
1001 = 1:10 Postscaler
1010 = 1:11 Postscaler
1011 = 1:12 Postscaler
1100 = 1:13 Postscaler
1101 = 1:14 Postscaler
1110 = 1:15 Postscaler
1111 = 1:16 Postscaler

bit 2 **TMRxON:** TimerX On bit

1 = TimerX is on
0 = TimerX is off

bit 1-0 **TxCKPS<1:0>:** Timer2-type Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

16.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode would typically be used in RS-232 systems. The receiver block diagram is shown in Figure 16-2. The data is received on the RXx/DTx pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREGx register.

16.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTAx register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXSTAx register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTAx register enables the EUSART. The RXx/DTx I/O pin must be configured as an input by setting the corresponding TRIS control bit. If the RXx/DTx pin is shared with an analog peripheral the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

16.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See **Section 16.1.2.5 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RCxIF interrupt flag bit of the PIR1/PIR3 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREGx register.

Note:	If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. See **Section 16.1.2.6 "Receive Overrun Error"** for more information on overrun errors.

16.1.2.3 Receive Data Polarity

The polarity of the receive data can be controlled with the DTRXP bit of the BAUDCONx register. The default state of this bit is '0' which selects high true receive idle and data bits. Setting the DTRXP bit to '1' will invert the receive data resulting in low true idle and data bits. The DTRXP bit controls receive data polarity only in Asynchronous mode. In Synchronous mode the DTRXP bit has a different function.

18.4 Comparator Interrupt Operation

The comparator interrupt flag will be set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 18-2). The first latch is updated with the comparator output value, when the CMxCON0 register is read or written. The value is latched on the third cycle of the system clock, also known as Q3. This first latch retains the comparator value until another read or write of the CMxCON0 register occurs or a Reset takes place. The second latch is updated with the comparator output value on every first cycle of the system clock, also known as Q1. When the output value of the comparator changes, the second latch is updated and the output values of both latches no longer match one another, resulting in a mismatch condition. The latch outputs are fed directly into the inputs of an exclusive-or gate. This mismatch condition is detected by the exclusive-or gate and sent to the interrupt circuitry. The mismatch condition will persist until the first latch value is updated by performing a read of the CMxCON0 register or the comparator output returns to the previous state.

Note 1: A write operation to the CMxCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

2: Comparator interrupts will operate correctly regardless of the state of CxOE.

When the mismatch condition occurs, the comparator interrupt flag is set. The interrupt flag is triggered by the edge of the changing value coming from the exclusive-or gate. This means that the interrupt flag can be reset once it is triggered without the additional step of reading or writing the CMxCON0 register to clear the mismatch latches. When the mismatch registers are cleared, an interrupt will occur upon the comparator's return to the previous state, otherwise no interrupt will be generated.

Software will need to maintain information about the status of the comparator output, as read from the CMxCON0 register, or CM2CON1 register, to determine the actual change that has occurred. See Figures 18-3 and 18-4.

The CxIF bit of the PIR2 register is the comparator interrupt flag. This bit must be reset by software by clearing it to '0'. Since it is also possible to write a '1' to this register, an interrupt can be generated.

In mid-range Compatibility mode the CxIE bit of the PIE2 register and the PEIE/GIEL and GIE/GIEH bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR2 register will still be set if an interrupt condition occurs.

18.4.1 PRESETTING THE MISMATCH LATCHES

The comparator mismatch latches can be preset to the desired state before the comparators are enabled. When the comparator is off the CxPOL bit controls the CxOUT level. Set the CxPOL bit to the desired CxOUT non-interrupt level while the CxON bit is cleared. Then, configure the desired CxPOL level in the same instruction that the CxON bit is set. Since all register writes are performed as a read-modify-write, the mismatch latches will be cleared during the instruction read phase and the actual configuration of the CxON and CxPOL bits will be occur in the final write phase.

FIGURE 18-3: COMPARATOR INTERRUPT TIMING W/O CMxCON0 READ

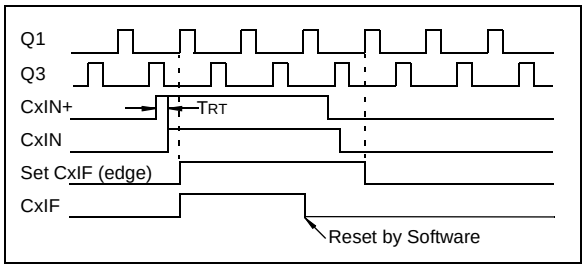
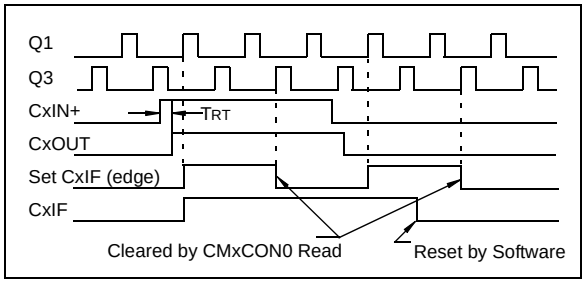


FIGURE 18-4: COMPARATOR INTERRUPT TIMING WITH CMxCON0 READ



Note 1: If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF interrupt flag of the PIR2 register may not get set.

2: When either comparator is first enabled, bias circuitry in the comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

22.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DACOUT pin

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the VREFCON1 register.

22.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DACR<4:0> bits of the VREFCON2 register.

The DAC output voltage is determined by the following equations:

EQUATION 22-1: DAC OUTPUT VOLTAGE

$$V_{OUT} = \left((V_{SRC+} - V_{SRC-}) \times \frac{DACR<4:0>}{2^5} \right) + V_{SRC-}$$

$$V_{SRC+} = V_{DD}, V_{REF+} \text{ or } FVR1$$

$$V_{SRC-} = V_{SS} \text{ or } V_{REF-}$$

22.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in **Section 27.0 "Electrical Specifications"**.

22.3 Low-Power Voltage State

In order for the DAC module to consume the least amount of power, one of the two voltage reference input sources to the resistor ladder must be disconnected. Either the positive voltage source, (VSRC+), or the negative voltage source, (VSRC-) can be disabled.

The negative voltage source is disabled by setting the DACLPS bit in the VREFCON1 register. Clearing the DACLPS bit in the VREFCON1 register disables the positive voltage source.

22.4 Output Clamped to Positive Voltage Source

The DAC output voltage can be set to VSRC+ with the least amount of power consumption by performing the following:

- Clearing the DACEN bit in the VREFCON1 register.
- Setting the DACLPS bit in the VREFCON1 register.
- Configuring the DACPSS bits to the proper positive source.
- Configuring the DACRx bits to '11111' in the VREFCON2 register.

This is also the method used to output the voltage level from the FVR to an output pin. See **Section 22.6 "DAC Voltage Reference Output"** for more information.

22.5 Output Clamped to Negative Voltage Source

The DAC output voltage can be set to VSRC- with the least amount of power consumption by performing the following:

- Clearing the DACEN bit in the VREFCON1 register.
- Clearing the DACLPS bit in the VREFCON1 register.
- Configuring the DACPSS bits to the proper negative source.
- Configuring the DACRx bits to '00000' in the VREFCON2 register.

This allows the comparator to detect a zero-crossing while not consuming additional current through the DAC module.

22.6 DAC Voltage Reference Output

The DAC can be output to the DACOUT pin by setting the DACOE bit of the VREFCON1 register to '1'. Selecting the DAC reference voltage for output on the DACOUT pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACOUT pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to DACOUT. Figure 22-2 shows an example buffering technique.

TABLE 24-1: CONFIGURATION BITS AND DEVICE IDs

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	—	—	—	—	—	—	—	—	0000 0000
300001h	CONFIG1H	IESO	FCMEN	PRICLKEN	PLLCFG	FOSC<3:0>				0010 0101
300002h	CONFIG2L	—	—	—	BORV<1:0>		BOREN<1:0>		$\overline{\text{PWRTEN}}$	0001 1111
300003h	CONFIG2H	—	—	WDPS<3:0>				WDTEN<1:0>		0011 1111
300004h	CONFIG3L	—	—	—	—	—	—	—	—	0000 0000
300005h	CONFIG3H	MCLRE	—	P2BMX	T3CMX	HFOFST	CCP3MX	PBADEN	CCP2MX	1011 1111
300006h	CONFIG4L	$\overline{\text{DEBUG}}$	XINST	—	—	—	LVP(1)	—	STRVEN	1000 0101
300007h	CONFIG4H	—	—	—	—	—	—	—	—	1111 1111
300008h	CONFIG5L	—	—	—	—	CP3(2)	CP2(2)	CP1	CP0	0000 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	1100 0000
30000Ah	CONFIG6L	—	—	—	—	WRT3(2)	WRT2(2)	WRT1	WRT0	0000 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC(3)	—	—	—	—	—	1110 0000
30000Ch	CONFIG7L	—	—	—	—	EBTR3(2)	EBTR2(2)	EBTR1	EBTR0	0000 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	0100 0000
3FFFFEh	DEVID1(4)	DEV<2:0>			REV<4:0>					qqqq qqqq
3FFFFFh	DEVID2(4)	DEV<10:3>								0101 qqqq

Legend: – = unimplemented, q = value depends on condition. Shaded bits are unimplemented, read as '0'.

Note 1: Can only be changed when in high voltage programming mode.

2: Available on PIC18(L)FX5K22 and PIC18(L)FX6K22 devices only.

3: In user mode, this bit is read-only and cannot be self-programmed.

4: See Register 24-12 and Register 24-13 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

TABLE 25-1: OPCODE FIELD DESCRIPTIONS

Field	Description
a	RAM access bit a = 0: RAM location in Access RAM (BSR register is ignored) a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7).
BSR	Bank Select Register. Used to select the current RAM bank.
C, DC, Z, OV, N	ALU Status bits: **C**arry, **D**igit **C**arry, **Z**ero, **Ov**erflow, **N**egative.
d	Destination select bit d = 0: store result in WREG d = 1: store result in file register f
dest	Destination: either the WREG register or the specified register file location.
f	8-bit Register file address (00h to FFh) or 2-bit FSR designator (0h to 3h).
f_s	12-bit Register file address (000h to FFFh). This is the source address.
f_d	12-bit Register file address (000h to FFFh). This is the destination address.
GIE	Global Interrupt Enable bit.
k	Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value).
label	Label name.
mm * *+ *- +*	The mode of the TBLPTR register for the table read and table write instructions. Only used with table read and table write instructions: No change to register (such as TBLPTR with table reads and writes) Post-Increment register (such as TBLPTR with table reads and writes) Post-Decrement register (such as TBLPTR with table reads and writes) Pre-Increment register (such as TBLPTR with table reads and writes)
n	The relative address (2's complement number) for relative branch instructions or the direct address for CALL/BRANCH and RETURN instructions.
PC	Program Counter.
PCL	Program Counter Low Byte.
PCH	Program Counter High Byte.
PCLATH	Program Counter High Byte Latch.
PCLATU	Program Counter Upper Byte Latch.
$\overline{PD}$	Power-down bit.
PRODH	Product of Multiply High Byte.
PRODL	Product of Multiply Low Byte.
s	Fast Call/Return mode select bit s = 0: do not update into/from shadow registers s = 1: certain registers loaded into/from shadow registers (Fast mode)
TBLPTR	21-bit Table Pointer (points to a Program Memory location).
TABLAT	8-bit Table Latch.
$\overline{TO}$	Time-out bit.
TOS	Top-of-Stack.
u	Unused or unchanged.
WDT	Watchdog Timer.
WREG	Working register (accumulator).
x	Don't care ('0' or '1'). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
z_s	7-bit offset value for indirect addressing of register files (source).
z_d	7-bit offset value for indirect addressing of register files (destination).
{ }	Optional argument.
[text]	Indicates an indexed address.
(text)	The contents of text.
[expr]<n>	Specifies bit n of the register indicated by the pointer expr.
→	Assigned to.
< >	Register bit field.
∈	In the set of.
italics	User defined term (font is Courier).

BNOV **Branch if Not Overflow**

Syntax: BNOV n

Operands: -128 ≤ n ≤ 127

Operation: if OVERFLOW bit is '0'
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0101	nnnn	nnnn

Description: If the OVERFLOW bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNOV Jump

Before Instruction
PC = address (HERE)
After Instruction
If OVERFLOW = 0;
PC = address (Jump)
If OVERFLOW = 1;
PC = address (HERE + 2)

BNZ **Branch if Not Zero**

Syntax: BNZ n

Operands: -128 ≤ n ≤ 127

Operation: if ZERO bit is '0'
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0001	nnnn	nnnn

Description: If the ZERO bit is '0', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNZ Jump

Before Instruction
PC = address (HERE)
After Instruction
If ZERO = 0;
PC = address (Jump)
If ZERO = 1;
PC = address (HERE + 2)

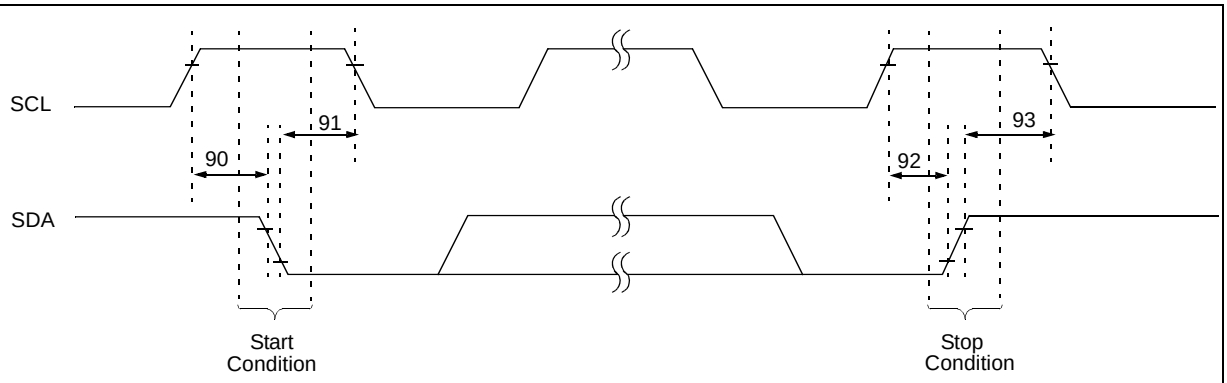
27.3 DC Characteristics: RC Run Supply Current, PIC18(L)F2X/4XK22

PIC18LF2X/4XK22		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
PIC18F2X/4XK22		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	**Device Characteristics**	**Typ**	**Max**	**Units**	**Conditions**		
D020	Supply Current (IDD)(1),(2)	3.6	23	µA	-40°C	VDD = 1.8V	FOSC = 31 kHz (**RC_RUN** mode, LFINTOSC source)
		3.9	25	µA	+25°C		
		3.9	—	µA	+60°C		
		3.9	28	µA	+85°C		
		4.0	30	µA	125°C		
D021		8.1	26	µA	-40°C	VDD = 3.0V	
		8.4	30	µA	+25°C		
		8.6	—	µA	+60°C		
		8.7	35	µA	+85°C		
		10.7	40	µA	+125°C		
D022		16	35	µA	-40°C	VDD = 2.3V	FOSC = 31 kHz (**RC_RUN** mode, LFINTOSC source)
		17	35	µA	+25°C		
		18	35	µA	+85°C		
		19	50	µA	+125°C		
D023		18	50	µA	-40°C	VDD = 3.0V	
		20	50	µA	+25°C		
		21	50	µA	+85°C		
		22	60	µA	+125°C		
D024		19	55	µA	-40°C	VDD = 5.0V	
		21	55	µA	+25°C		
		22	55	µA	+85°C		
		23	70	µA	+125°C		
D025		0.14	0.25	mA	-40°C to +125°C	VDD = 1.8V	FOSC = 500 kHz (**RC_RUN** mode, MFINTOSC source)
D026		0.17	0.30	mA	-40°C to +125°C	VDD = 3.0V	
D027		0.18	0.25	mA	-40°C to +125°C	VDD = 2.3V	FOSC = 500 kHz (**RC_RUN** mode, MFINTOSC source)
D028		0.20	0.30	mA	-40°C to +125°C	VDD = 3.0V	
D029		0.25	0.35	mA	-40°C to +125°C	VDD = 5.0V	

Note 1: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
Test condition: All Peripheral Module Control bits in PMD0, PMD1 and PMD2 set to '1'.

2: The test conditions for all IDD measurements in active operation mode are:
All I/O pins set as outputs driven to Vss;
$\overline{MCLR}$ = VDD;
OSC1 = external square wave, from rail-to-rail (PRI_RUN and PRI_IDLE only).

FIGURE 27-19: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS



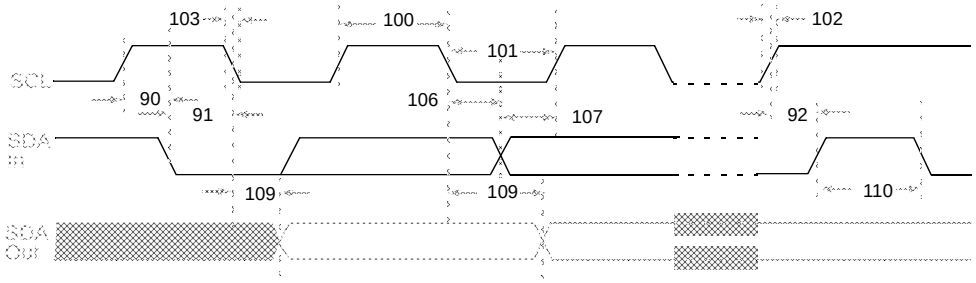
Note: Refer to Figure 27-6 for load conditions.

TABLE 27-17: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ns	
			400 kHz mode	2(TOSC)(BRG + 1)	—		
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—		

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

FIGURE 27-20: MASTER SSP I²C BUS DATA TIMING



Note: Refer to Figure 27-6 for load conditions.

TABLE 27-18: MASTER SSP I^2C BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock High Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			400 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	ms	
101	TLOW	Clock Low Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			400 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	ms	
102	TR	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
103	TF	SDA and SCL Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
90	TSU:STA	Start Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ms	Only relevant for Repeated Start condition
			400 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	ms	
91	THD:STA	Start Condition Hold Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ms	After this period, the first clock pulse is generated
			400 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	ms	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	ms	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			400 kHz mode	2(TOSC)(BRG + 1)	—	ms	
			1 MHz mode(1)	2(TOSC)(BRG + 1)	—	ms	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(1)	—	—	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	ms	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	ms	
D102	CB	Bus Capacitive Loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I^2C pins.

2: A fast mode I^2C bus device can be used in a standard mode I^2C bus system, but parameter 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line, parameter 102 + parameter 107 = 1000 + 250 = 1250 ns (for 100 kHz mode), before the SCL line is released.

FIGURE 28-20: PIC18LF2X/4XK22 TYPICAL IDD: RC_RUN LF-INTOSC 31 kHz

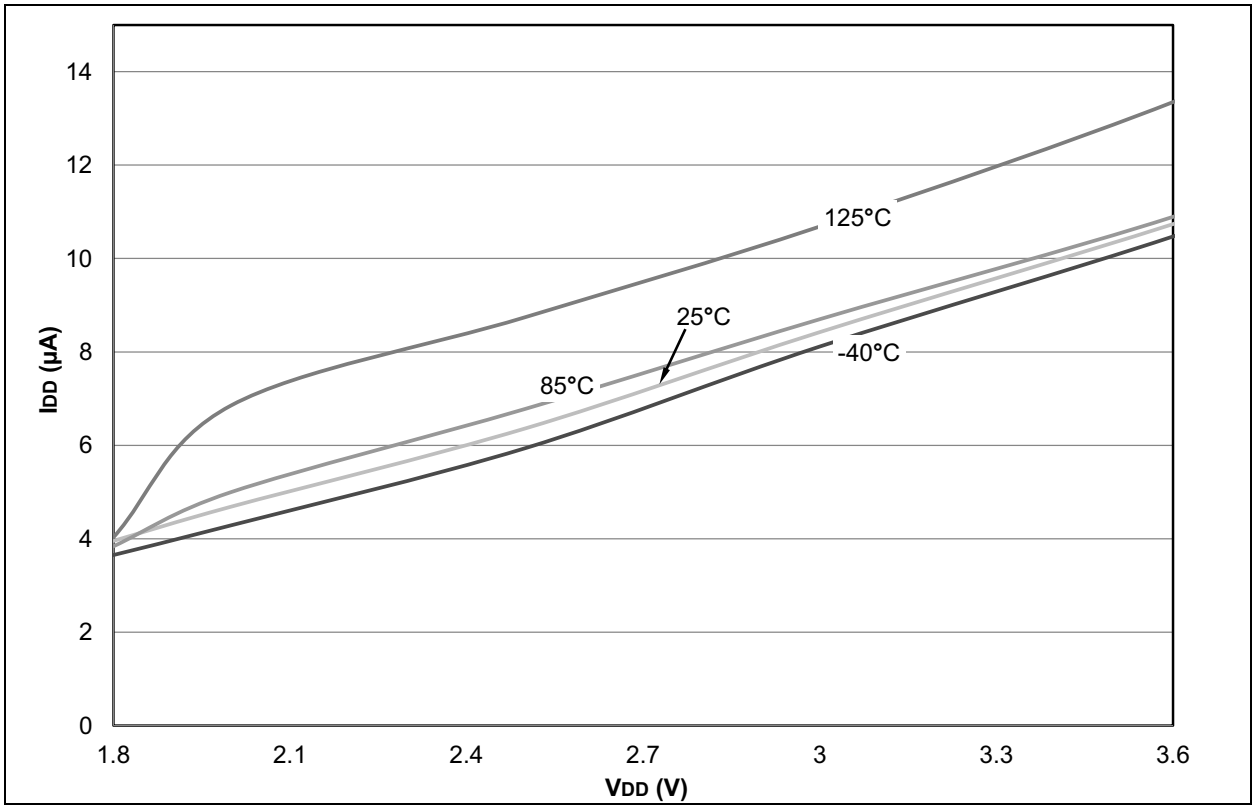


FIGURE 28-21: PIC18LF2X/4XK22 MAXIMUM IDD: RC_RUN LF-INTOSC 31 kHz

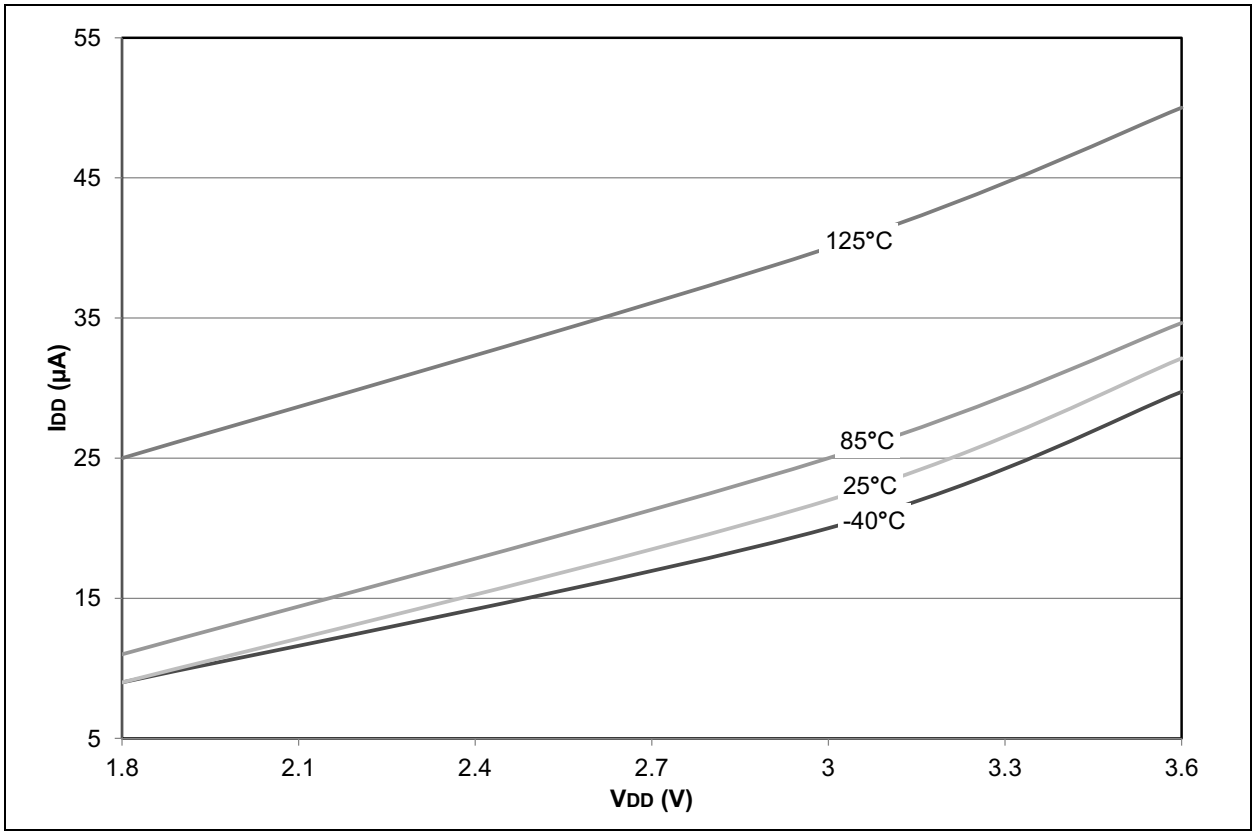


FIGURE 28-34: PIC18LF2X/4XK22 TYPICAL IDD: RC_IDLE LF-INTOSC 31 kHz

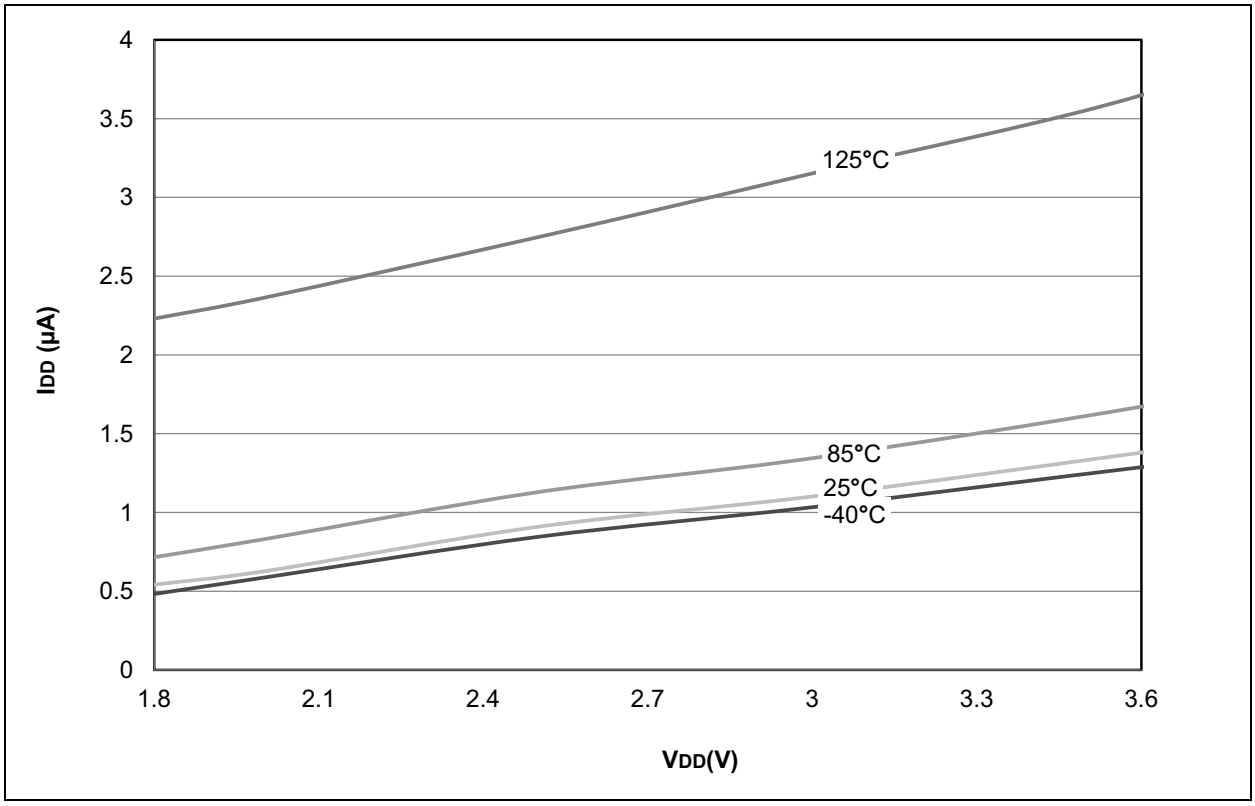


FIGURE 28-35: PIC18LF2X/4XK22 MAXIMUM IDD: RC_IDLE LF-INTOSC 31 kHz

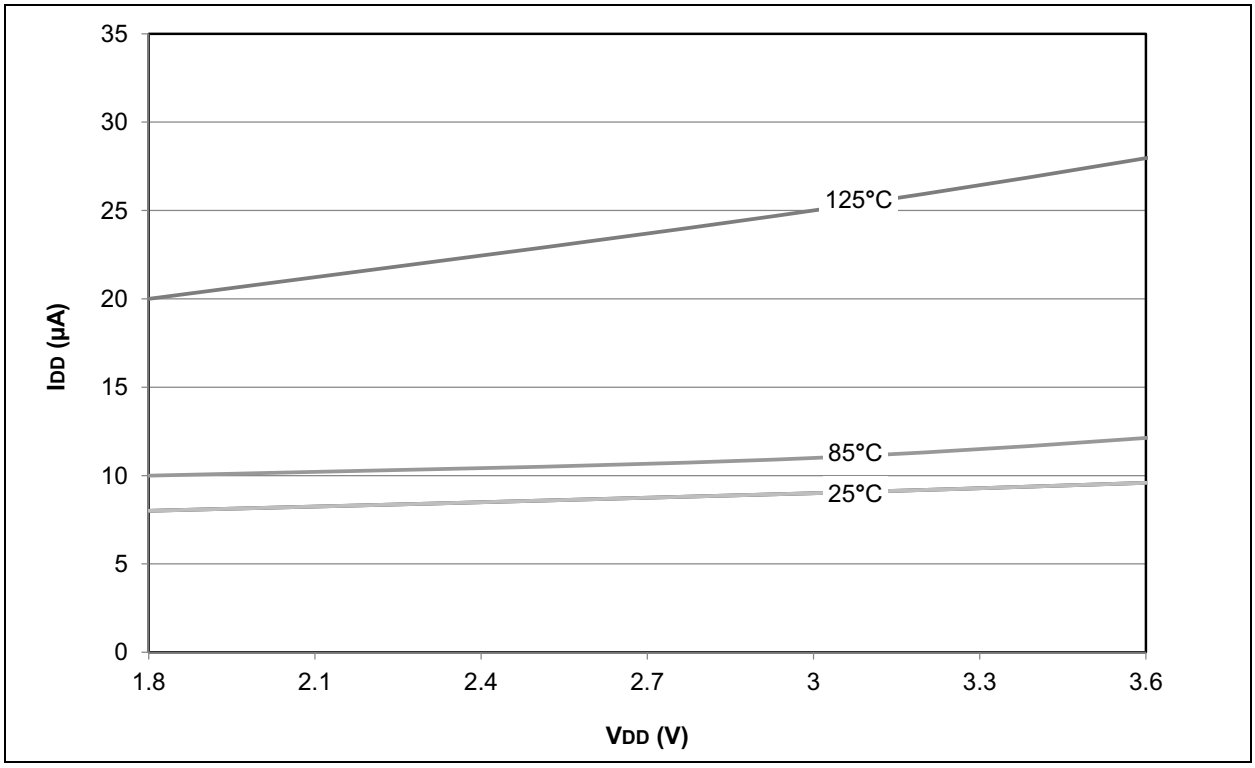


FIGURE 28-40: PIC18LF2X/4XK22 TYPICAL IDD: RC_IDLE HF-INTOSC

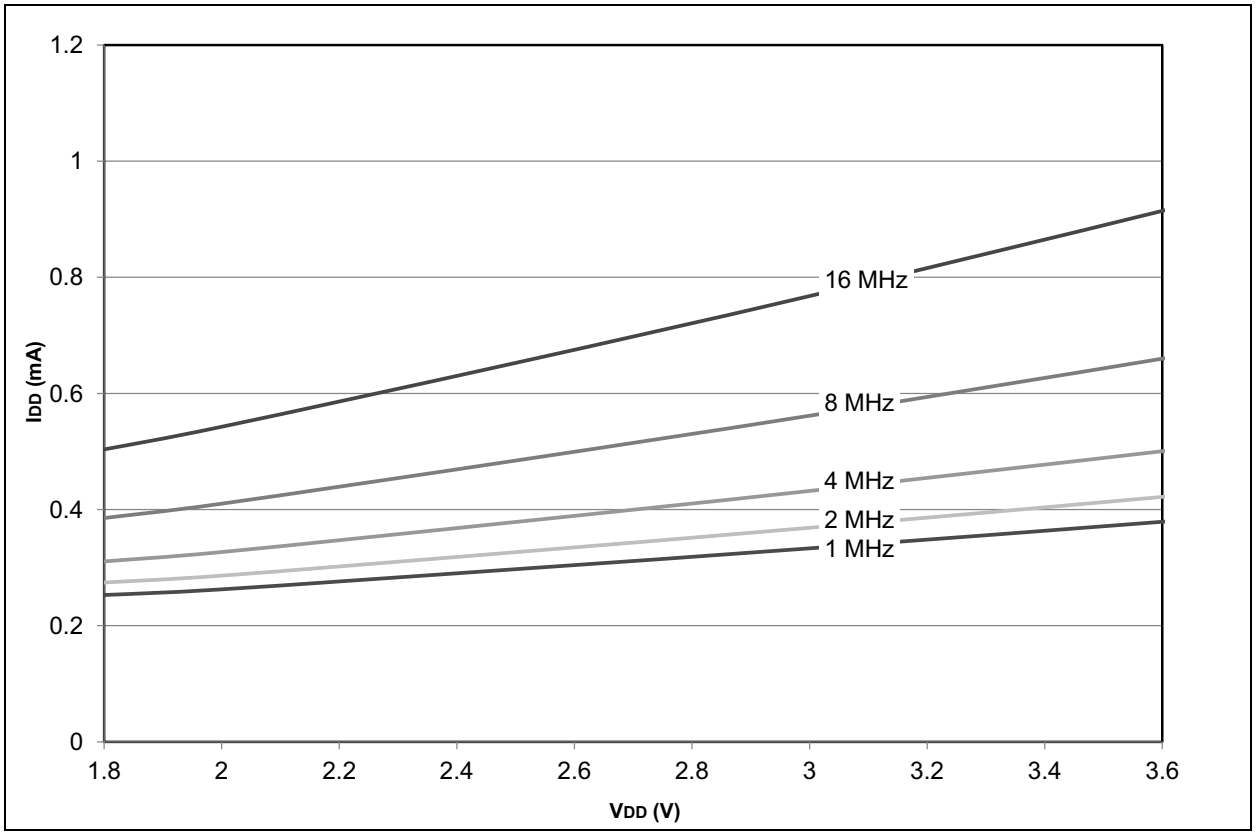


FIGURE 28-41: PIC18LF2X/4XK22 MAXIMUM IDD: RC_IDLE HF-INTOSC

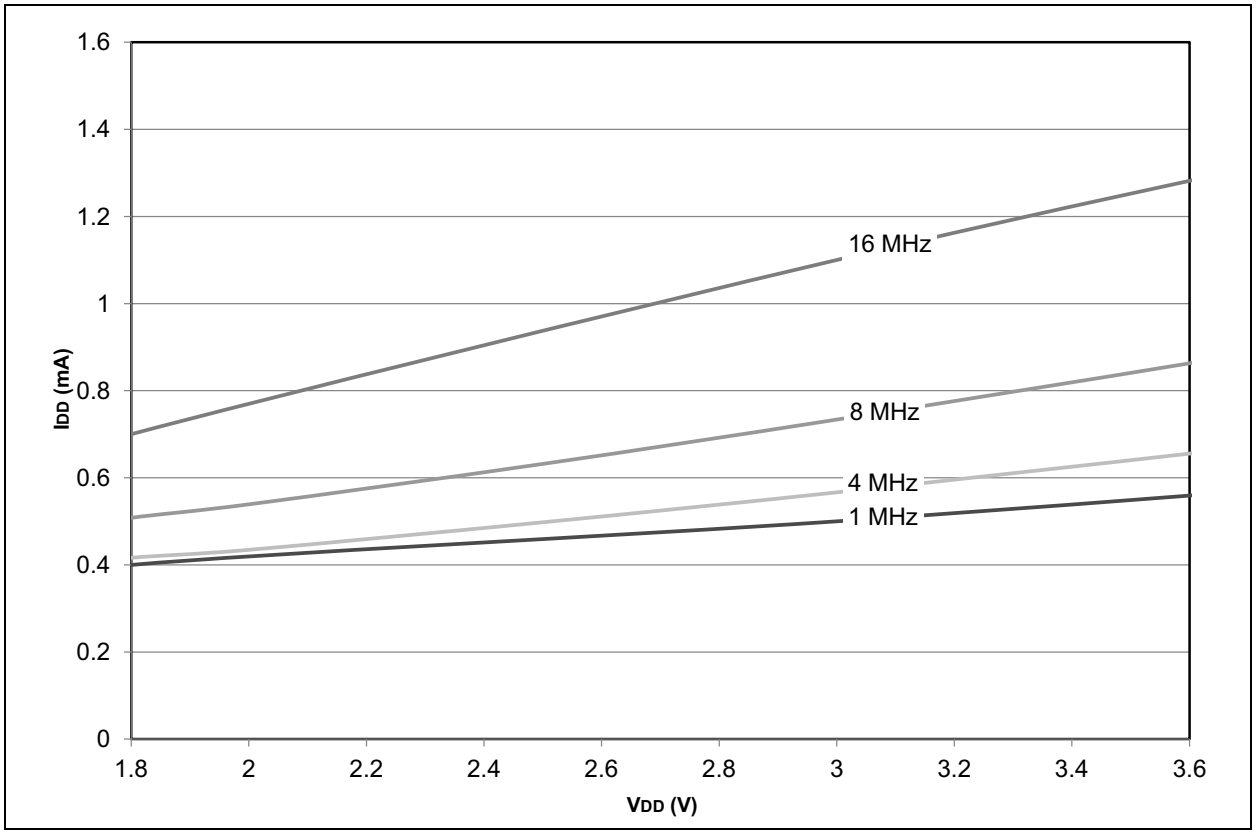


FIGURE 28-68: PIC18LF2X/4XK22 TYPICAL IDD: PRI_IDLE EC with PLL

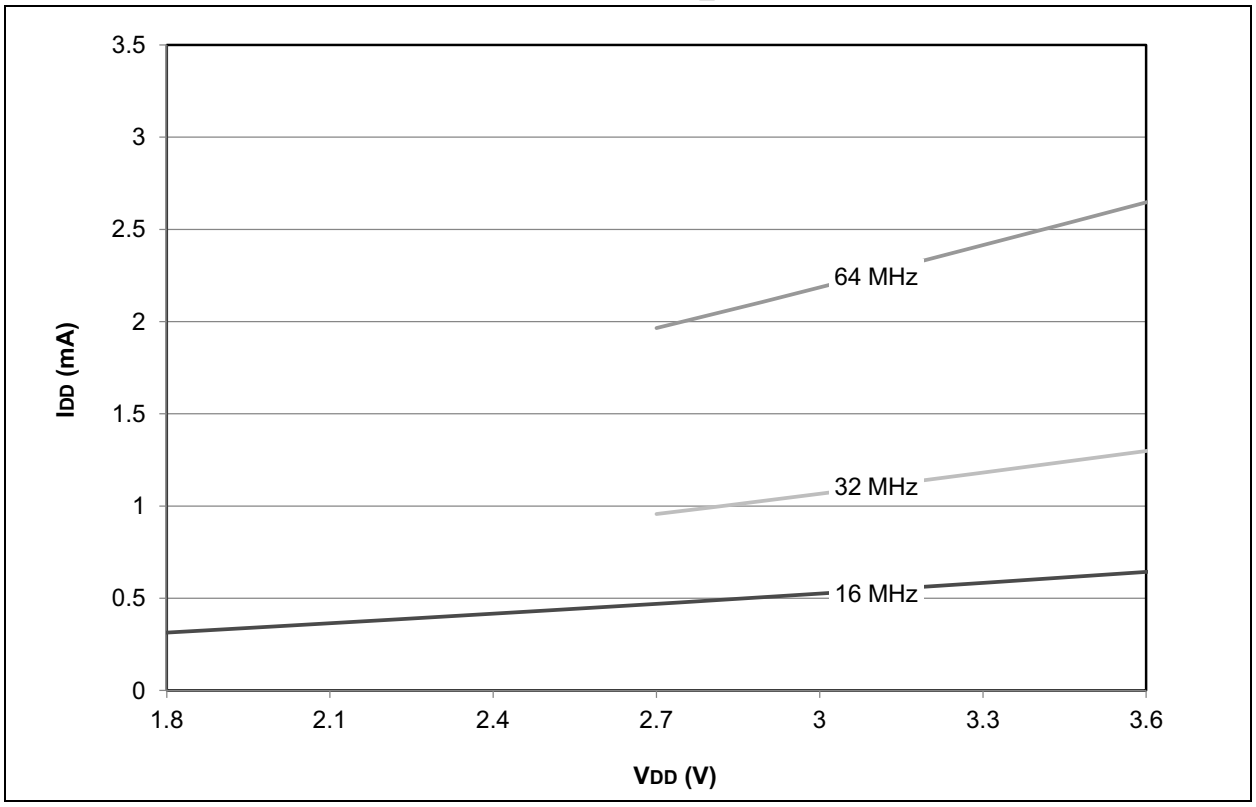


FIGURE 28-69: PIC18LF2X/4XK22 MAXIMUM IDD: PRI_IDLE EC with PLL

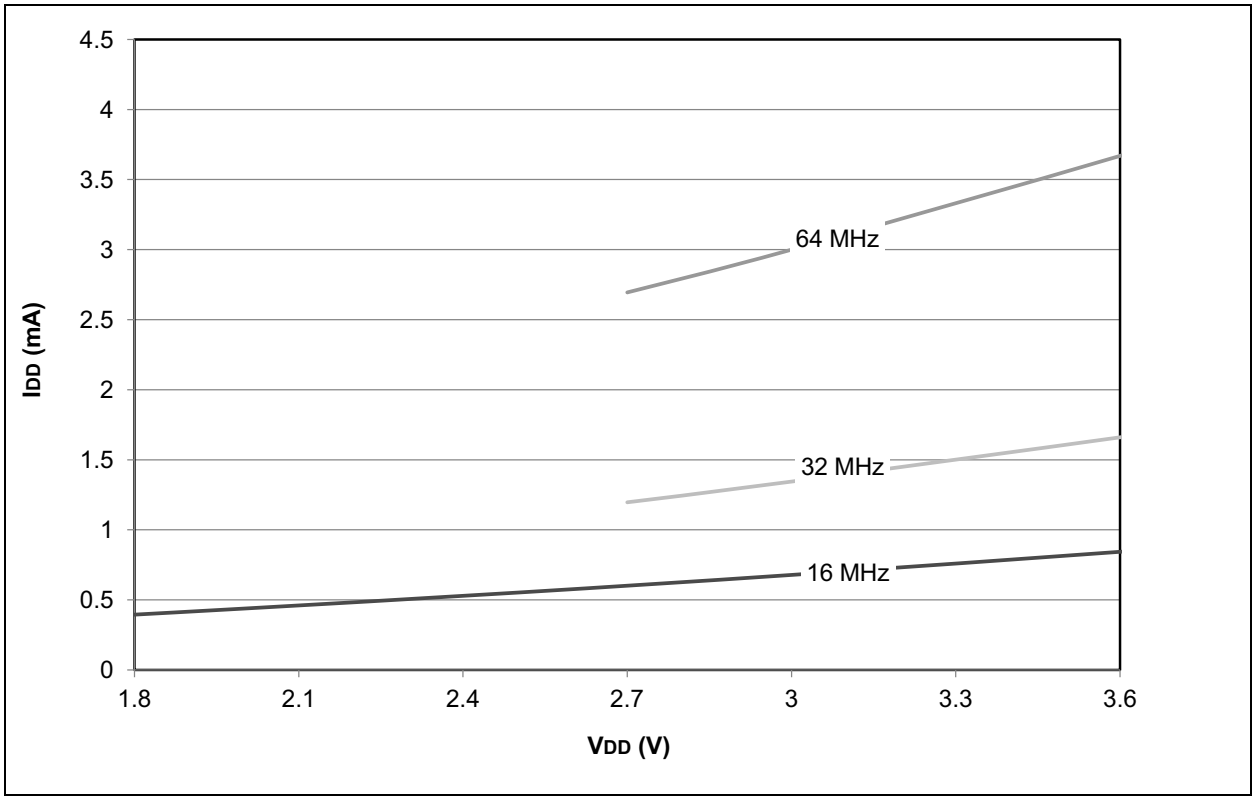


FIGURE 28-89: PIC18LF2X/4XK22 COMPARATOR OFFSET VOLTAGE, NORMAL-POWER MODE; VDD=1.8V