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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f26k22-i-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

	Pin M	lumber		Din Nome	Pin	Buffer	Description
PDIP	TQFP	QFN	UQFN	Pin Name	Туре	Туре	Description
10	27	27	25	RE2/CCP5/AN7			
				RE2	I/O	ST	Digital I/O.
				CCP5	I/O	ST	Capture 5 input/Compare 5 output/PWM 5 output
				AN7	Ι	Analog	Analog input 7.
1	18	18	16	RE3/VPP/MCLR			
				RE3	Ι	ST	Digital input.
				Vpp	Р		Programming voltage input.
				MCLR	I	ST	Active-low Master Clear (device Reset) input.
11,32	7, 28	7, 8, 28, 29	7, 26	Vdd	Р	—	Positive supply for logic and I/O pins.
12,31	6, 29	6,30, 31	6, 27	Vss	Р	_	Ground reference for logic and I/O pins.
	12,13, 33,34	13		NC			

TABLE 1-3: PIC18(L)F4XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power.

Note 1: Default pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

2.5.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 2-6). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode offers a Medium Power (MP) and a High Power (HP) option selectable by the FOSC<3:0> bits. The MP selections are best suited for oscillator frequencies between 4 MHz and 16 MHz. The HP selection has the highest gain setting of the internal inverter-amplifier and is best suited for frequencies above 16 MHz. HS mode is best suited for resonators that require a high drive setting.

FIGURE 2-6: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

- **2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.
- **3:** For oscillator design assistance, refer to the following Microchip Application Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC[®] and PIC[®] Devices" (DS00826)
 - AN849, "Basic PIC[®] Oscillator Design" (DS00849)
 - AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)



CERAMIC RESONATOR OPERATION (XT OR HS MODE)



3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

4.2 Register Definitions: Reset Control

REGISTER 4-1: RCON: RESET CONTROL REGISTER

R/W-0/	0 R/W-q/u	U-0	R/W-1/a	R-1/q	R-1/q	R/W-q/u	R/W-0/a	
IPEN	SBOREN ⁽¹⁾	_	RI	то	PD	POR ⁽²⁾	BOR	
bit 7	I				L		bit 0	
							,	
Legend:								
R = Reada	able bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'		
'1' = Bit is	set	'0' = Bit is cle	ared	-n/n = Value	at POR and BO	R/Value at all c	ther Resets	
x = Bit is	unknown	u = unchang	ed	q = depends	on condition			
bit 7	IPEN: Interrup 1 = Enable pr 0 = Disable pr	ot Priority Enat iority levels on riority levels on	ble bit interrupts i interrupts (P	IC16CXXX Co	mpatibility mode	•)		
bit 6	0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode) Dit 6 SBOREN: BOR Software Enable bit ⁽¹⁾ <u>If BOREN<1:0> = 01:</u> 1 = BOR is enabled 0 = BOR is disabled <u>If BOREN<1:0> = 00, 10 or 11:</u> Bit is disabled and read as 10'							
bit 5	Unimplemen	ted: Read as '	0'					
bit 4	RI: RESET INS	struction Flag b	oit					
	1 = The RESE 0 = The RESE code-exe	ET instruction v ET instruction cuted Reset of	vas not execu was executec ccurs)	ited (set by firm d causing a de	ware or Power- vice Reset (mu	on Reset) st be set in fin	mware after a	
bit 3	TO: Watchdog	g Time-out Flag	g bit					
	1 = Set by po 0 = A WDT ti	wer-up, CLRW	DT instruction ed	or SLEEP instr	uction			
bit 2	PD: Power-do	own Detection	Flag bit					
	1 = Set by po	ower-up or by t	he CLRWDT in	struction				
L :L 4	0 = Set by ex	ecution of the	SLEEP INStruc	Ction				
DIT		on Reset Statu	S DIT-					
	1 = NO POWER0 = A Power-0	on Reset occu	rred (must be	set in software	after a Power-o	on Reset occur	s)	
bit 0	BOR: Brown-	out Reset State	us bit ⁽³⁾				- /	
	1 = A Brown- 0 = A Brown-	out Reset has out Reset occi	not occurred urred (must be	(set by firmwai e set by firmwa	e only) re after a POR o	or Brown-out R	eset occurs)	
Note 1:	When CONFIG2L[2:1] = 01, then	the SBOREN	Reset state is	; '1'; otherwise.	it is '0'.		
2:	The actual Reset v	alue of POR is	determined b	by the type of c	levice Reset. Se	e the notes fol	lowing this	

register and Section 4.7 "Reset State of Registers" for additional information.

3: See Table 4-1.

Note 1: Brown-out Reset is indicated when BOR is '0' and POR is '1' (assuming that both POR and BOR were set to '1' by firmware immediately after POR).

2: It is recommended that the POR bit be set after a Power-on Reset has been detected so that subsequent Power-on Resets may be detected.

					••••			-	
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CONFIG2L	—			BORV<1:0> BOR			N<1:0>	PWRTEN	346
CONFIG2H	—	—		WDPS<3:0>				N<1:0>	347
CONFIG3H	MCLRE	—	P2BMX	T3CMX	HFOFST	CCP3MX	PBADEN	CCP2MX	348
CONFIG4L	DEBUG	XINST			_	LVP		STRVEN	349

TABLE 4-5: CONFIGURATION REGISTERS ASSOCIATED WITH RESETS

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used for Resets.



FIGURE 5-1: PROGRAM MEMORY MAP AND STACK FOR PIC18(L)F2X/4XK22 DEVICES

5.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCH register. Updates to the PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see **Section 5.2.2.1 "Computed GOTO**").

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of '0'.

The PC increments by two to address sequential instructions in the program memory.

The CALL, RCALL, GOTO and program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

5.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space.

12.7.2.3 Comparator C1 Gate Operation

The output resulting from a Comparator 1 operation can be selected as a source for Timer1/3/5 Gate Control. The Comparator 1 output (sync_C1OUT) can be synchronized to the Timer1/3/5 clock or left asynchronous. For more information see **Section 18.8.4 "Synchronizing Comparator Output to Timer1"**.

12.7.2.4 Comparator C2 Gate Operation

The output resulting from a Comparator 2 operation can be selected as a source for Timer1/3/5 Gate Control. The Comparator 2 output (sync_C2OUT) can be synchronized to the Timer1/3/5 clock or left asynchronous. For more information see **Section 18.8.4 "Synchronizing Comparator Output to Timer1"**.

12.7.3 TIMER1/3/5 GATE TOGGLE MODE

When Timer1/3/5 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1/3/5 gate signal, as opposed to the duration of a single level pulse.

The Timer1/3/5 Gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 12-5 for timing details.

Timer1/3/5 Gate Toggle mode is enabled by setting the TxGTM bit of the TxGCON register. When the TxGTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note: Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

12.7.4 TIMER1/3/5 GATE SINGLE-PULSE MODE

When Timer1/3/5 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1/3/5 Gate Single-Pulse mode is first enabled by setting the TxGSPM bit in the TxGCON register. Next, the TxGGO/DONE bit in the TxGCON register must be set. The Timer1/3/5 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the TxGGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1/3/5 until the TxGGO/DONE bit is once again set in software.

Clearing the TxGSPM <u>bit of the TxGCON</u> register will also clear the TxGGO/DONE bit. See Figure 12-6 for timing details.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1/3/5 Gate source to be measured. See Figure 12-7 for timing details.

12.7.5 TIMER1/3/5 GATE VALUE STATUS

When Timer1/3/5 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the TxGVAL bit in the TxGCON register. The TxGVAL bit is valid even when the Timer1/3/5 Gate is not enabled (TMRxGE bit is cleared).

12.7.6 TIMER1/3/5 GATE EVENT INTERRUPT

When Timer1/3/5 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of TxGVAL occurs, the TMRxGIF flag bit in the PIR3 register will be set. If the TMRxGIE bit in the PIE3 register is set, then an interrupt will be recognized.

The TMRxGIF flag bit operates even when the Timer1/3/5 Gate is not enabled (TMRxGE bit is cleared).

For more information on selecting high or low priority status for the Timer1/3/5 Gate Event Interrupt see **Section 9.0 "Interrupts"**.

FIGURE 12-7:	TIMER1/3/5 GATE SING	LE-PULSE AND TOGGLE COMBINED MODE
TMRxGE		
TxGPOL		
TxGSPM		
TxGTM		
TxGG <u>O/</u> DONE	 Set by software Counting enabled of the set of the	Cleared by hardware on falling edge of TxGVAL
TxG_IN	rising edge of TxG	
ТхСКІ		
TxGVAL		
TIMER1/3/5	Ν	<u>N + 1</u> <u>N + 2</u> <u>N + 3</u> <u>N + 4</u>
TMRxGIF	Cleared by software	Set by hardware on falling edge of TxGVAL

12.12 Peripheral Module Disable

When a peripheral module is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module's clock source. The Module Disable bits for Timer1 (TMR1MD), Timer3 (TMR3MD) and Timer5 (TMR5MD) are in the PMD0 Register. See Section 3.0 "Power-Managed Modes" for more information.

15.5.8 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I^2C protocol, defined as address 0x00. When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically \overline{ACK} the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 15-24 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCLx. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.



FIGURE 15-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE

15.5.9 SSPx MASK REGISTER

An SSPx Mask (SSPxMSK) register (Register 15-6) is available in I²C Slave mode as a mask for the value held in the SSPxSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSPx operation until written with a mask value.

The SSPx Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSPx mask has no effect during the reception of the first (high) byte of the address.

15.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPxBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDAx pin after the falling edge of SCLx is asserted. SCLx is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCLx is released high. When the SCLx pin is released high, it is held that way for TBRG. The data on the SDAx pin must remain stable for that duration and some hold time after the next falling edge of SCLx. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDAx. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of \overline{ACK} is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPxIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPxBUF, leaving SCLx low and SDAx unchanged (Figure 15-28).

After the write to the SSPxBUF, each bit of the address will be shifted out on the falling edge of SCLx until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will release the SDAx pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDAx pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT Status bit of the SSPxCON2 register. Following the falling edge of the ninth clock transmission of the address, the SSPxIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPxBUF takes place, holding SCLx low and allowing SDAx to float.

15.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSPxSTAT register is set when the CPU writes to SSPxBUF and is cleared when all 8 bits are shifted out.

15.6.6.2 WCOL Status Flag

If the user writes the SSPxBUF when a transmit is already in progress (i.e., SSPxSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

15.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSPxCON2 register is cleared when the slave has sent an Acknowledge ($\overline{ACK} = 0$) and is set when the slave does not Acknowledge ($\overline{ACK} = 1$). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

15.6.6.4 Typical Transmit Sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
- 2. SSPxIF is set by hardware on completion of the Start.
- 3. SSPxIF is cleared by software.
- 4. The MSSPx module will wait the required start time before any other operation takes place.
- 5. The user loads the SSPxBUF with the slave address to transmit.
- 6. Address is shifted out the SDAx pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
- 7. The MSSPx module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
- The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
- 9. The user loads the SSPxBUF with eight bits of data.
- 10. Data is shifted out the SDAx pin until all eight bits are transmitted.
- The MSSPx module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
- 12. Steps 8-11 are repeated for all transmitted data bytes.
- The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSPx-CON2 register. Interrupt is generated once the Stop/Restart condition is complete.

15.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN, of the SSPxCON2 register. When this bit is set, the SCLx pin is pulled low and the contents of the Acknowledge data bit are presented on the SDAx pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCLx pin is deasserted (pulled high). When the SCLx pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCLx pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSPx module then goes into Idle mode (Figure 15-30).

15.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

15.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDAx pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN, of the SSPxCON2 register. At the end of a receive/transmit, the SCLx line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDAx line low. When the SDAx line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCLx pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDAx pin will be deasserted. When the SDAx pin is sampled high while SCLx is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 15-31).

15.6.9.1 WCOL Status Flag

If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 15-30: ACKNOWLEDGE SEQUENCE WAVEFORM



- 16.1.2.9 Asynchronous Reception Setup:
- Initialize the SPBRGHx:SPBRGx register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 16.4 "EUSART Baud Rate Generator (BRG)").
- 2. Set the RXx/DTx and TXx/CKx TRIS controls to '1'.
- 3. Enable the serial port by setting the SPEN bit and the RXx/DTx pin TRIS bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCxIE interrupt enable bit and set the GIE/GIEH and PEIE/GIEL bits of the INTCON register.
- 5. If 9-bit reception is desired, set the RX9 bit.
- 6. Set the DTRXP if inverted receive polarity is desired.
- 7. Enable reception by setting the CREN bit.
- 8. The RCxIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit was also set.
- 9. Read the RCSTAx register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
- 10. Get the received eight Least Significant data bits from the receive buffer by reading the RCREGx register.
- 11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

16.1.2.10 9-bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- 1. Initialize the SPBRGHx, SPBRGx register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 16.4 "EUSART Baud Rate Generator (BRG)").
- 2. Set the RXx/DTx and TXx/CKx TRIS controls to '1'.
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCxIE interrupt enable bit and set the GIE/GIEH and PEIE/GIEL bits of the INTCON register.
- 5. Enable 9-bit reception by setting the RX9 bit.
- 6. Enable address detection by setting the ADDEN bit.
- 7. Set the DTRXP if inverted receive polarity is desired.
- 8. Enable reception by setting the CREN bit.
- The RCxIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCxIE interrupt enable bit was also set.
- 10. Read the RCSTAx register to get the error flags. The ninth data bit will always be set.
- 11. Get the received eight Least Significant data bits from the receive buffer by reading the RCREGx register. Software determines if this is the device's address.
- 12. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
- 13. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

22.0 DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- ADC input channel
- DACOUT pin

The Digital-to-Analog Converter (DAC) can be enabled by setting the DACEN bit of the VREFCON1 register.

22.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the DACR<4:0> bits of the VREFCON2 register.

The DAC output voltage is determined by the following equations:

EQUATION 22-1: DAC OUTPUT VOLTAGE

$$VOUT = \left((VSRC+ - VSRC-) \neq \frac{DACR < 4:0>}{2^5} \right) + VSRC-$$
$$VSRC+ = VDD, VREF+ or FVR1$$
$$VSRC- = VSS or VREF-$$

22.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in **Section 27.0** "**Electrical Specifications**".

22.3 Low-Power Voltage State

In order for the DAC module to consume the least amount of power, one of the two voltage reference input sources to the resistor ladder must be disconnected. Either the positive voltage source, (VSRC+), or the negative voltage source, (VSRC-) can be disabled. The negative voltage source is disabled by setting the DACLPS bit in the VREFCON1 register. Clearing the DACLPS bit in the VREFCON1 register disables the positive voltage source.

22.4 Output Clamped to Positive Voltage Source

The DAC output voltage can be set to VsRC+ with the least amount of power consumption by performing the following:

- Clearing the DACEN bit in the VREFCON1 register.
- Setting the DACLPS bit in the VREFCON1 register.
- Configuring the DACPSS bits to the proper positive source.
- Configuring the DACRx bits to '11111' in the VREFCON2 register.

This is also the method used to output the voltage level from the FVR to an output pin. See **Section 22.6 "DAC Voltage Reference Output"** for more information.

22.5 Output Clamped to Negative Voltage Source

The DAC output voltage can be set to VSRC- with the least amount of power consumption by performing the following:

- Clearing the DACEN bit in the VREFCON1 register.
- Clearing the DACLPS bit in the VREFCON1 register.
- Configuring the DACPSS bits to the proper negative source.
- Configuring the DACRx bits to '00000' in the VREFCON2 register.

This allows the comparator to detect a zero-crossing while not consuming additional current through the DAC module.

22.6 DAC Voltage Reference Output

The DAC can be output to the DACOUT pin by setting the DACOE bit of the VREFCON1 register to '1'. Selecting the DAC reference voltage for output on the DACOUT pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACOUT pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to DACOUT. Figure 22-2 shows an example buffering technique.

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—			DACR<4:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 22-2: VREFCON2: VOLTAGE REFERENCE CONTROL REGISTER 1

bit 7-5 Unimplemented: Read as '0'

bit 4-0 DACR<4:0>: DAC Voltage Output Select bits VOUT = ((VSRC+) - (VSRC-))*(DACR<4:0>/(2⁵)) + VSRC-

TABLE 22-1: REGISTERS ASSOCIATED WITH DAC MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
VREFCON0	FVREN	FVRST	FVRS	<1:0>	—	—	—	—	332
VREFCON1	DACEN	DACLPS	DACOE	—	DACPS	SS<1:0>	—	DACNSS	335
VREFCON2	—	—	—			DACR<4:0>			336

Legend: — = Unimplemented locations, read as '0'. Shaded bits are not used by the DAC module.

RRN	NCF	R	otate R	lig	ght f (N	o Ca	rry)	
Synt	ax:	RI	RNCF	fł	{,d {,a}}			
Oper	rands:	0 : d a	≤ f ≤ 258 ∈ [0,1] ∈ [0,1]	5				
Oper	ration:	(f< (f<	$(n>) \rightarrow ($ $(0>) \rightarrow ($	de de	st <n 1<br="" –="">st<7></n>	>,		
Statu	is Affected:	N,	Z					
Enco	oding:		0100		00da	fff	f	ffff
Desc	pription:	Th or pland If see in se in m Se Bi Li	ne conte ne bit to placed i aced ba 'a' is '0', elected (ilue. If 'a elected a 'a' is '0' ti s enal Indexec ode whe ection 2 torient teral Of	nt the ck the deating are ble ter fs ►	s of regi e right. I W. If 'd' in regis fault), o s '1', the per the ad the ex- ed, this i literal Of ever $f \leq$ 2.3 "By d Instrue et Mode	ster 'f' f 'd' is is '1', ter 'f' ss Bar verridi en the BSR v ktende nstruc ffset A 95 (5F te-Ori ction e ³ for egister	' are ' 0', the (defa hk wi ing t ban value ed in tion defa Fh). S enter s in f	rotated the result result is ault). ill be he BSR k will be e. struction operates essing See ed and Indexed ils.
Word	ds:	1						
Cycle	es:	1						
QU			02		03	1		04
	Decode		Read		Proce	ess	v	Vrite to
		reę	gister 'f'		Dat	a	de	stination
<u>Exar</u>	nple 1: Before Instruc REG After Instructic REG	RF tion = on =	RNCF 1101 1110	R 0	EG, 1, 111 011	0		
Exar	nple 2:	RF	RNCF	R	EG, 0,	0		
	Before Instruc	tion						
	W	=	?					
	REG After Instructio	= on	1101	0	111			
	W REG	=	1110 1101	1	011 111			
		_	U -	0	* * *			

SETF	Set f			
Syntax:	SETF f{,	a}		
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]			
Operation:	$FFh\tof$			
Status Affected:	None			
Encoding:	0110	100a	ffff	ffff
	are set to F If 'a' is '0', t If 'a' is '1', t GPR bank. If 'a' is '0' a set is enab in Indexed mode wher Section 25 Bit-Oriente Literal Offs	Fh. the Access the BSR i und the ex led, this i Literal O never f ≤ 5.2.3 "By ed Instru set Mode	ss Bank is is used to struction ffset Addre 95 (5Fh). te-Oriente ctions in e" for deta	selected. select the struction operates essing See ed and Indexed ils.
Words:	1			
Cycles:	1			
Q Cycle Activity:				
Q1	Q2	Q3	3	Q4
Decode	Read register 'f'	Proce Dat	ess a re	Write gister 'f'
Example: Before Instru REG	SETF ction = 5A	REG \h	3, 1	

= FFh

REG

SUBWFB	Subtract W from f with Borrow						
Syntax:	SI	JBWFB	f {,d {,a	n}}			
Operands:	0 : d a	≤ f ≤ 255 ∈ [0,1] ∈ [0,1]					
Operation:	(f)	– (W) –	$(\overline{C}) \rightarrow de$	st			
Status Affected:	N, OV, C, DC, Z						
Encoding:		0101	10da	fff	f ffff		
Description:	Su (b) sta sta sta f' GF ff Se in ma Se Bi Lit	ubtract W orrow) fro ent metho bred in W bred back a' is '0', 1 PR bank. a' is '0' a ti s enab Indexed bode where ection 25 t-Oriente teral Official	and the form register $(-1)^{-1}$ and the form register $(-1)^{-1}$. If $(-1)^{-1}$ is $(-1)^{-1}$, if $(-1)^{-1}$ is $(-1)^{-1}$. If $(-1)^{-1}$ is $(-1)^{-1}$, if $(-1)^{-1}$ is $(-1)^{-1}$, if $(-1)^{-1}$ is $(-1)^{-1}$. The form $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$. The form $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$. The form $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$. The form $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$ is $(-1)^{-1}$. The form $(-1)^{-1}$ is $(-1)^{-$	CARR er 'f' (2 is '0', t 1', the er 'f' (0 is Ban s used attende fiset An 95 (5F te-Oria ctions " for o	Y flag 2's comple- the result is default). k is selected. I to select the d instruction tion operates ddressing h). See ented and s in Indexed details.		
Words:	1						
Cvcles:	1						
Q Cycle Activity:							
Q1		Q2	Q	3	Q4		
Decode		Read	Proce	ess	Write to		
	re	gister 'f'	Dat	a	destination		
Example 1:	5	SUBWFB	REG, 1	, 0			
Before Instruc REG W C	tion = = =	19h 0Dh 1	(000)	1 100 0 110	01) 01)		
After Instructio REG W C Z	n = = =	0Ch 0Dh 1 0	(000)	0 110 0 110	00) 01)		
Ν	=	0	; resu	lt is po	sitive		
Example 2:	S	SUBWFB	REG, 0	, 0			
Before Instruc REG W C	tion = = =	1Bh 1Ah 0	(000)	1 101 1 101	.1) .0)		
After Instructic REG W C	n = =	1Bh 00h 1	(000)	1 101	1)		
Ž N	= =	1 0	; resu	lt is ze	ro		
Example 3:	5	SUBWFB	REG, 1	, 0			
Before Instruc REG W C	tion = = =	03h 0Eh 1	(000)	0 001 0 111	.1) .0)		
After Instructio REG	n = =	F5h 0Eh	(111); ; [2's ((000)	1 010 comp] 0 111	01) .0)		
C Z N	= = =	0 0 1	; resu	lt is ne	egative		

SWAPF	Swap f					
Syntax:	SWAPF 1	{,d {,a}}				
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]	5				
Operation:	(f<3:0>) → (f<7:4>) →	→ dest<7:4 → dest<3:0	l>,)>			
Status Affected:	None					
Encoding:	0011	10da	ffff	ffff		
Dooolpiion	'f' are exch is placed in r placed in r If 'a' is '0', If 'a' is '1', GPR bank If 'a' is '0'; set is enak in Indexed mode whe Section 2 Bit-Orient Literal Off	hanged. If n W. If 'd' register 'f' the Access the BSR i and the e: bled, this i Literal O never $f \le$ 5.2.3 "By red Instruction fset Mode	'd' is '0', t is '1', the (default). ss Bank is is used to struction ffset Addre 95 (5Fh). te-Oriente ictions in e" for deta	he result result is selected. select the struction operates sessing See ed and Indexed ils.		
Words:	1					
Cycles:	1					
Q Cycle Activity:						
Q1	Q2	Q3	3	Q4		

Decode	Read	Process	Write to
	register 'f'	Data	destination

REG, 1, 0

Example:

SWAPF

Before Instruction REG = 53h After Instruction REG = 35h











FIGURE 28-73: PIC18LF2X/4XK22 MAXIMUM IDD: SEC_RUN 32.768 kHz





FIGURE 28-101: PIC18LF2X/4XK22 TYPICAL LF-INTOSC FREQUENCY vs. VDD Min/Max = 31.25 kHz ± 15%, T = -40°C to +85°C





28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Optional Center Pad Width	W2			4.25	
Optional Center Pad Length	T2			4.25	
Contact Pad Spacing	C1		5.70		
Contact Pad Spacing	C2		5.70		
Contact Pad Width (X28)	X1			0.37	
Contact Pad Length (X28)	Y1			1.00	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

Features ⁽¹⁾	PIC18F23K22 PIC18LF23K2 2	PIC18F24K22 PIC18LF24K2 2	PIC18F25K22 PIC18LF25K22	PIC18F26K22 PIC18LF26K22	PIC18F43K22 PIC18LF43K22	PIC18F44K22 PIC18LF44K22	PIC18F45K22 PIC18LF45K22	PIC18F46K22 PIC18LF46K22
Program Memory (Bytes)	8192	16384	32768	65536	8192	16384	32768	65536
SRAM (Bytes)	512	768	1536	3896	512	768	1536	3896
EEPROM (Bytes)	256	256	256	1024	256	256	256	1024
Interrupt Sources	26	26	33	33	26	26	33	33
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E			
Capture/Compare/PWM Modules (CCP)	2	2	2	2	2	2	2	2
Enhanced CCP Modules (ECCP) Full Bridge	1	1	1	1	2	2	2	2
ECCP Module Half Bridge	2	2	2	2	1	1	1	1
10-bit Analog-to-Digital Module	17 input channels	17 input channels	17 input channels	17 input channels	28 input channels	28 input channels	28 input channels	28 input channels
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN			

TABLE B-1: DEVICE DIFFERENCES

Note 1: PIC18FXXK22: operating voltage, 2.3V-5.5V. PIC18LFXXK22: operating voltage, 1.8V-3.6V.