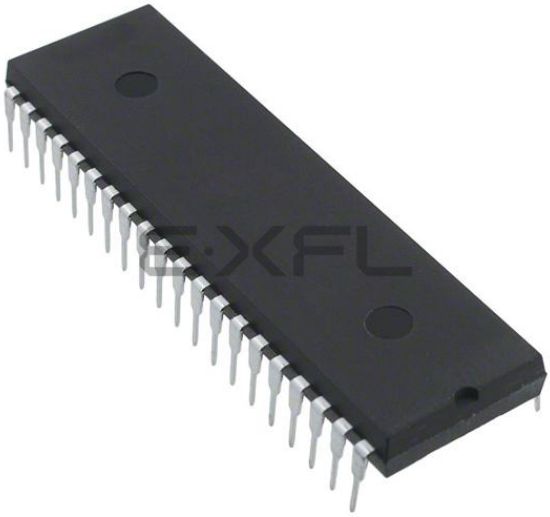

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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 64MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 8KB (4K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 30x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 40-DIP (0.600", 15.24mm) |
| Supplier Device Package | 40-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f43k22-i-p |

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**TABLE 4-1: BOR CONFIGURATIONS**

| BOR Configuration | | Status of SBOREN (RCON<6>) | BOR Operation |
|---|---|---|---|
| BOREN1 | BOREN0 | | |
| 0 | 0 | Unavailable | BOR disabled; must be enabled by reprogramming the Configuration bits. |
| 0 | 1 | Available | BOR enabled by software; operation controlled by SBOREN. |
| 1 | 0 | Unavailable | BOR enabled by hardware in Run and Idle modes, disabled during Sleep mode. |
| 1 | 1 | Unavailable | BOR enabled by hardware; must be disabled by reprogramming the Configuration bits. |

## 4.6 Device Reset Timers

PIC18(L)F2X/4XK22 devices incorporate three separate on-chip timers that help regulate the Power-on Reset process. Their main function is to ensure that the device clock is stable before code is executed. These timers are:

- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- PLL Lock Time-out

### 4.6.1 POWER-UP TIMER (PWRT)

The Power-up Timer (PWRT) of PIC18(L)F2X/4XK22 devices is an 11-bit counter which uses the LFINTOSC source as the clock input. This yields an approximate time interval of 2048 x 32 μs = 65.6 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the LFINTOSC clock and will vary from chip-to-chip due to temperature and process variation.

The PWRT is enabled by clearing the $\overline{\text{PWRTEN}}$ Configuration bit.

### 4.6.2 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset, or on exit from all power-managed modes that stop the external oscillator.

### 4.6.3 PLL LOCK TIME-OUT

With the PLL enabled, the time-out sequence following a Power-on Reset is slightly different from other oscillator modes. A separate timer is used to provide a fixed time-out that is sufficient for the PLL to lock to the main oscillator frequency. This PLL lock time-out ($T_{PLL}$) is typically 2 ms and follows the oscillator start-up time-out.

### 4.6.4 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

1. After the POR pulse has cleared, PWRT time-out is invoked (if enabled).
2. Then, the OST is activated.

The total time-out will vary based on oscillator configuration and the status of the PWRT. Figure 4-3, Figure 4-4, Figure 4-5, Figure 4-6 and Figure 4-7 all depict time-out sequences on power-up, with the Power-up Timer enabled and the device operating in HS Oscillator mode. Figures 4-3 through 4-6 also apply to devices operating in XT or LP modes. For devices in RC mode and with the PWRT disabled, on the other hand, there will be no time-out at all.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, all time-outs will expire, after which, bringing $\overline{\text{MCLR}}$ high will allow program execution to begin immediately (Figure 4-5). This is useful for testing purposes or to synchronize more than one PIC® MCU device operating in parallel.

**REGISTER 9-2: INTCON2: INTERRUPT CONTROL 2 REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | U-0 | R/W-1 | U-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{RBPU}}$ | INTEDG0 | INTEDG1 | INTEDG2 | — | TMR0IP | — | RBIP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **$\overline{\text{RBPU}}$:** PORTB Pull-up Enable bit
1 = All PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled provided that the pin is an input and the corresponding WPUB bit is set.

bit 6 **INTEDG0:** External Interrupt 0 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 5 **INTEDG1:** External Interrupt 1 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 4 **INTEDG2:** External Interrupt 2 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge

bit 3 **Unimplemented:** Read as '0'

bit 2 **TMR0IP:** TMR0 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 **Unimplemented:** Read as '0'

bit 0 **RBIP:** RB Port Change Interrupt Priority bit
1 = High priority
0 = Low priority

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

**REGISTER 9-4: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1**

| U-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | ADIF | RC1IF | TX1IF | SSP1IF | CCP1IF | TMR2IF | TMR1IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **Unimplemented:** Read as '0'.

bit 6 **ADIF:** A/D Converter Interrupt Flag bit
1 = An A/D conversion completed (must be cleared by software)
0 = The A/D conversion is not complete or has not been started

bit 5 **RC1IF:** EUSART1 Receive Interrupt Flag bit
1 = The EUSART1 receive buffer, RCREG1, is full (cleared when RCREG1 is read)
0 = The EUSART1 receive buffer is empty

bit 4 **TX1IF:** EUSART1 Transmit Interrupt Flag bit
1 = The EUSART1 transmit buffer, TXREG1, is empty (cleared when TXREG1 is written)
0 = The EUSART1 transmit buffer is full

bit 3 **SSP1IF:** Master Synchronous Serial Port 1 Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared by software)
0 = Waiting to transmit/receive

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR register capture occurred (must be cleared by software)
0 = No TMR register capture occurred
Compare mode:
1 = A TMR register compare match occurred (must be cleared by software)
0 = No TMR register compare match occurred
PWM mode:
Unused in this mode

bit 1 **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared by software)
0 = No TMR2 to PR2 match occurred

bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared by software)
0 = TMR1 register did not overflow

**Note 1:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE/GIEH of the INTCON register.

**Note:** User software should ensure the appropriate interrupt flag bits are cleared prior to enabling an interrupt and after servicing that interrupt.

**REGISTER 9-6: PIR3: PERIPHERAL INTERRUPT (FLAG) REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSP2IF | BCL2IF | RC2IF | TX2IF | CTMUIF | TMR5GIF | TMR3GIF | TMR1GIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **SSP2IF:** Synchronous Serial Port Interrupt Flag bit
1 = The transmission/reception is complete (must be cleared in software)
0 = Waiting to transmit/receive

bit 6 **BCL2IF:** MSSP2 Bus Collision Interrupt Flag bit
1 = A bus collision has occurred while the SSP2 module configured in $I^2C$ master was transmitting (must be cleared in software)
0 = No bus collision occurred

bit 5 **RC2IF:** EUSART2 Receive Interrupt Flag bit
1 = The EUSART2 receive buffer, RCREG2, is full (cleared by reading RCREG2)
0 = The EUSART2 receive buffer is empty

bit 4 **TX2IF:** EUSART2 Transmit Interrupt Flag bit
1 = The EUSART2 transmit buffer, TXREG2, is empty (cleared by writing TXREG2)
0 = The EUSART2 transmit buffer is full

bit 3 **CTMUIF:** CTMU Interrupt Flag bit
1 = CTMU interrupt occurred (must be cleared in software)
0 = No CTMU interrupt occurred

bit 2 **TMR5GIF:** TMR5 Gate Interrupt Flag bits
1 = TMR gate interrupt occurred (must be cleared in software)
0 = No TMR gate occurred

bit 1 **TMR3GIF:** TMR3 Gate Interrupt Flag bits
1 = TMR gate interrupt occurred (must be cleared in software)
0 = No TMR gate occurred

bit 0 **TMR1GIF:** TMR1 Gate Interrupt Flag bits
1 = TMR gate interrupt occurred (must be cleared in software)
0 = No TMR gate occurred

## 14.1 Capture Mode

The Capture mode function described in this section is identical for all CCP and ECCP modules available on this device family.

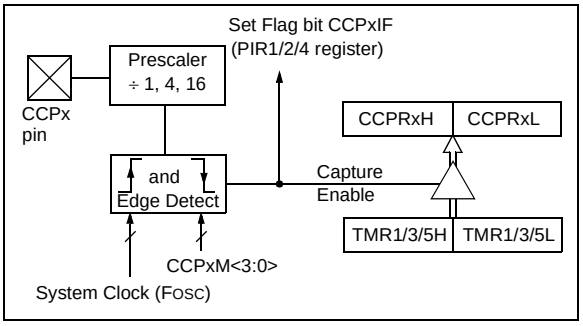
Capture mode makes use of the 16-bit Timer resources, Timer1, Timer3 and Timer5. The timer resources for each CCP capture function are independent and are selected using the CCPTMRS0 and CCPTMRS1 registers. When an event occurs on the CCPx pin, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMRxH:TMRxL register pair, respectively. An event is defined as one of the following and is configured by the CCPxM<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the corresponding Interrupt Request Flag bit CCPxIF of the PIR1, PIR2 or PIR4 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH:CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 14-1 shows a simplified diagram of the Capture operation.

**FIGURE 14-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**




### 14.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Some CCPx outputs are multiplexed on a couple of pins. Table 14-2 shows the CCP output pin multiplexing. Selection of the output pin is determined by the CCPxMX bits in Configuration register 3H (CONFIG3H). Refer to Register 24-4 for more details.

| **Note:** | If the CCPx pin is configured as an output, a write to the port can cause a capture condition. |
|---|---|

**TABLE 14-2: CCP PIN MULTIPLEXING**

| CCP OUTPUT | CONFIG 3H Control Bit | Bit Value | PIC18(L)F2XK22 I/O pin | PIC18(L)F4XK22 I/O pin |
|---|---|---|---|---|
| CCP2 | CCP2MX | 0 | RB3 | RB3 |
| | | 1(*) | RC1 | RC1 |
| CCP3 | CCP3MX | 0(*) | RC6 | RE0 |
| | | 1 | RB5 | RB5 |

**Legend:** * = Default

### 14.1.2 TIMER1 MODE RESOURCE

The 16-bit Timer resource must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See **Section 12.0 "Timer1/3/5 Module with Gate Control"** for more information on configuring the 16-bit Timers.

### 14.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIE1, PIE2 or PIE4 register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIR1, PIR2 or PIR4 register following any change in Operating mode.

| **Note:** | Clocking the 16-bit Timer resource from the system clock (FOSC) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, the Timer resource must be clocked from the instruction clock (FOSC/4) or from an external clock source. |
|---|---|

**REGISTER 14-3: CCPTMRS0: PWM TIMER SELECTION CONTROL REGISTER 0**

| R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| C3TSEL<1:0> | | — | C2TSEL<1:0> | | — | C1TSEL<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-6 **C3TSEL<1:0>:** CCP3 Timer Selection bits
00 = CCP3 – Capture/Compare modes use Timer1, PWM modes use Timer2
01 = CCP3 – Capture/Compare modes use Timer3, PWM modes use Timer4
10 = CCP3 – Capture/Compare modes use Timer5, PWM modes use Timer6
11 = Reserved

bit 5 **Unused**

bit 4-3 **C2TSEL<1:0>:** CCP2 Timer Selection bits
00 = CCP2 – Capture/Compare modes use Timer1, PWM modes use Timer2
01 = CCP2 – Capture/Compare modes use Timer3, PWM modes use Timer4
10 = CCP2 – Capture/Compare modes use Timer5, PWM modes use Timer6
11 = Reserved

bit 2 **Unused**

bit 1-0 **C1TSEL<1:0>:** CCP1 Timer Selection bits
00 = CCP1 – Capture/Compare modes use Timer1, PWM modes use Timer2
01 = CCP1 – Capture/Compare modes use Timer3, PWM modes use Timer4
10 = CCP1 – Capture/Compare modes use Timer5, PWM modes use Timer6
11 = Reserved

**REGISTER 14-4: CCPTMRS1: PWM TIMER SELECTION CONTROL REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | C5TSEL<1:0> | | C4TSEL<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-2 **C5TSEL<1:0>:** CCP5 Timer Selection bits
00 = CCP5 – Capture/Compare modes use Timer1, PWM modes use Timer2
01 = CCP5 – Capture/Compare modes use Timer3, PWM modes use Timer4
10 = CCP5 – Capture/Compare modes use Timer5, PWM modes use Timer6
11 = Reserved

bit 1-0 **C4TSEL<1:0>:** CCP4 Timer Selection bits
00 = CCP4 – Capture/Compare modes use Timer1, PWM modes use Timer2
01 = CCP4 – Capture/Compare modes use Timer3, PWM modes use Timer4
10 = CCP4 – Capture/Compare modes use Timer5, PWM modes use Timer6
11 = Reserved

**REGISTER 14-6: PWMxCON: ENHANCED PWM CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PxRSEN | PxDC<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7 **PxRSEN:** PWM Restart Enable bit
- 1 = Upon auto-shutdown, the CCPxASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically
- 0 = Upon auto-shutdown, CCPxASE must be cleared in software to restart the PWM

bit 6-0 **PxDC<6:0>:** PWM Delay Count bits

PxDCx = Number of FOSC/4 (4 * TOSC) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it transitions active

**REGISTER 14-7: PSTRxCON: PWM STEERING CONTROL REGISTER(1)**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | STRxSYNC | STRxD | STRxC | STRxB | STRxA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **STRxSYNC:** Steering Sync bit
- 1 = Output steering update occurs on next PWM period
- 0 = Output steering update occurs at the beginning of the instruction cycle boundary

bit 3 **STRxD:** Steering Enable bit D
- 1 = PxD pin has the PWM waveform with polarity control from CCPxM<1:0>
- 0 = PxD pin is assigned to port pin

bit 2 **STRxC:** Steering Enable bit C
- 1 = PxC pin has the PWM waveform with polarity control from CCPxM<1:0>
- 0 = PxC pin is assigned to port pin

bit 1 **STRxB:** Steering Enable bit B
- 1 = PxB pin has the PWM waveform with polarity control from CCPxM<1:0>
- 0 = PxB pin is assigned to port pin

bit 0 **STRxA:** Steering Enable bit A
- 1 = PxA pin has the PWM waveform with polarity control from CCPxM<1:0>
- 0 = PxA pin is assigned to port pin

**Note 1:** The PWM Steering mode is available only when the CCPxCON register bits CCPxM<3:2> = 11 and PxM<1:0> = 00.

**REGISTER 15-7: SSPxADD: MSSPx ADDRESS AND BAUD RATE REGISTER ($I^2C$ MODE)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADD<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

**Master mode:**

bit 7-0 **ADD<7:0>:** Baud Rate Clock Divider bits
SCLx pin clock period = ((ADD<7:0> + 1) *4)/FOSC

**10-Bit Slave mode — Most Significant Address byte:**

bit 7-3 **Not used:** Unused for Most Significant Address byte. Bit state of this register is a "don't care". Bit pattern sent by master is fixed by $I^2C$ specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.

bit 2-1 **ADD<2:1>:** Two Most Significant bits of 10-bit address

bit 0 **Not used:** Unused in this mode. Bit state is a "don't care".

**10-Bit Slave mode — Least Significant Address byte:**

bit 7-0 **ADD<7:0>:** Eight Least Significant bits of 10-bit address

**7-Bit Slave mode:**

bit 7-1 **ADD<7:1>:** 7-bit address

bit 0 **Not used:** Unused in this mode. Bit state is a "don't care".

**REGISTER 24-3: CONFIG2H: CONFIGURATION REGISTER 2 HIGH**

| U-0 | U-0 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 |
|---|---|---|---|---|---|---|---|
| — | — | WDTPS<3:0> | | | | WDTEN<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | P = Programmable bit | U = Unimplemented bit, read as '0' |
| -n = Value when device is unprogrammed | | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **WDTPS<3:0>:** Watchdog Timer Postscale Select bits
1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1

bit 1-0 **WDTEN<1:0>:** Watchdog Timer Enable bits
11 = WDT enabled in hardware; SWDTEN bit disabled
10 = WDT controlled by the SWDTEN bit
01 = WDT enabled when device is active, disabled when device is in Sleep; SWDTEN bit disabled
00 = WDT disabled in hardware; SWDTEN bit disabled

**XORWF** **Exclusive OR W with f**

Syntax: XORWF f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .XOR. (f) → dest

Status Affected: N, Z

Encoding:

| 0001 | 10da | ffff | ffff |
|---|---|---|---|

Description: Exclusive OR the contents of W with register 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register 'f' (default).
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process Data | Write to destination |

Example: `XORWF REG, 1, 0`

Before Instruction
REG = AFh
W = B5h
After Instruction
REG = 1Ah
W = B5h

### 25.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB® IDE TOOLS

The latest versions of Microchip's software tools have been designed to fully support the extended instruction set of the PIC18(L)F2X/4XK22 family of devices. This includes the MPLAB C18 C compiler, MPASM assembly language and MPLAB Integrated Development Environment (IDE).

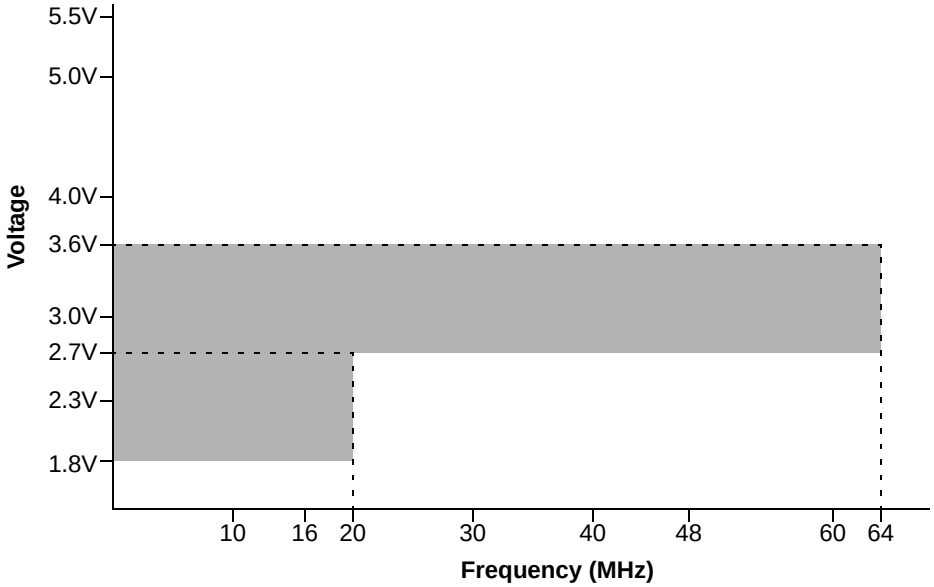
When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is '0', disabling the extended instruction set and Indexed Literal Offset Addressing mode. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

- A menu option, or dialog box within the environment, that allows the user to configure the language tool and its settings for the project
- A command line option
- A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.

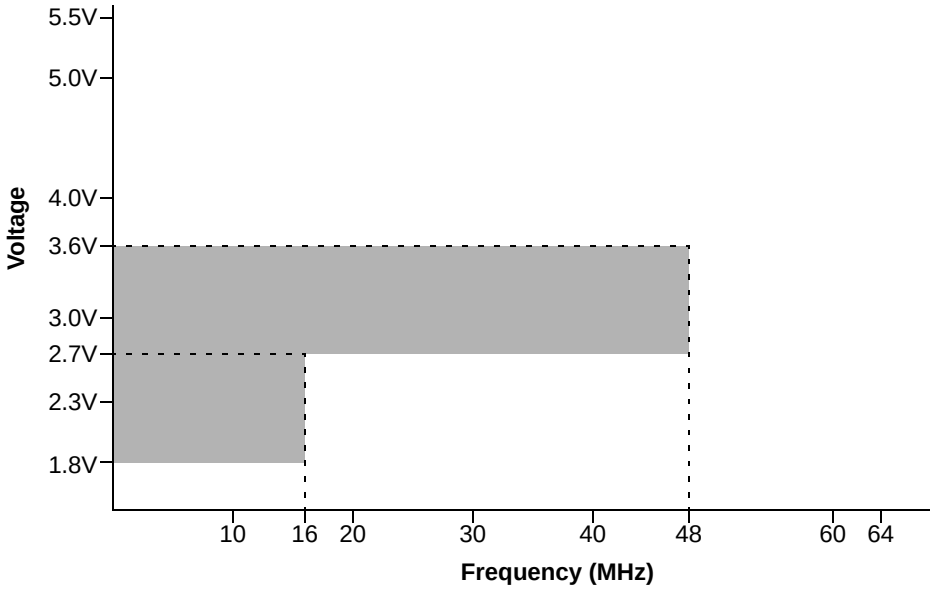
**FIGURE 27-1: PIC18LF2X/4XK22 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL TEMPERATURE)**




**Note 1:** Maximum Frequency 20 MHz, 1.8V to 2.7V, -40°C to +85°C

**2:** Maximum Frequency 64 MHz, 2.7V to 3.6V, -40°C to +85°C

**FIGURE 27-2: PIC18LF2X/4XK22 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED TEMPERATURE)**




**Note 1:** Maximum Frequency 16 MHz, 1.8V to 2.7V, +85°C to +125°C

**2:** Maximum Frequency 48 MHz, 2.7V to 3.6V, +85°C to +125°C

27.11.3 TIMING DIAGRAMS AND SPECIFICATIONS

**FIGURE 27-7: EXTERNAL CLOCK TIMING (ALL MODES EXCEPT PLL)**

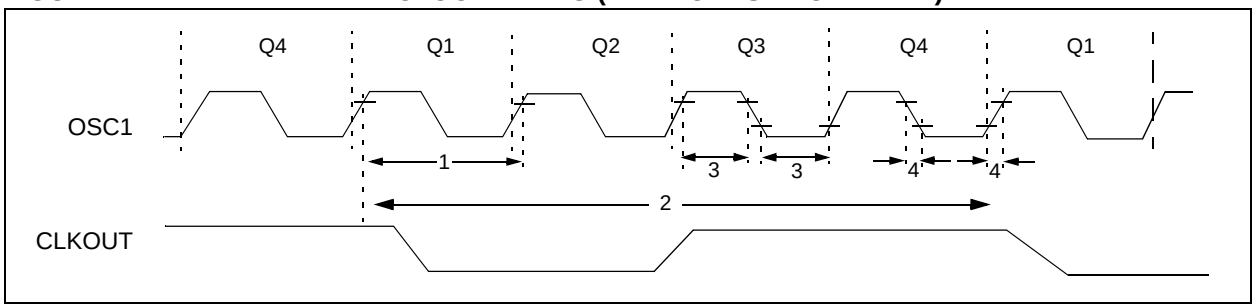



**TABLE 27-7: EXTERNAL CLOCK TIMING REQUIREMENTS**

| Param. No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| 1A | FOSC | External CLKIN Frequency(1) | DC | 0.5 | MHz | EC, ECIO Oscillator mode (low power) |
| | | | DC | 16 | MHz | EC, ECIO Oscillator mode (medium power) |
| | | | DC | 64 | MHz | EC, ECIO Oscillator mode (high power) |
| | | Oscillator Frequency(1) | DC | 4 | MHz | RC Oscillator mode |
| | | | 5 | 200 | kHz | LP Oscillator mode |
| | | | 0.1 | 4 | MHz | XT Oscillator mode |
| | | | 4 | 4 | MHz | HS Oscillator mode, VDD < 2.7V |
| | | | 4 | 16 | MHz | HS Oscillator mode, VDD ≥ 2.7V, Medium-Power mode (HSMP) |
| | | | 4 | 20 | MHz | HS Oscillator mode, VDD ≥ 2.7V, High-Power mode (HSHP) |
| 1 | TOSC | External CLKIN Period(1) | 2.0 | — | µs | EC, ECIO Oscillator mode (low power) |
| | | | 62.5 | — | ns | EC, ECIO Oscillator mode (medium power) |
| | | | 15.6 | — | ns | EC, ECIO Oscillator mode (high power) |
| | | Oscillator Period(1) | 250 | — | ns | RC Oscillator mode |
| | | | 5 | 200 | µs | LP Oscillator mode |
| | | | 0.25 | 10 | µs | XT Oscillator mode |
| | | | 250 | 250 | ns | HS Oscillator mode, VDD < 2.7V |
| | | | 62.5 | 250 | ns | HS Oscillator mode, VDD ≥ 2.7V, Medium-Power mode (HSMP) |
| | | | 50 | 250 | ns | HS Oscillator mode, VDD ≥ 2.7V, High-Power mode (HSHP) |
| 2 | TCY | Instruction Cycle Time(1) | 62.5 | — | ns | TCY = 4/FOSC |
| 3 | TOSL, TOSH | External Clock in (OSC1) High or Low Time | 2.5 | — | µs | LP Oscillator mode |
| | | | 30 | — | ns | XT Oscillator mode |
| | | | 10 | — | ns | HS Oscillator mode |
| 4 | TOSR, TOSF | External Clock in (OSC1) Rise or Fall Time | — | 50 | ns | LP Oscillator mode |
| | | | — | 20 | ns | XT Oscillator mode |
| | | | — | 7.5 | ns | HS Oscillator mode |

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

**TABLE 27-22: A/D CONVERSION REQUIREMENTS PIC18(L)F2X/4XK22**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature Tested at +25°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| 130 | TAD | A/D Clock Period | 1 | — | 25 | µs | -40°C to +85°C |
| | | | 1 | — | 4 | µs | +85°C to +125°C |
| 131 | TCNV | Conversion Time (not including acquisition time) **(Note 1)** | 11 | — | 11 | TAD | |
| 132 | TACQ | Acquisition Time **(Note 2)** | 1.4 | — | — | µs | VDD = 3V, Rs = 50Ω |
| 135 | TSWC | Switching Time from Convert → Sample | — | — | **(Note 3)** | | |
| 136 | TDIS | Discharge Time | 1 | — | 1 | TCY | |

**Note 1:** ADRES register may be read on the following TCY cycle.

**2:** The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (*RS*) on the input channels is 50 Ω.

**3:** On the following cycle of the device clock.

**FIGURE 28-50: PIC18F2X/4XK22 TYPICAL IDD: PRI_RUN EC MEDIUM POWER**

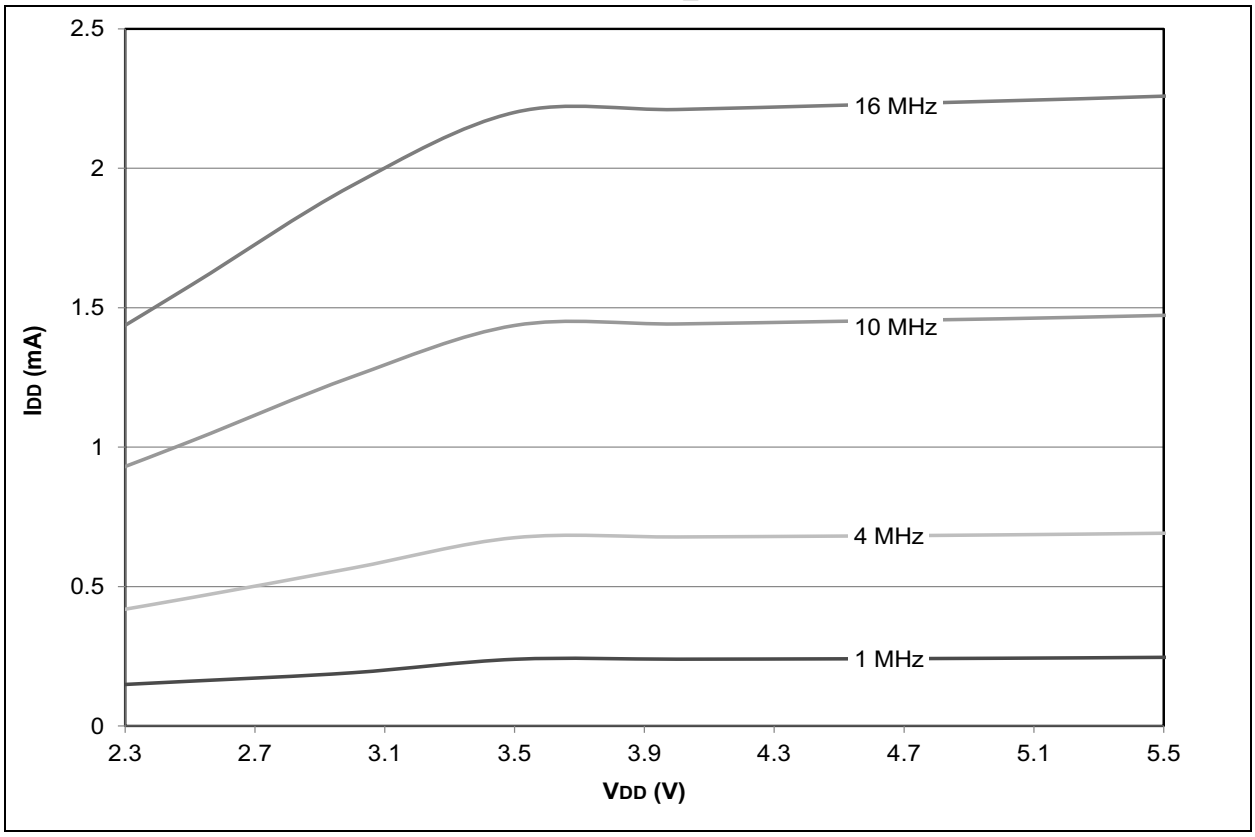



**FIGURE 28-51: PIC18F2X/4XK22 MAXIMUM IDD: PRI_RUN EC MEDIUM POWER**

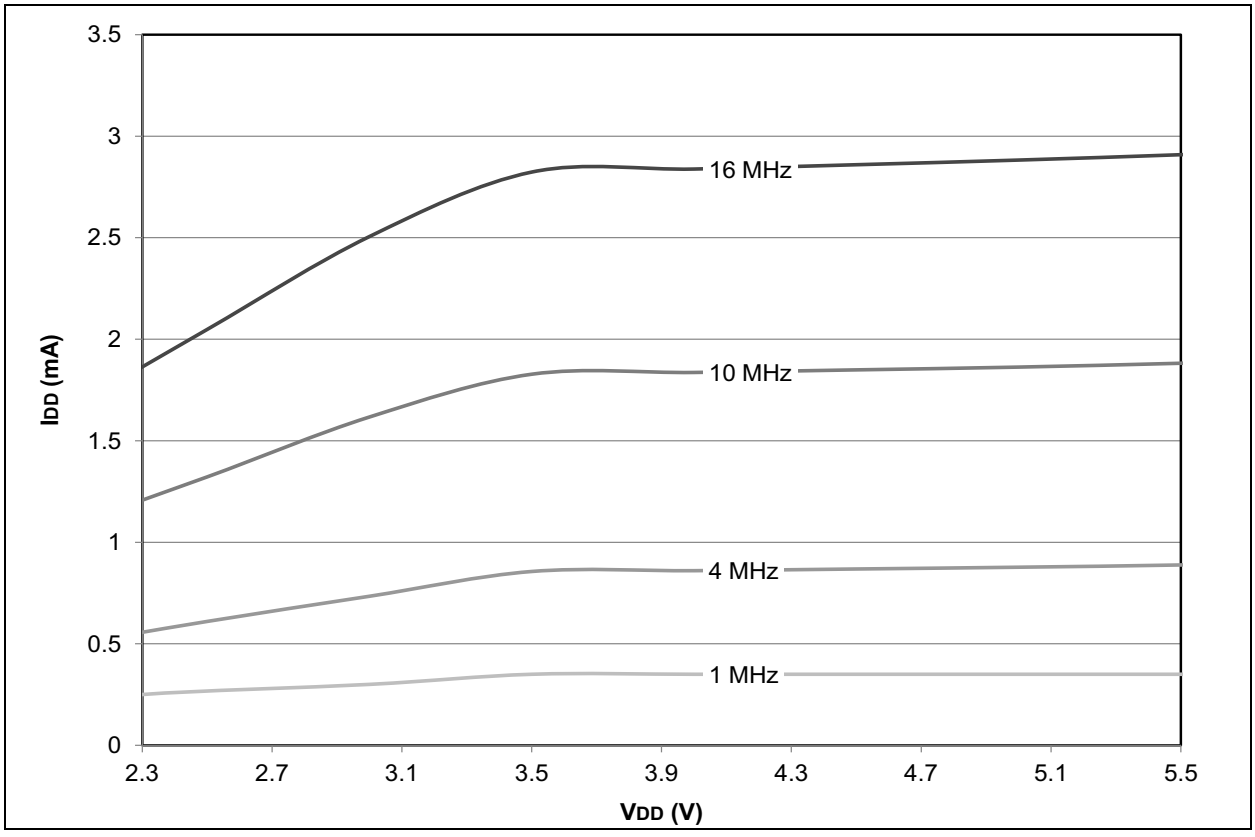


**FIGURE 28-80: PIC18(L)F2X/4XK22 TTL BUFFER INPUT LOW VOLTAGE**

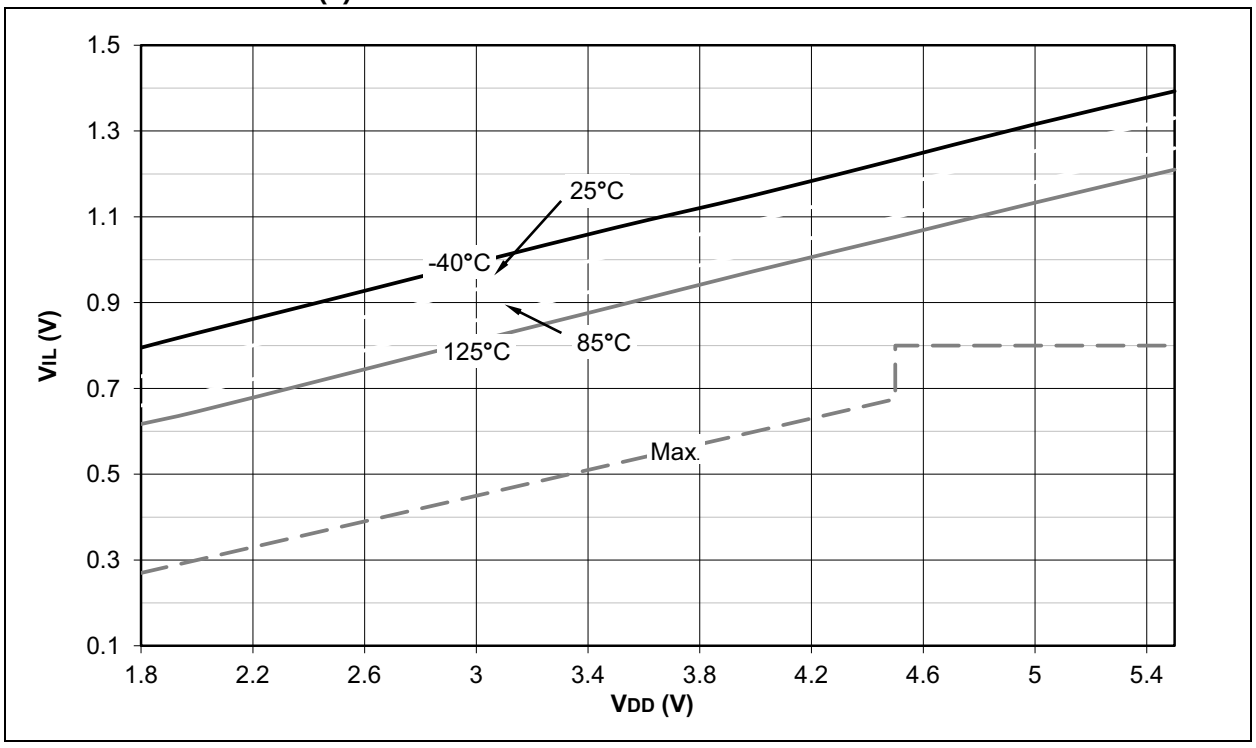
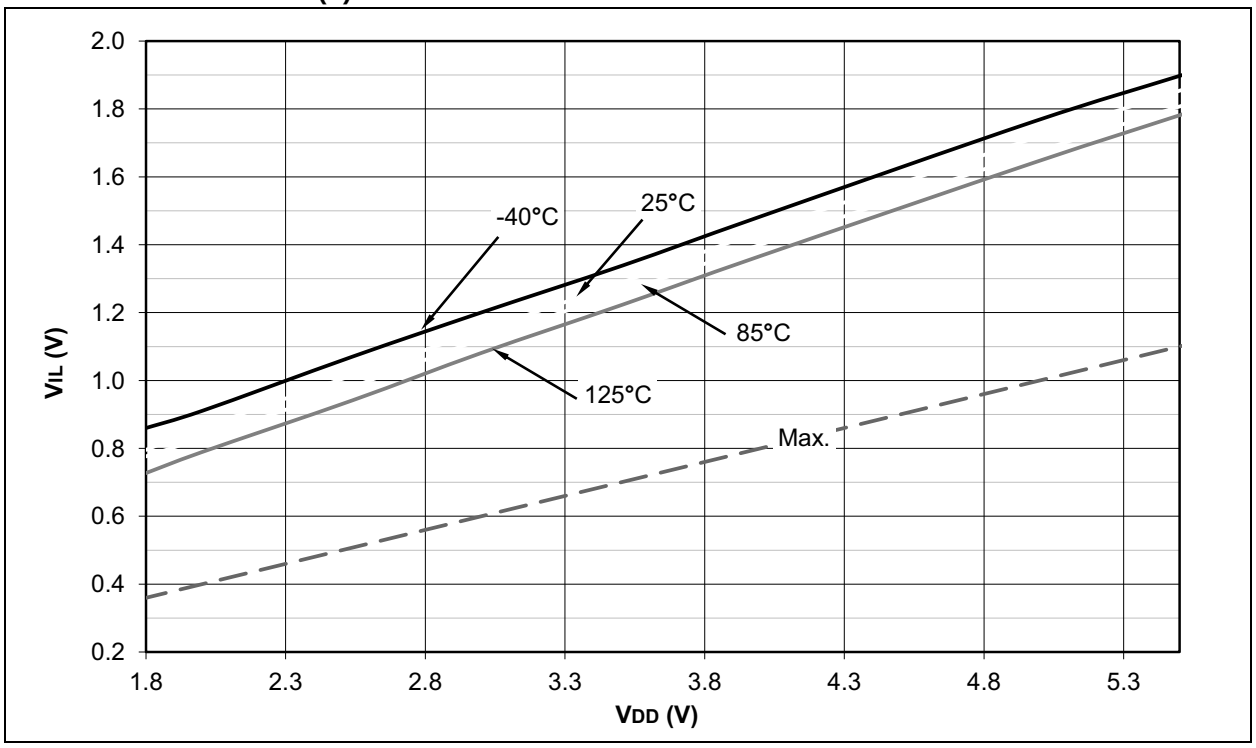
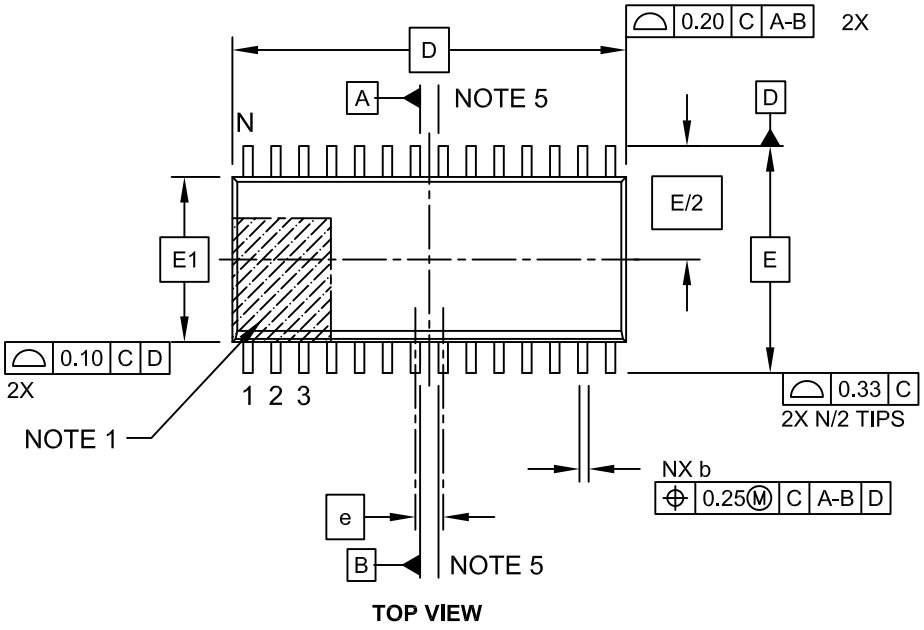



**FIGURE 28-81: PIC18(L)F2X/4XK22 SCHMITT TRIGGER BUFFER INPUT LOW VOLTAGE**

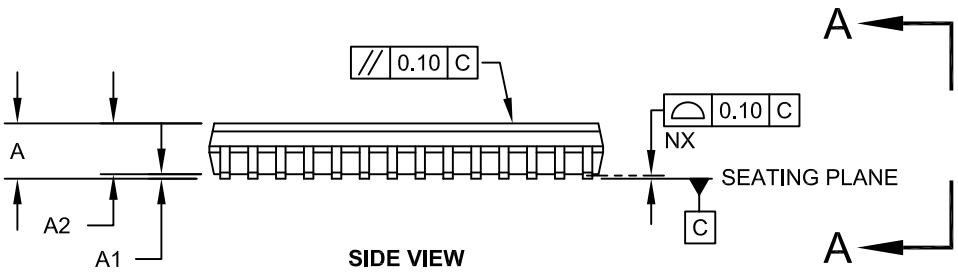


### 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

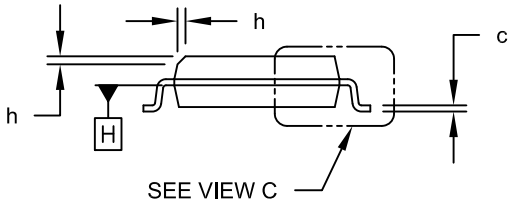
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW**




**SIDE VIEW**

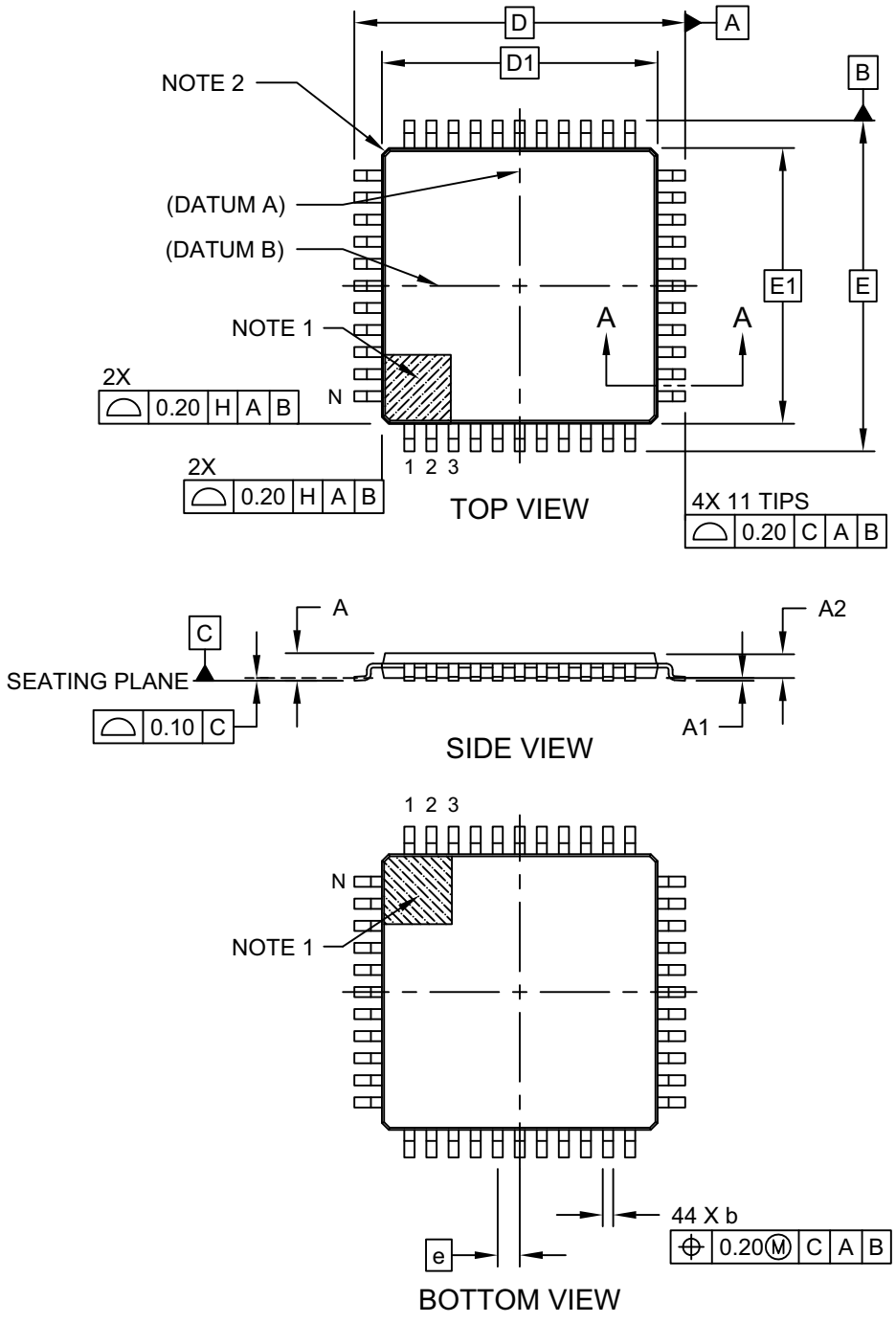



**VIEW A-A**

Microchip Technology Drawing C04-052C Sheet 1 of 2

### 44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-076C Sheet 1 of 2

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

| Features[1] | PIC18F23K22 PIC18LF23K22 | PIC18F24K22 PIC18LF24K22 | PIC18F25K22 PIC18LF25K22 | PIC18F26K22 PIC18LF26K22 | PIC18F43K22 PIC18LF43K22 | PIC18F44K22 PIC18LF44K22 | PIC18F45K22 PIC18LF45K22 | PIC18F46K22 PIC18LF46K22 |
|---|---|---|---|---|---|---|---|---|
| Program Memory (Bytes) | 8192 | 16384 | 32768 | 65536 | 8192 | 16384 | 32768 | 65536 |
| SRAM (Bytes) | 512 | 768 | 1536 | 3896 | 512 | 768 | 1536 | 3896 |
| EEPROM (Bytes) | 256 | 256 | 256 | 1024 | 256 | 256 | 256 | 1024 |
| Interrupt Sources | 26 | 26 | 33 | 33 | 26 | 26 | 33 | 33 |
| I/O Ports | Ports A, B, C, (E) | Ports A, B, C, (E) | Ports A, B, C, (E) | Ports A, B, C, (E) | Ports A, B, C, D, E | Ports A, B, C, D, E | Ports A, B, C, D, E | Ports A, B, C, D, E |
| Capture/Compare/PWM Modules (CCP) | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Enhanced CCP Modules (ECCP) Full Bridge | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 |
| ECCP Module Half Bridge | 2 | 2 | 2 | 2 | 1 | 1 | 1 | 1 |
| 10-bit Analog-to-Digital Module | 17 input channels | 17 input channels | 17 input channels | 17 input channels | 28 input channels | 28 input channels | 28 input channels | 28 input channels |
| Packages | 28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN | 28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN | 28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN | 28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN | 40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN | 40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN | 40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN | 40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN |

**Note 1:** PIC18FXXK22: operating voltage, 2.3V-5.5V.

PIC18LFXXK22: operating voltage, 1.8V-3.6V.