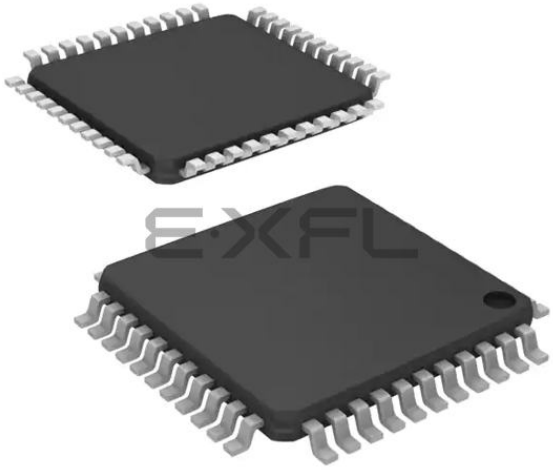

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 64MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 8KB (4K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 30x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f43k22-i-pt |

# 1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F23K22
- PIC18F24K22
- PIC18F25K22
- PIC18F26K22
- PIC18F43K22
- PIC18F44K22
- PIC18F45K22
- PIC18F46K22
- PIC18LF23K22
- PIC18LF24K22
- PIC18LF25K22
- PIC18LF26K22
- PIC18LF43K22
- PIC18LF44K22
- PIC18LF45K22
- PIC18LF46K22

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Flash program memory. On top of these features, the PIC18(L)F2X/4XK22 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

## 1.1 New Core Features

### 1.1.1 XLP TECHNOLOGY

All of the devices in the PIC18(L)F2X/4XK22 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 27.0 "Electrical Specifications"** for values.

### 1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18(L)F2X/4XK22 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O)
- Two External RC Oscillator modes with the same pin options as the External Clock modes
- An internal oscillator block which contains a 16 MHz HFINTOSC oscillator and a 31 kHz LFINTOSC oscillator, which together provide eight user selectable clock frequencies, from 31 kHz to 16 MHz. This option frees the two oscillator pins for use as additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both external and internal oscillator modes, which allows clock speeds of up to 64 MHz. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 64 MHz – all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the LFINTOSC. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or Wake-up from Sleep mode, until the primary clock source is available.

**TABLE 4-2: TIME-OUT IN VARIOUS SITUATIONS**

| Oscillator Configuration | Power-up[2] and Brown-out | | Exit from Power-Managed Mode |
|---|---|---|---|
| | $\overline{\text{PWRTEN}}$ = 0 | $\overline{\text{PWRTEN}}$ = 1 | |
| HSPLL | 66 ms[1] + 1024 TOSC + 2 ms[2] | 1024 TOSC + 2 ms[2] | 1024 TOSC + 2 ms[2] |
| HS, XT, LP | 66 ms[1] + 1024 TOSC | 1024 TOSC | 1024 TOSC |
| EC, ECIO | 66 ms[1] | — | — |
| RC, RCIO | 66 ms[1] | — | — |
| INTIO1, INTIO2 | 66 ms[1] | — | — |

**Note 1:** 66 ms (65.5 ms) is the nominal Power-up Timer (PWRT) delay.
**2:** 2 ms is the nominal time required for the PLL to lock.

**FIGURE 4-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO VDD, VDD RISE < TPWRT)**

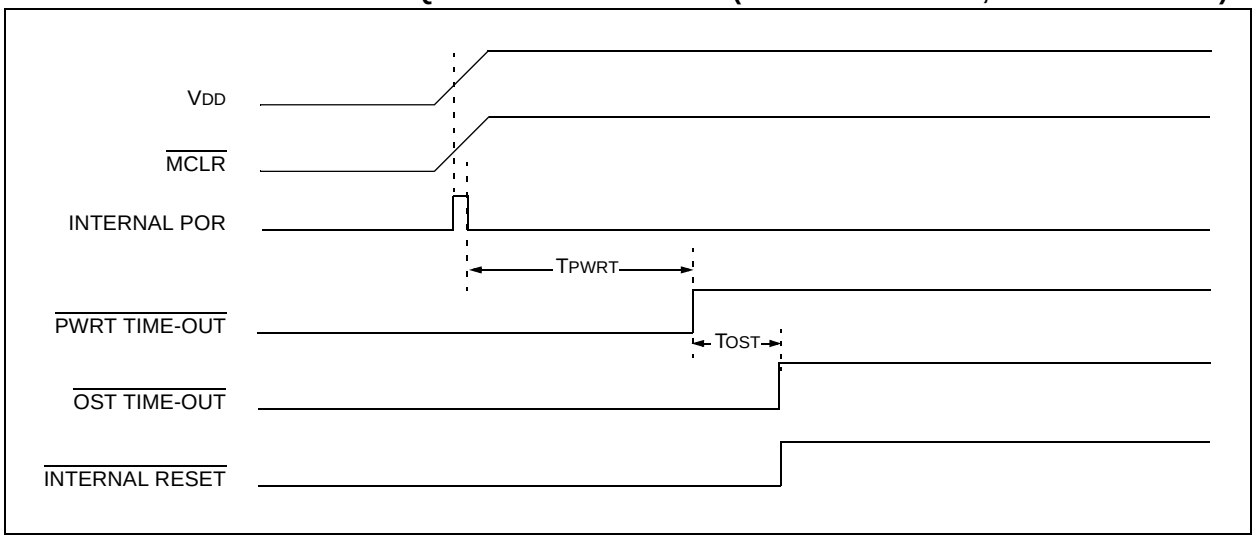
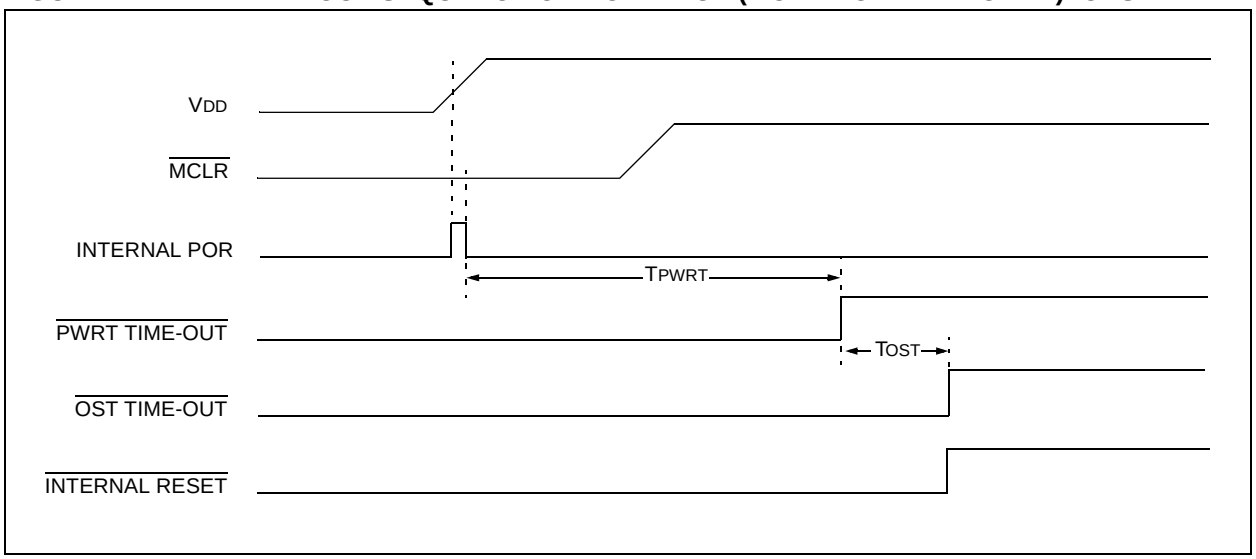



**FIGURE 4-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO VDD): CASE 1**



## 5.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 Enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate buses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 6.0 "Flash Program Memory"**. Data EEPROM is discussed separately in **Section 7.0 "Data EEPROM Memory"**.

### 5.1 Program Memory Organization

PIC18 microcontrollers implement a 21-bit program counter, which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

This family of devices contain the following:

- PIC18(L)F23K22, PIC18(L)F43K22: 8 Kbytes of Flash Memory, up to 4,096 single-word instructions
- PIC18(L)F24K22, PIC18(L)F44K22: 16 Kbytes of Flash Memory, up to 8,192 single-word instructions
- PIC18(L)F25K22, PIC18(L)F45K22: 32 Kbytes of Flash Memory, up to 16,384 single-word instructions
- PIC18(L)F26K22, PIC18(L)F46K22: 64 Kbytes of Flash Memory, up to 37,768 single-word instructions

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory map for PIC18(L)F2X/4XK22 devices is shown in Figure 5-1. Memory block details are shown in Figure 20-2.

**TABLE 5-2: REGISTER FILE SUMMARY FOR PIC18(L)F2X/4XK22 DEVICES (CONTINUED)**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR |
|---|---|---|---|---|---|---|---|---|---|---|
| FD1h | WDTCON | — | — | — | — | — | — | — | SWDTEN | ---- ---0 |
| FD0h | RCON | IPEN | SBOREN | — | $\overline{RI}$ | $\overline{TO}$ | $\overline{PD}$ | $\overline{POR}$ | $\overline{BOR}$ | 01-1 1100 |
| FCFh | TMR1H | Holding Register for the Most Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx |
| FCEh | TMR1L | Least Significant Byte of the 16-bit TMR1 Register | | | | | | | | xxxx xxxx |
| FCDh | T1CON | TMR1CS<1:0> | | T1CKPS<1:0> | | T1SOSCEN | $\overline{T1SYNC}$ | T1RD16 | TMR1ON | 0000 0000 |
| FCCh | T1GCON | TMR1GE | T1GPOL | T1GTM | T1GSPM | T1GGO/$\overline{DONE}$ | T1GVAL | T1GSS<1:0> | | 0000 xx00 |
| FCBh | SSP1CON3 | ACKTIM | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN | 0000 0000 |
| FCAh | SSP1MSK | SSP1 MASK Register bits | | | | | | | | 1111 1111 |
| FC9h | SSP1BUF | SSP1 Receive Buffer/Transmit Register | | | | | | | | xxxx xxxx |
| FC8h | SSP1ADD | SSP1 Address Register in $I^2C$ Slave Mode. SSP1 Baud Rate Reload Register in $I^2C$ Master Mode | | | | | | | | 0000 0000 |
| FC7h | SSP1STAT | SMP | CKE | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF | 0000 0000 |
| FC6h | SSP1CON1 | WCOL | SSPOV | SSPEN | CKP | SSPM<3:0> | | | | 0000 0000 |
| FC5h | SSP1CON2 | GCEN | ACKSTAT | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 0000 0000 |
| FC4h | ADRESH | A/D Result, High Byte | | | | | | | | xxxx xxxx |
| FC3h | ADRESL | A/D Result, Low Byte | | | | | | | | xxxx xxxx |
| FC2h | ADCON0 | — | CHS<4:0> | | | | | GO/$\overline{DONE}$ | ADON | --00 0000 |
| FC1h | ADCON1 | TRIGSEL | — | — | — | PVCFG<1:0> | | NVCFG<1:0> | | 0--- 0000 |
| FC0h | ADCON2 | ADFM | — | ACQT<2:0> | | | ADCS<2:0> | | | 0-00 0000 |
| FBFh | CCPR1H | Capture/Compare/PWM Register 1, High Byte | | | | | | | | xxxx xxxx |
| FBEh | CCPR1L | Capture/Compare/PWM Register 1, Low Byte | | | | | | | | xxxx xxxx |
| FBDh | CCP1CON | P1M<1:0> | | DC1B<1:0> | | CCP1M<3:0> | | | | 0000 0000 |
| FBCh | TMR2 | Timer2 Register | | | | | | | | 0000 0000 |
| FBBh | PR2 | Timer2 Period Register | | | | | | | | 1111 1111 |
| FBAh | T2CON | — | T2OUTPS<3:0> | | | | TMR2ON | T2CKPS<1:0> | | -000 0000 |
| FB9h | PSTR1CON | — | — | — | STR1SYNC | STR1D | STR1C | STR1B | STR1A | ---0 0001 |
| FB8h | BAUDCON1 | ABDOVF | RCIDL | DTRXP | CKTXP | BRG16 | — | WUE | ABDEN | 0100 0-00 |
| FB7h | PWM1CON | P1RSEN | P1DC<6:0> | | | | | | | 0000 0000 |
| FB6h | ECCP1AS | CCP1ASE | CCP1AS<2:0> | | | PSS1AC<1:0> | | PSS1BD<1:0> | | 0000 0000 |
| FB4h | T3GCON | TMR3GE | T3GPOL | T3GTM | T3GSPM | T3GGO/$\overline{DONE}$ | T3GVAL | T3GSS<1:0> | | 0000 0x00 |
| FB3h | TMR3H | Holding Register for the Most Significant Byte of the 16-bit TMR3 Register | | | | | | | | xxxx xxxx |
| FB2h | TMR3L | Least Significant Byte of the 16-bit TMR3 Register | | | | | | | | xxxx xxxx |
| FB1h | T3CON | TMR3CS<1:0> | | T3CKPS<1:0> | | T3SOSCEN | $\overline{T3SYNC}$ | T3RD16 | TMR3ON | 0000 0000 |
| FB0h | SPBRGH1 | EUSART1 Baud Rate Generator, High Byte | | | | | | | | 0000 0000 |
| FAFh | SPBRG1 | EUSART1 Baud Rate Generator, Low Byte | | | | | | | | 0000 0000 |
| FAEh | RCREG1 | EUSART1 Receive Register | | | | | | | | 0000 0000 |
| FADh | TXREG1 | EUSART1 Transmit Register | | | | | | | | 0000 0000 |
| FACh | TXSTA1 | CSRC | TX9 | TXEN | SYNC | SENDB | BRGH | TRMT | TX9D | 0000 0010 |
| FABh | RCSTA1 | SPEN | RX9 | SREN | CREN | ADDEN | FERR | OERR | RX9D | 0000 000x |
| FAAh | EEADRH(5) | — | — | — | — | — | — | EEADR<9:8> | | ---- --00 |
| FA9h | EEADR | EEADR<7:0> | | | | | | | | 0000 0000 |
| FA8h | EEDATA | EEPROM Data Register | | | | | | | | 0000 0000 |
| FA7h | EECON2 | EEPROM Control Register 2 (not a physical register) | | | | | | | | ---- --00 |
| FA6h | EECON1 | EEPGD | CFGS | — | FREE | WRERR | WREN | WR | RD | xx-0 x000 |
| FA5h | IPR3 | SSP2IP | BCL2IP | RC2IP | TX2IP | CTMUIP | TMR5GIP | TMR3GIP | TMR1GIP | 0000 0000 |
| FA4h | PIR3 | SSP2IF | BCL2IF | RC2IF | TX2IF | CTMUIF | TMR5GIF | TMR3GIF | TMR1GIF | 0000 0000 |
| FA3h | PIE3 | SSP2IE | BCL2IE | RC2IE | TX2IE | CTMUIE | TMR5GIE | TMR3GIE | TMR1GIE | 0000 0000 |

**Legend:** x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

**Note 1:** PIC18(L)F4XK22 devices only.
**2:** PIC18(L)F2XK22 devices only.
**3:** PIC18(L)F23/24K22 and PIC18(L)F43/44K22 devices only.
**4:** PIC18(L)F26K22 and PIC18(L)F46K22 devices only.

**REGISTER 9-11: PIE3: PERIPHERAL INTERRUPT ENABLE (FLAG) REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSP2IE | BCL2IE | RC2IE | TX2IE | CTMUIE | TMR5GIE | TMR3GIE | TMR1GIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **SSP2IE:** Master Synchronous Serial Port 2 Interrupt Enable bit
1 = Enables the MSSP2 interrupt
0 = Disables the MSSP2 interrupt

bit 6 **BCL2IE:** Bus Collision Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 5 **RC2IE:** EUSART2 Receive Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 4 **TX2IE:** EUSART2 Transmit Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 3 **CTMUIE:** CTMU Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 2 **TMR5GIE:** TMR5 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 1 **TMR3GIE:** TMR3 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

bit 0 **TMR1GIE:** TMR1 Gate Interrupt Enable bit
1 = Enabled
0 = Disabled

**TABLE 10-8: PORTC I/O SUMMARY**

| Pin Name | Function | TRIS Setting | ANSEL setting | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| RC0/P2B/T3CKI/T3G/ T1CKI/SOSCO | RC0 | 0 | — | O | DIG | LATC<0> data output; not affected by analog input. |
| | | 1 | — | I | ST | PORTC<0> data input; disabled when analog input enabled. |
| | P2B(2) | 0 | — | O | DIG | Enhanced CCP2 PWM output 2. |
| | T3CKI(1) | 1 | — | I | ST | Timer3 clock input. |
| | T3G | 1 | — | I | ST | Timer3 external clock gate input. |
| | T1CKI | 1 | — | I | ST | Timer1 clock input. |
| | SOSCO | x | — | O | XTAL | Secondary oscillator output. |
| RC1/P2A/CCP2/SOSCI | RC1 | 0 | — | O | DIG | LATC<1> data output; not affected by analog input. |
| | | 1 | — | I | ST | PORTC<1> data input; disabled when analog input enabled. |
| | P2A | 0 | — | O | DIG | Enhanced CCP2 PWM output 1. |
| | CCP2(1) | 0 | — | O | DIG | Compare 2 output/PWM 2 output. |
| | | 1 | — | I | ST | Capture 2 input. |
| | SOSCI | x | — | I | XTAL | Secondary oscillator input. |
| RC2/CTPLS/P1A/ CCP1/T5CKI/AN14 | RC2 | 0 | 0 | O | DIG | LATC<2> data output; not affected by analog input. |
| | | 1 | 0 | I | ST | PORTC<2> data input; disabled when analog input enabled. |
| | CTPLS | 0 | 0 | O | DIG | CTMU pulse generator output. |
| | P1A | 0 | 0 | O | DIG | Enhanced CCP1 PWM output 1. |
| | CCP1 | 0 | 0 | O | DIG | Compare 1 output/PWM 1 output. |
| | | 1 | 0 | I | ST | Capture 1 input. |
| | T5CKI | 1 | 0 | I | ST | Timer5 clock input. |
| | AN14 | 1 | 1 | I | AN | Analog input 14. |
| RC3/SCK1/SCL1/AN15 | RC3 | 0 | 0 | O | DIG | LATC<3> data output; not affected by analog input. |
| | | 1 | 0 | I | ST | PORTC<3> data input; disabled when analog input enabled. |
| | SCK1 | 0 | 0 | O | DIG | MSSP1 SPI Clock output. |
| | | 1 | 0 | I | ST | MSSP1 SPI Clock input. |
| | SCL1 | 0 | 0 | O | DIG | MSSP1 $I^2C$ Clock output. |
| | | 1 | 0 | I | $I^2C$ | MSSP1 $I^2C$ Clock input. |
| | AN15 | 1 | 1 | I | AN | Analog input 15. |
| RC4/SDI1/SDA1/AN16 | RC4 | 0 | 0 | O | DIG | LATC<4> data output; not affected by analog input. |
| | | 1 | 0 | I | ST | PORTC<4> data input; disabled when analog input enabled. |
| | SDI1 | 1 | 0 | I | ST | MSSP1 SPI data input. |
| | SDA1 | 0 | 0 | O | DIG | MSSP1 $I^2C$ data output. |
| | | 1 | 0 | I | $I^2C$ | MSSP1 $I^2C$ data input. |
| | AN16 | 1 | 1 | I | AN | Analog input 16. |

**Legend:** AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; $I^2C$ = Schmitt Trigger input with $I^2C$.

**Note 1:** Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

**2:** Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

**3:** Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

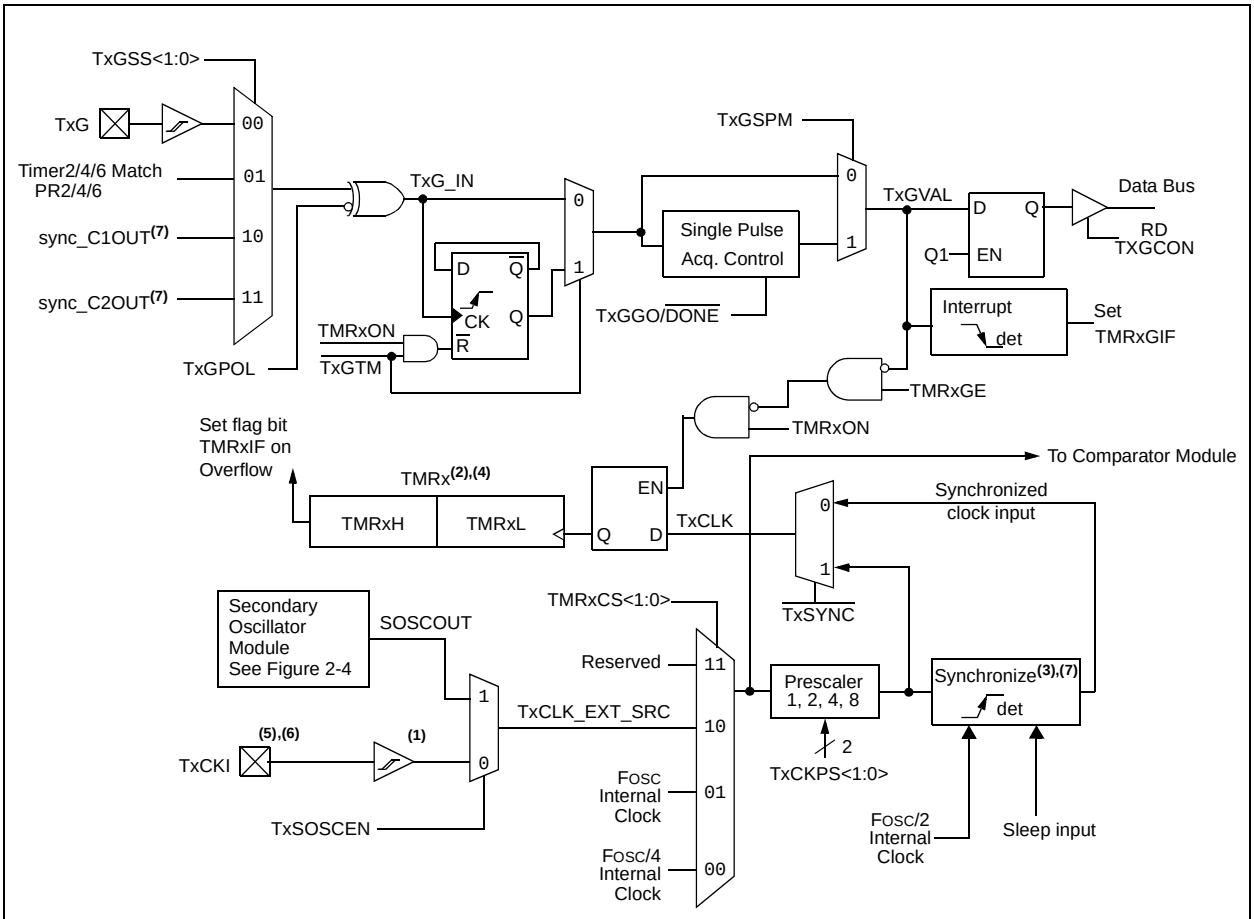
## 12.0 TIMER1/3/5 MODULE WITH GATE CONTROL

The Timer1/3/5 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMRxH:TMRxL)
- Programmable internal or external clock source
- 2-bit prescaler
- Dedicated Secondary 32 kHz oscillator circuit
- Optionally synchronized comparator out
- Multiple Timer1/3/5 gate (count enable) sources
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- 16-Bit Read/Write Operation
- Time base for the Capture/Compare function
- Special Event Trigger (with CCP/ECCP)
- Selectable Gate Source Polarity
- Gate Toggle mode
- Gate Single-pulse mode
- Gate Value Status
- Gate Event Interrupt

Figure 12-1 is a block diagram of the Timer1/3/5 module.

**FIGURE 12-1: TIMER1/3/5 BLOCK DIAGRAM**




**Note 1:** ST Buffer is high speed type when using TxCKI.

**2:** Timer1/3/5 register increments on rising edge.

**3:** Synchronize does not operate while in Sleep.

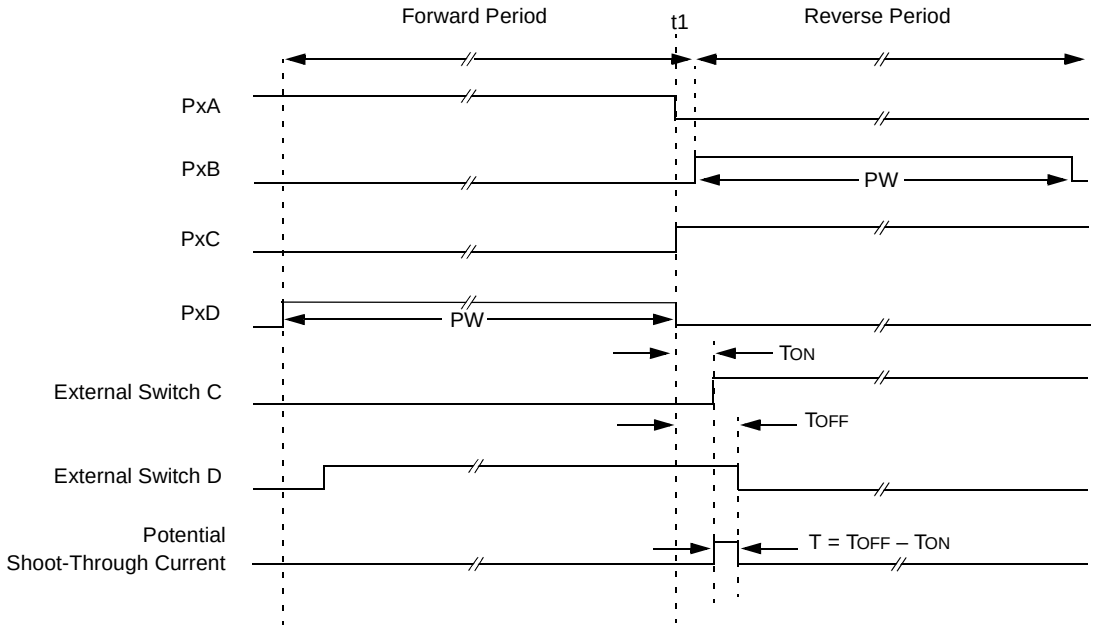
**4:** See Figure 12-2 for 16-Bit Read/Write Mode Block Diagram.

**5:** T1CKI is not available when the secondary oscillator is enabled. (SOSCGO = 1 or TXSOSCEN = 1)

**6:** T3CKI is not available when the secondary oscillator is enabled, unless T3CMX = 1.

**7:** Synchronized comparator output should not be used in conjunction with synchronized TxCKI.

**FIGURE 14-13: EXAMPLE OF PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE**




**Note 1:** All signals are shown as active-high.

**2:** TON is the turn-on delay of power switch QC and its driver.

**3:** TOFF is the turn-off delay of power switch QD and its driver.

### 14.4.3 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the CCPxAS<2:0> bits of the ECCPxAS register. A shutdown event may be generated by:

- A logic '0' on the INT pin
- Comparator Cx (async_CxOUT)
- Setting the CCPxASE bit in firmware

A shutdown condition is indicated by the CCPxASE (Auto-Shutdown Event Status) bit of the ECCPxAS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The CCPxASE bit is set to '1'. The CCPxASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 14.4.4 "Auto-Restart Mode"**).

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [PxA/PxC] and [PxB/PxD].

The state of each pin pair is determined by the PSSxAC<1:0> and PSSxBD<1:0> bits of the ECCPxAS register. Each pin pair may be placed into one of three states:

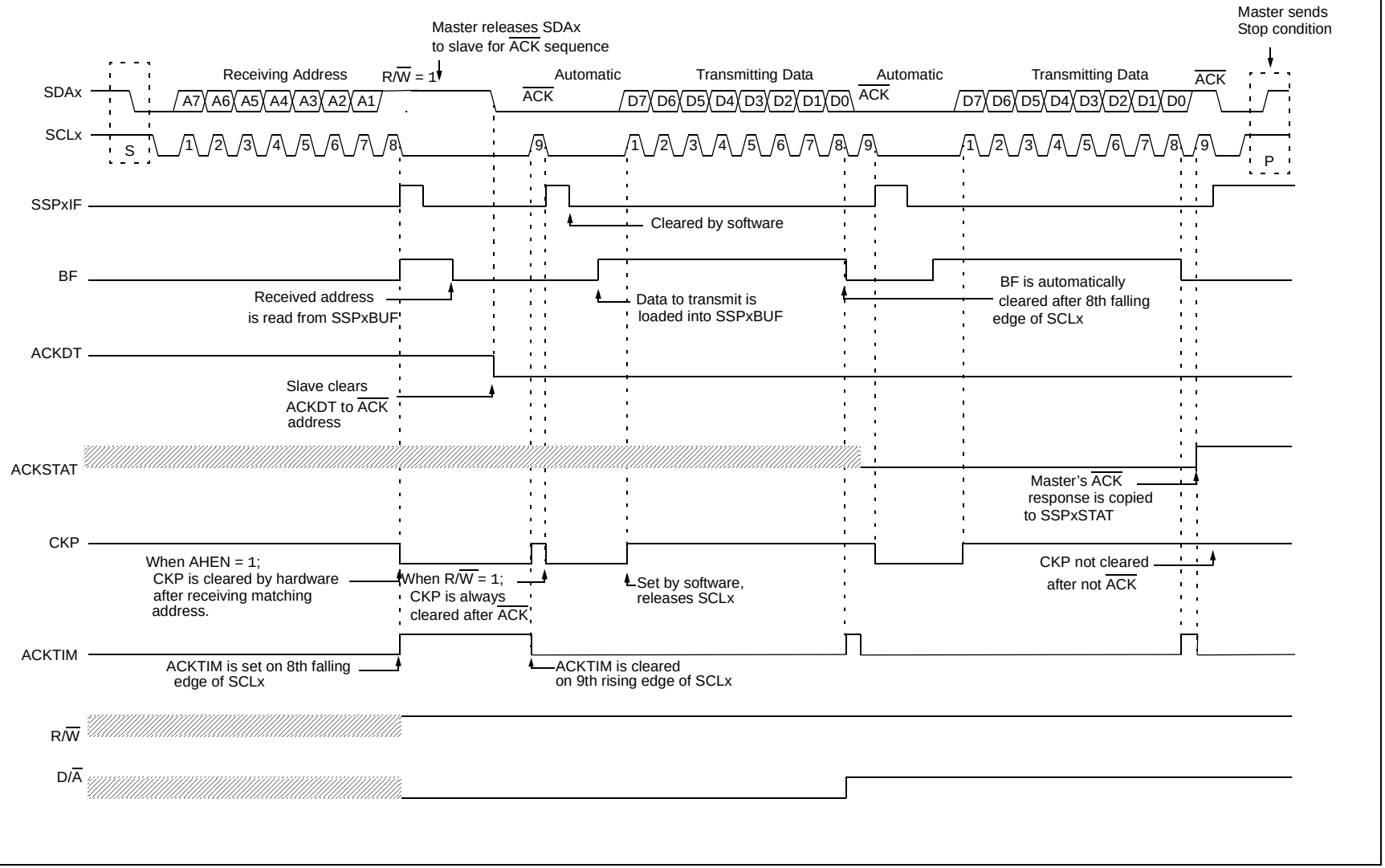
- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

**Note 1:** The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

**2:** Writing to the CCPxASE bit is disabled while an auto-shutdown condition persists.

**3:** Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

**FIGURE 15-19: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)**



### 15.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN, of the SSPxCON2 register. When this bit is set, the SCLx pin is pulled low and the contents of the Acknowledge data bit are presented on the SDAx pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCLx pin is deasserted (pulled high). When the SCLx pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCLx pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSPx module then goes into Idle mode (Figure 15-30).

#### 15.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

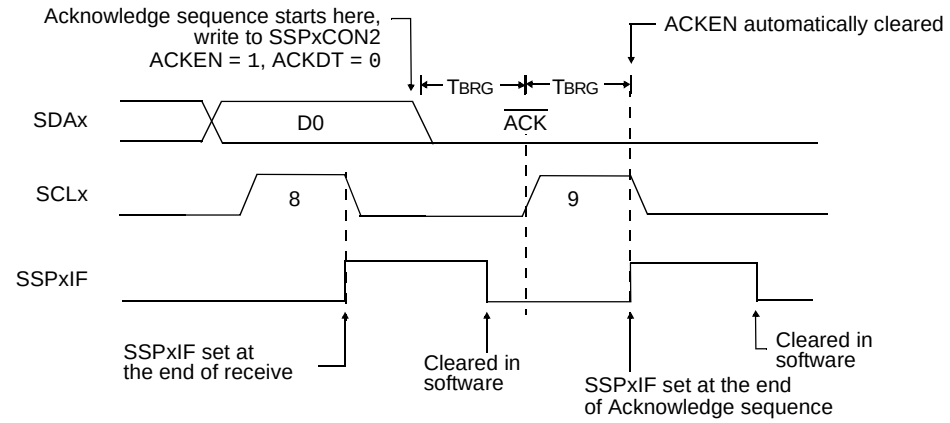
### 15.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDAx pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN, of the SSPxCON2 register. At the end of a receive/transmit, the SCLx line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDAx line low. When the SDAx line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCLx pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDAx pin will be deasserted. When the SDAx pin is sampled high while SCLx is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 15-31).

#### 15.6.9.1 WCOL Status Flag

If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

**FIGURE 15-30: ACKNOWLEDGE SEQUENCE WAVEFORM**




**Note:** TBRG = one Baud Rate Generator period.

#### 15.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDAx pin has been deasserted and allowed to float high, SDAx is sampled low after the BRG has timed out (Case 1).

b) After the SCLx pin is deasserted, SCLx is sampled low before SDAx goes high (Case 2).

The Stop condition begins with SDAx asserted low. When SDAx is sampled low, the SCLx pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD and counts down to zero. After the BRG times out, SDAx is sampled. If SDAx is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 15-38). If the SCLx pin is sampled low before SDAx is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 15-39).

**FIGURE 15-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)**

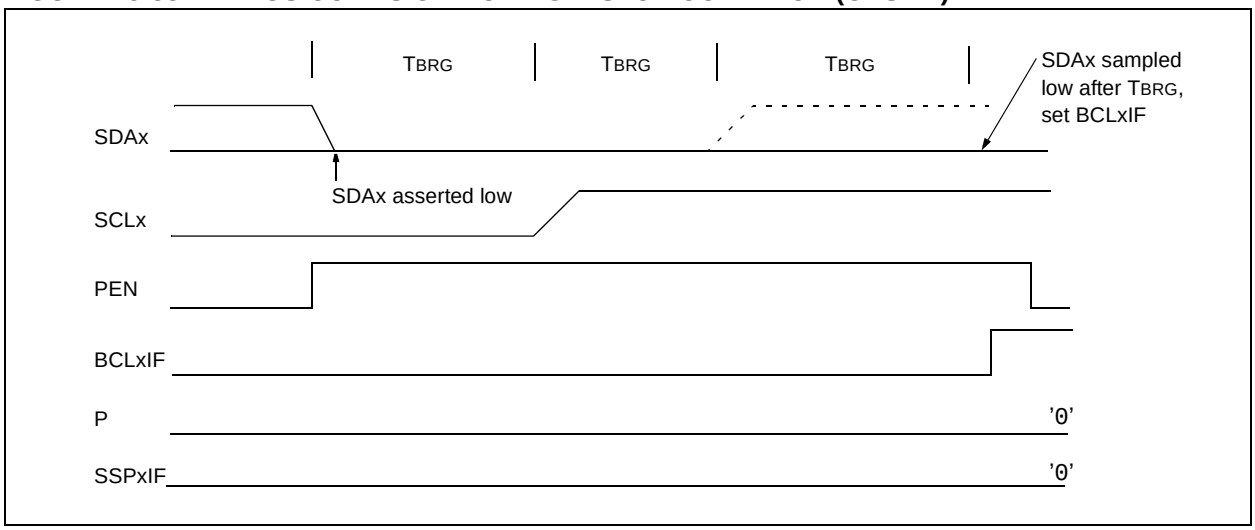
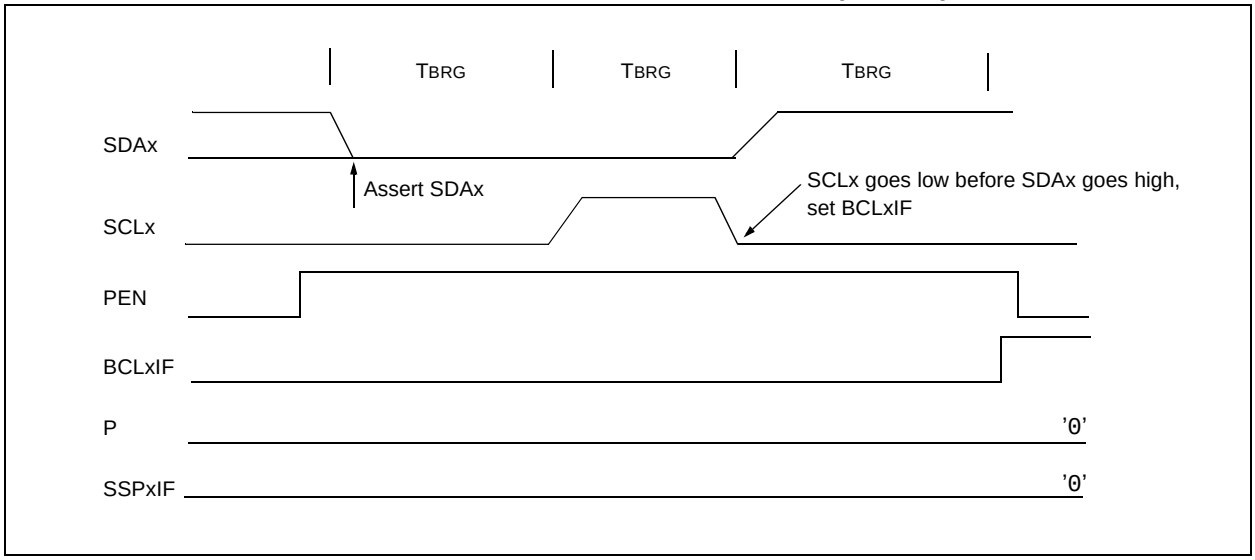



**FIGURE 15-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)**



## 16.3 Register Definitions: EUSART Control

### REGISTER 16-1: TxSTAx: TRANSMIT STATUS AND CONTROL REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-1 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSRC | TX9 | TXEN(1) | SYNC | SENDB | BRGH | TRMT | TX9D |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

**Note 1:** SREN/CREN overrides TXEN in Sync mode.

## 18.2 Comparator Control

Each comparator has a separate control and Configuration register: CM1CON0 for Comparator C1 and CM2CON0 for Comparator C2. In addition, Comparator C2 has a second control register, CM2CON1, for controlling the interaction with Timer1 and simultaneous reading of both comparator outputs.

The CM1CON0 and CM2CON0 registers (see Register 18-1) contain the control and status bits for the following:

- Enable
- Input selection
- Reference selection
- Output selection
- Output polarity
- Speed selection

### 18.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

### 18.2.2 COMPARATOR INPUT SELECTION

The CxCH<1:0> bits of the CMxCON0 register direct one of four analog input pins to the comparator inverting input.

| | |
|---|---|
| **Note:** | To use CxIN+ and C12INx- pins as analog inputs, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers. |

### 18.2.3 COMPARATOR REFERENCE SELECTION

Setting the CxR bit of the CMxCON0 register directs an internal voltage reference or an analog input pin to the non-inverting input of the comparator. See **Section 21.0 "Fixed Voltage Reference (FVR)"** for more information on the Internal Voltage Reference module.

### 18.2.4 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CM2CON1 register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CxON bit of the CMxCON0 register must be set

| | |
|---|---|
| **Note 1:** | The CxOE bit overrides the PORT data latch. Setting the CxON has no impact on the port override. |
| **2:** | The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched. |

### 18.2.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 18-1 shows the output state versus input conditions, including polarity control.

**TABLE 18-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS**

| Input Condition | CxPOL | CxOUT |
|---|---|---|
| CxVIN- > CxVIN+ | 0 | 0 |
| CxVIN- < CxVIN+ | 0 | 1 |
| CxVIN- > CxVIN+ | 1 | 1 |
| CxVIN- < CxVIN+ | 1 | 0 |

### 18.2.6 COMPARATOR SPEED SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the normal speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

## 18.3 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 27.0 "Electrical Specifications"** for more details.

**CPFSGT** **Compare f with W, skip if f > W**

Syntax: CPFSGT f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: (f) – (W),
skip if (f) > (W)
(unsigned comparison)

Status Affected: None

Encoding:

| 0110 | 010a | ffff | ffff |
|---|---|---|---|

Description: Compares the contents of data memory location 'f' to the contents of the W by performing an unsigned subtraction.
If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.
If 'a' is '0', the Access Bank is selected.
If 'a' is '1', the BSR is used to select the GPR bank.
If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1(2)
**Note:** 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process Data | No operation |

If skip:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| No operation | No operation | No operation | No operation |

If skip and followed by 2-word instruction:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| No operation | No operation | No operation | No operation |
| No operation | No operation | No operation | No operation |

Example:
```
HERE      CPFSGT REG, 0
NGREATER  :
GREATER   :
```

Before Instruction
PC = Address (HERE)
W = ?
After Instruction
If REG > W;
PC = Address (GREATER)
If REG ≤ W;
PC = Address (NGREATER)

**CPFSLT** **Compare f with W, skip if f < W**

Syntax: CPFSLT f {,a}

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: (f) – (W),
skip if (f) < (W)
(unsigned comparison)

Status Affected: None

Encoding:

| 0110 | 000a | ffff | ffff |
|---|---|---|---|

Description: Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction.
If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.
If 'a' is '0', the Access Bank is selected.
If 'a' is '1', the BSR is used to select the GPR bank.

Words: 1

Cycles: 1(2)
**Note:** 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| Decode | Read register 'f' | Process Data | No operation |

If skip:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| No operation | No operation | No operation | No operation |

If skip and followed by 2-word instruction:

| Q1 | Q2 | Q3 | Q4 |
|---|---|---|---|
| No operation | No operation | No operation | No operation |
| No operation | No operation | No operation | No operation |

Example:
```
HERE    CPFSLT REG, 1
NLESS   :
LESS    :
```

Before Instruction
PC = Address (HERE)
W = ?
After Instruction
If REG < W;
PC = Address (LESS)
If REG ≥ W;
PC = Address (NLESS)

**TABLE 27-13: CAPTURE/COMPARE/PWM REQUIREMENTS (ALL CCP MODULES)**

| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 50 | TccL | CCPx Input Low Time | No prescaler | 0.5 TCY + 20 | — | ns | |
| | | | With prescaler | 10 | — | ns | |
| 51 | TccH | CCPx Input High Time | No prescaler | 0.5 TCY + 20 | — | ns | |
| | | | With prescaler | 10 | — | ns | |
| 52 | TccP | CCPx Input Period | | $\frac{3\ T_{CY} + 40}{N}$ | — | ns | N = prescale value (1, 4 or 16) |
| 53 | TccR | CCPx Output Fall Time | | — | 25 | ns | |
| 54 | TccF | CCPx Output Fall Time | | — | 25 | ns | |

**TABLE 27-16: I²C BUS DATA REQUIREMENTS (SLAVE MODE)**

| Param. No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 100 | THIGH | Clock High Time | 100 kHz mode | 4.0 | — | µs | Must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | µs | Must operate at a minimum of 10 MHz |
| | | | SSP Module | 1.5 TCY | — | | |
| 101 | TLOW | Clock Low Time | 100 kHz mode | 4.7 | — | µs | Must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 1.3 | — | µs | Must operate at a minimum of 10 MHz |
| | | | SSP Module | 1.5 TCY | — | | |
| 102 | TR | SDA and SCL Rise Time | 100 kHz mode | — | 1000 | ns | |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | CB is specified to be from 10 to 400 pF |
| 103 | TF | SDA and SCL Fall Time | 100 kHz mode | — | 300 | ns | |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | CB is specified to be from 10 to 400 pF |
| 90 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4.7 | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 91 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4.0 | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 106 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| 107 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | **(Note 2)** |
| | | | 400 kHz mode | 100 | — | ns | |
| 92 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| 109 | TAA | Output Valid from Clock | 100 kHz mode | — | 3500 | ns | **(Note 1)** |
| | | | 400 kHz mode | — | — | ns | |
| 110 | TBUF | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| D102 | CB | Bus Capacitive Loading | | — | 400 | pF | |

**Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**2:** A fast mode I²C bus device can be used in a standard mode I²C bus system but the requirement, TSU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line, TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification), before the SCL line is released.

**FIGURE 28-7: PIC18LF2X/4XK22 DELTA IPD HIGH/LOW-VOLTAGE DETECT (HLVD)**

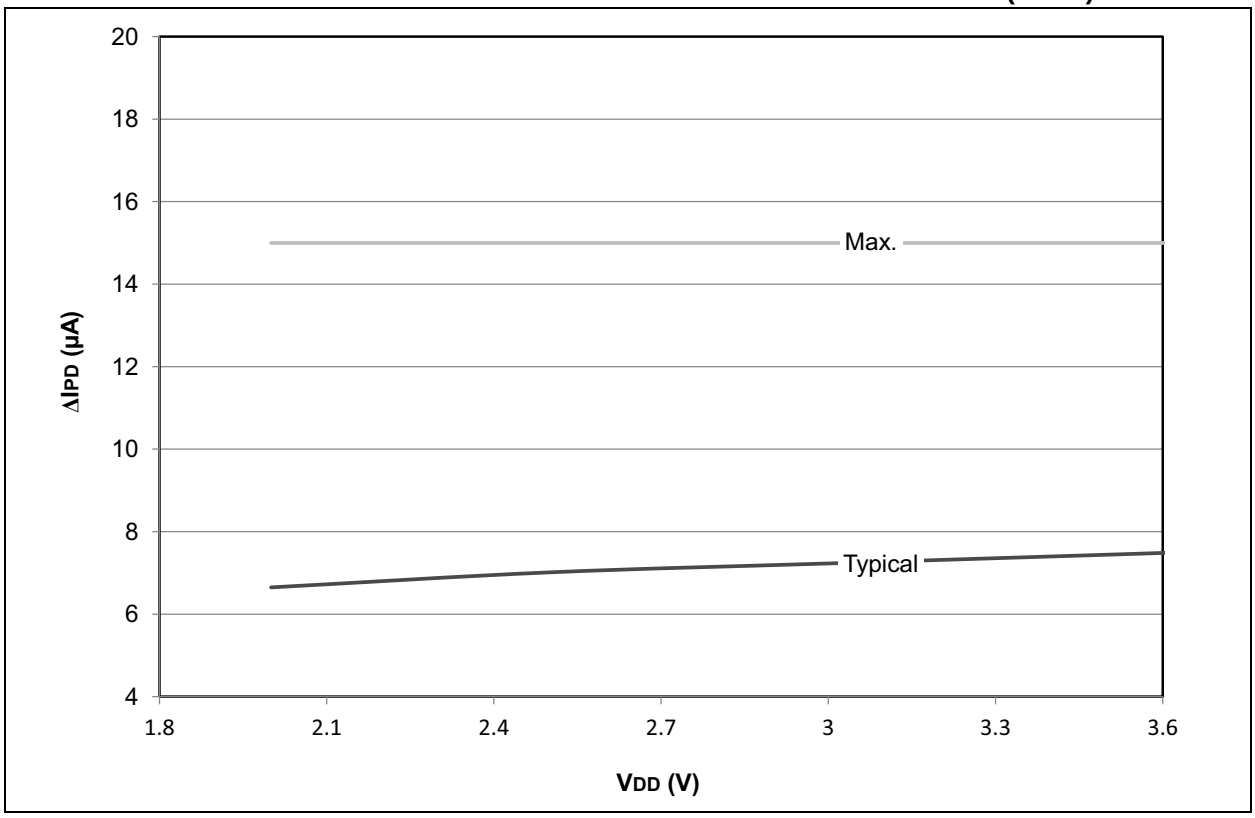



**FIGURE 28-8: PIC18F2X/4XK22 DELTA IPD HIGH/LOW-VOLTAGE DETECT (HLVD)**

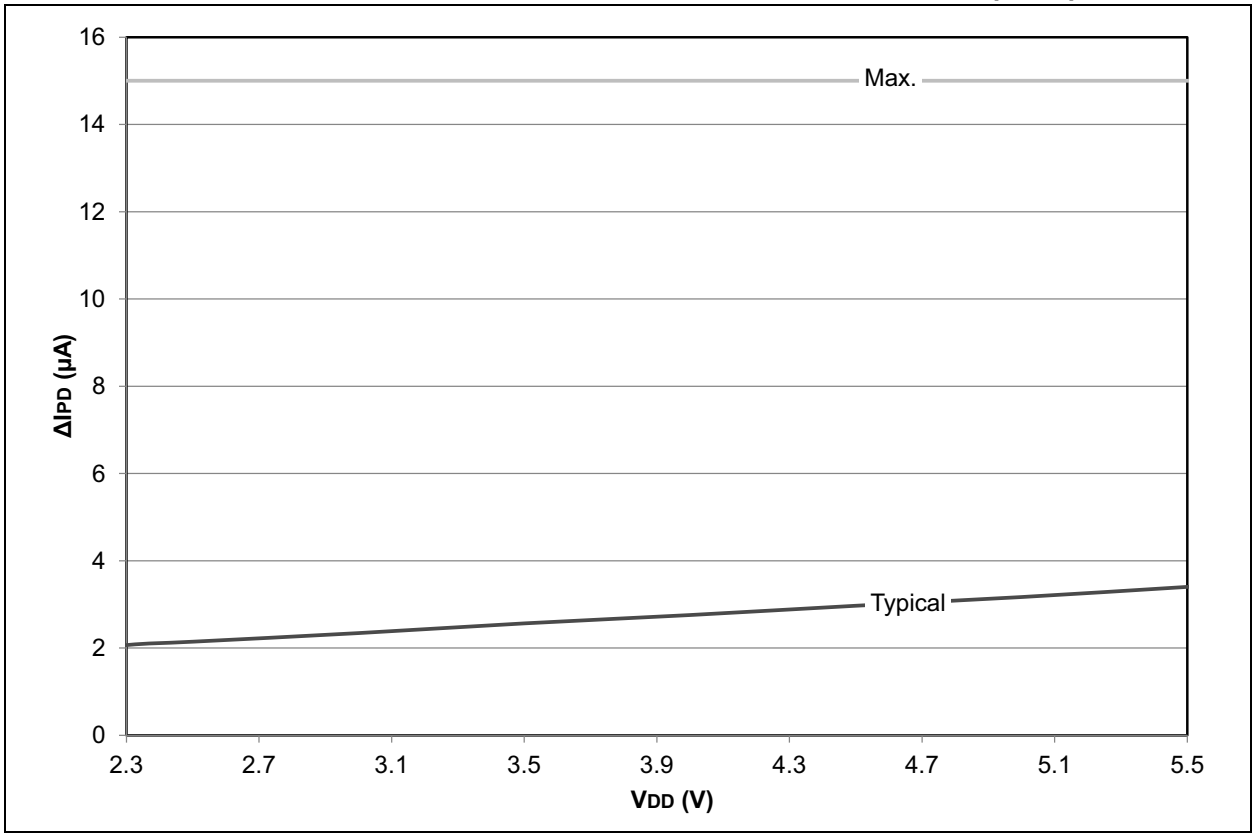


**FIGURE 28-20: PIC18LF2X/4XK22 TYPICAL IDD: RC_RUN LF-INTOSC 31 kHz**

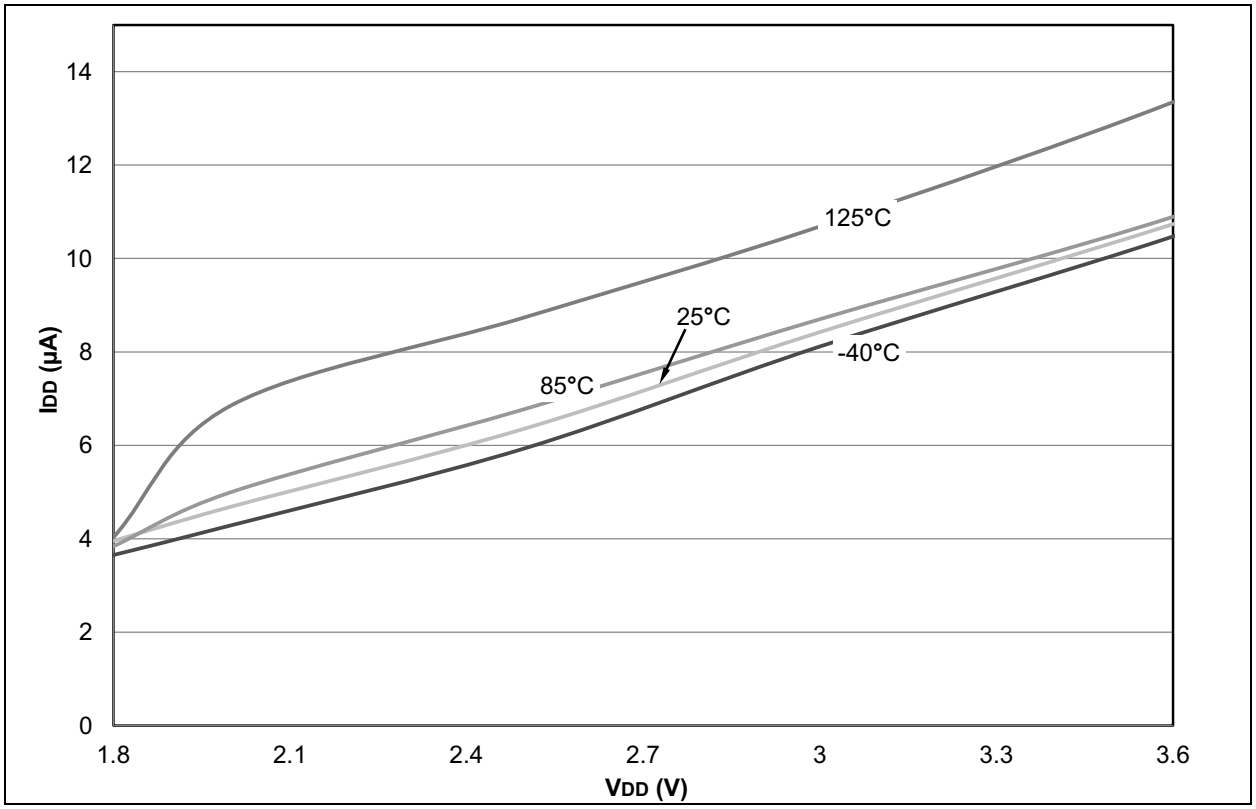



**FIGURE 28-21: PIC18LF2X/4XK22 MAXIMUM IDD: RC_RUN LF-INTOSC 31 kHz**

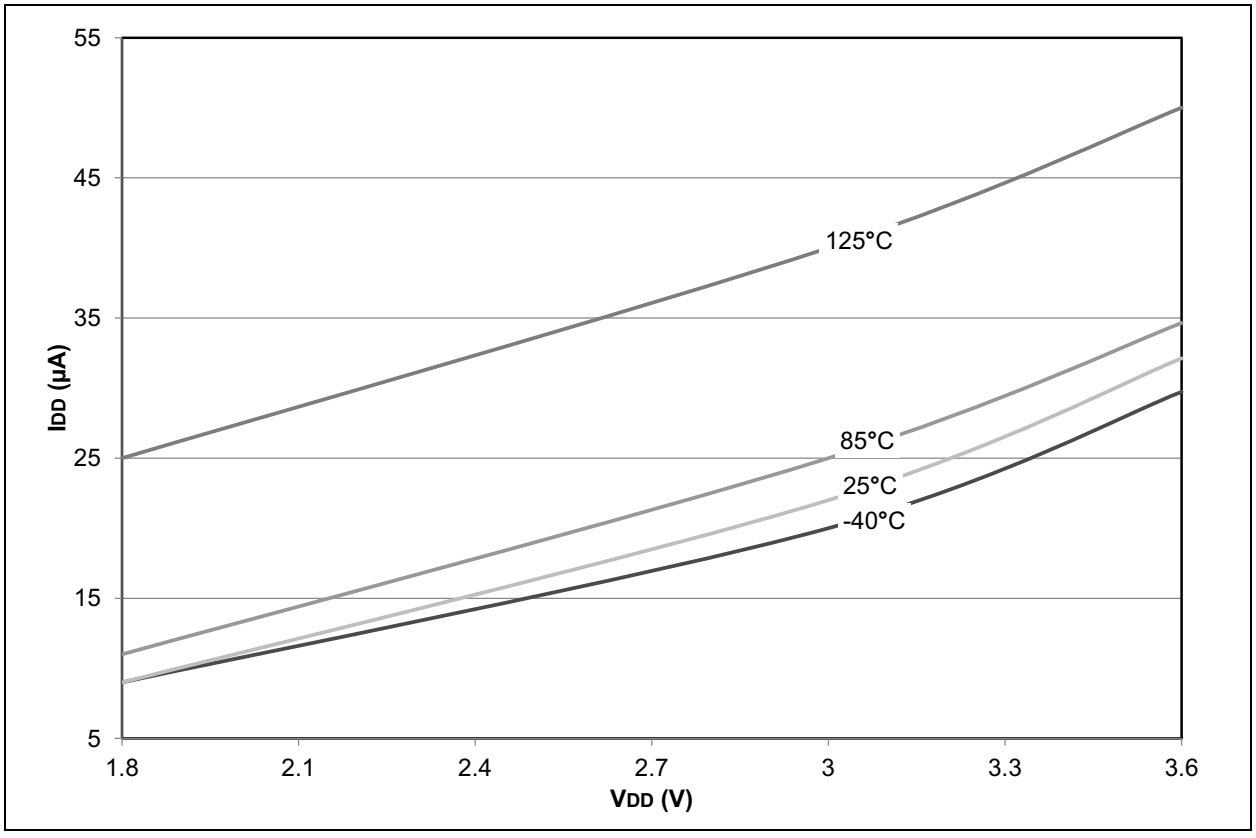


**FIGURE 28-72: PIC18LF2X/4XK22 TYPICAL IDD: SEC_RUN 32.768 kHz**

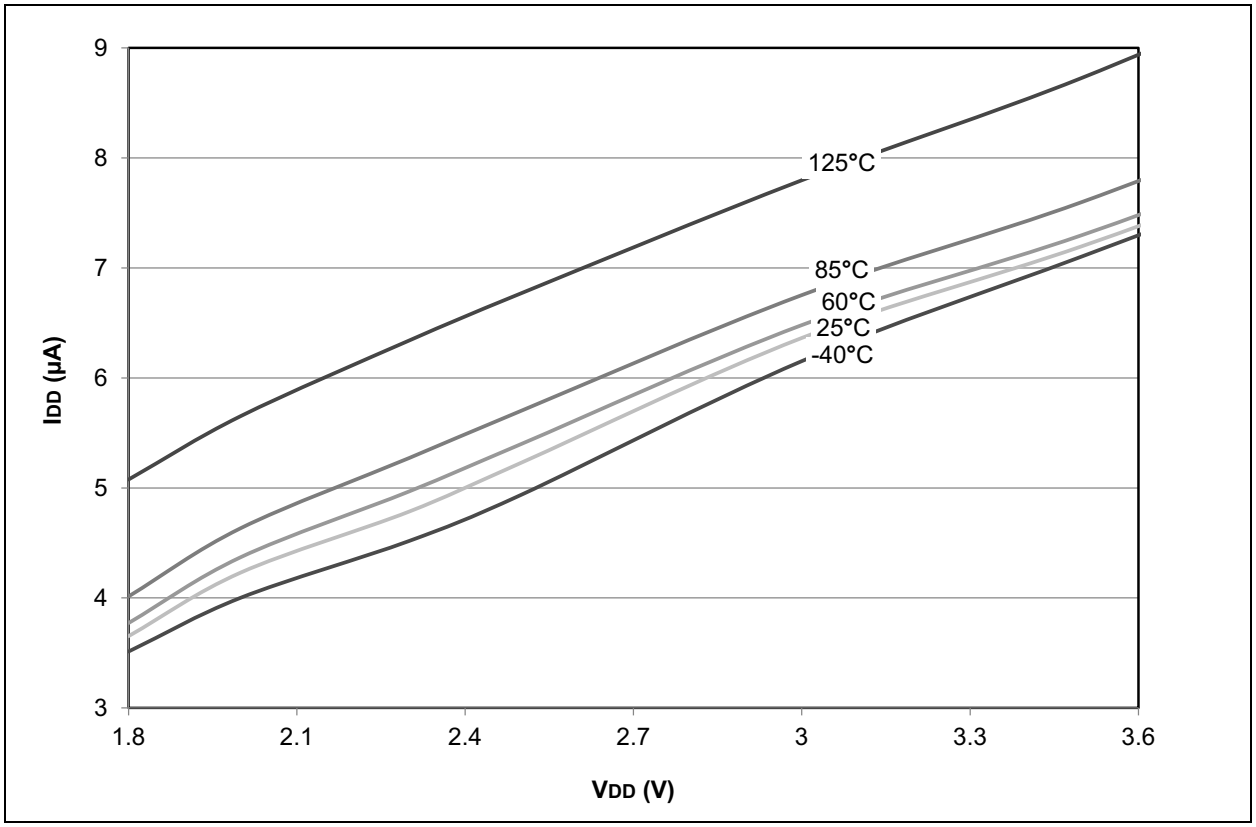
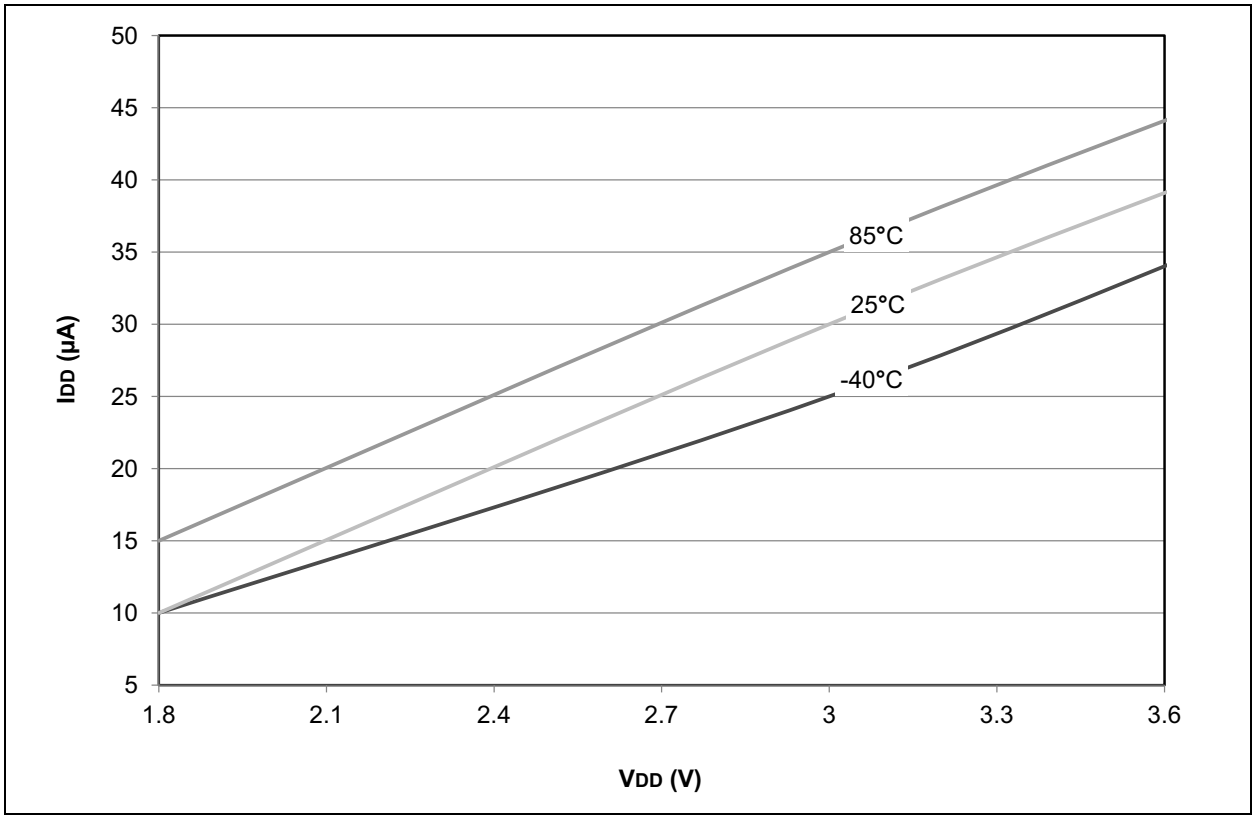
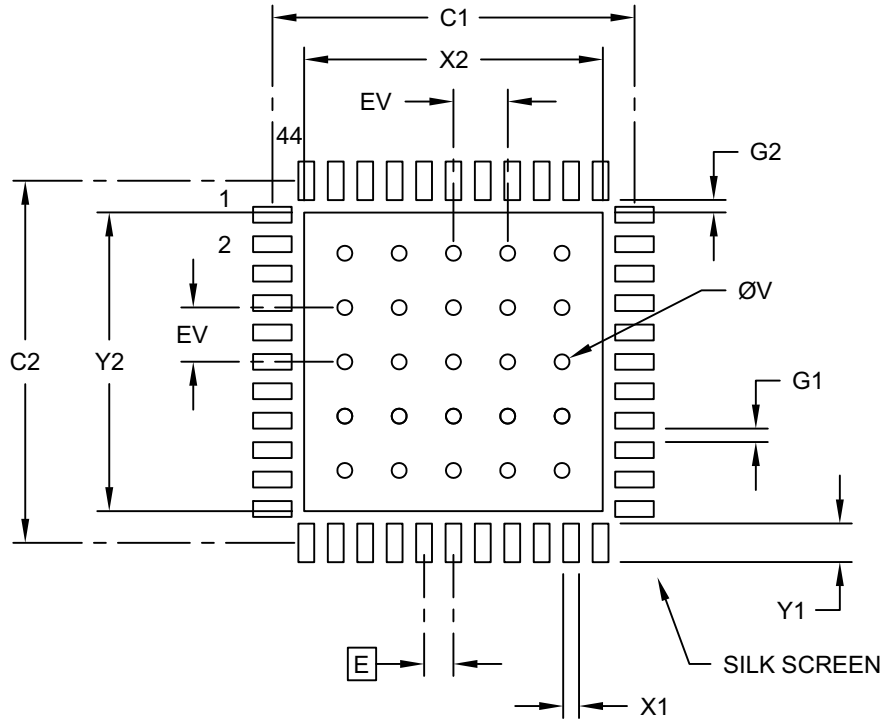



**FIGURE 28-73: PIC18LF2X/4XK22 MAXIMUM IDD: SEC_RUN 32.768 kHz**



### 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | X2 | | | 6.60 |
| Optional Center Pad Length | Y2 | | | 6.60 |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Width (X44) | X1 | | | 0.35 |
| Contact Pad Length (X44) | Y1 | | | 0.85 |
| Contact Pad to Contact Pad (X40) | G1 | 0.30 | | |
| Contact Pad to Center Pad (X44) | G2 | 0.28 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2103C