

Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 30x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f45k22-e-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

R-0/0	R-0/q	U-0	R/W-0/0	R/W-0/u	R/W-1/1	R-x/u	R-0/0
PLLRDY	SOSCRUN	_	MFIOSEL	SOSCGO <sup>(1)</sup>	PRISD	MFIOFS	LFIOFS
bit 7							bit 0
Legend:							
R = Readable	bit W = W	/ritable bit	U = Unimple	emented bit, rea	ıd as '0' q	= depends on	condition
'1' = Bit is set	'0' = B	it is cleared	x = Bit is un	known			
-n/n = Value at	t POR and BOR	Value at all oth	ner Resets				
bit 7	PLLRDY: PLL	Run Status bit					
	1 = System clo	ock comes fror	n 4xPLL	other then 4vD			
hit 6		CK COMES NO	n an Uscillator,		LL		
bit o	1 - System cl	ock comes from	n secondary S	090			
	0 = System clo	ock comes from	n an oscillator,	other than SO	SC		
bit 5	Unimplemente	ed: Read as '0					
bit 4	MFIOSEL: MF	INTOSC Selec	t bit				
	1 = MFINTOS	C is used in pla	ace of HFINTC	OSC frequencie	s of 500 kHz, 2	250 kHz and 31	l.25 kHz
bit 3		econdary Osc	illator Start Co	ntrol bit			
Sito	1 = Secondary	/ oscillator is e	nabled.				
	0 = Secondary	oscillator is s	hut off if no oth	ner sources are	requesting it.		
bit 2	PRISD: Primar	y Oscillator Dr	ive Circuit Shu	utdown bit			
	1 = Oscillator	drive circuit on					
1.11.4	0 = Oscillator	drive circuit off	(zero power)				
Dit 1		110SC Freque	ency Stable bit				
	1 = MFINTOS 0 = MFINTOS	C is stable C is not stable					
bit 0	LFIOFS: LFIN	TOSC Frequer	ncv Stable bit				
	1 = LFINTOS	C is stable	.,				
	0 = LFINTOSO	C is not stable					
Note 1: The	e SOSCGO bit is	only reset on	a POR Reset.				

#### REGISTER 2-2: OSCCON2: OSCILLATOR CONTROL REGISTER 2

#### 2.6.1.1 OSCTUNE Register

The HFINTOSC/MFINTOSC oscillator circuits are factory calibrated but can be adjusted in software by writing to the TUN<5:0> bits of the OSCTUNE register (Register 2-3).

The default value of the TUN<5:0> is '000000'. The value is a 6-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC/MFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

The TUN<5:0> bits in OSCTUNE do not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

The OSCTUNE register also implements the INTSRC and PLLEN bits, which control certain features of the internal oscillator block.

The INTSRC bit allows users to select which internal oscillator provides the clock source when the 31.25 kHz frequency option is selected. This is covered in greater detail in **Section 2.2.3 "Low Frequency Selection"**.

The PLLEN bit controls the operation of the frequency multiplier, PLL, for all primary external clock sources and internal oscillator modes. However, the PLL is intended for operation with clock sources between 4 MHz and 16 MHz. For more details about the function of the PLLEN bit, see **Section 2.8.2 "PLL in HFIN-TOSC Modes"** 

## 2.7 Register Definitions: Oscillator Tuning

#### REGISTER 2-3: OSCTUNE: OSCILLATOR TUNING REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INTSRC	PLLEN <sup>(1)</sup>			TUN	<5:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7	INTSRC: Internal Oscillator Low-Frequency Source Select bit
	<ul> <li>1 = 31.25 kHz device clock derived from the MFINTOSC or HFINTOSC source</li> <li>0 = 31.25 kHz device clock derived directly from LFINTOSC internal oscillator</li> </ul>
bit 6	PLLEN: Frequency Multiplier 4xPLL for HFINTOSC Enable bit <sup>(1)</sup> 1 = PLL enabled 0 = PLL disabled
bit 5-0	<pre>TUN&lt;5:0&gt;: Frequency Tuning bits – use to adjust MFINTOSC and HFINTOSC frequencies 011111 = Maximum frequency 011110 =     ••• 000001 = 000000 = Oscillator module (HFINTOSC and MFINTOSC) are running at the factory calibrated     frequency. 111111 =     ••• 100000 = Minimum frequency</pre>

**Note 1:** The PLLEN bit is active for all the primary clock sources (internal or external) and is designed to operate with clock frequencies between 4 MHz and 16 MHz.

# 6.3 Register Definitions: Memory Control

# REGISTER 6-1: EECON1: DATA EEPROM CONTROL 1 REGISTER

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	_	FREE	WRERR	WREN	WR	RD
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit				
S = Bit can be	set by software	e, but not clear	ed	U = Unimpler	nented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
h:4 7					-4 h:4		
DIT 7	1 - Accoss E	n Program or L		i wemory Selec			
	1 = Access r 0 = Access d	ata EEPROM	memory				
bit 6	CFGS: Flash	Program/Data	EEPROM or (	Configuration S	elect bit		
	1 = Access C	configuration re	gisters	-			
	0 = Access F	lash program	or data EEPRO	OM memory			
bit 5	Unimplement	ted: Read as '	0'				
bit 4	FREE: Flash	Row (Block) E	rase Enable bi	t			
	1 = Erase the	e program men	nory block add	ressed by TBL	PIR on the ne	ext WR commar	ld
	0 = Perform  V	write-only					
bit 3	WRERR: Flas	sh Program/Da	ta EEPROM E	Error Flag bit <sup>(1)</sup>			
	1 = A write op	peration is prei	maturely termi	nated (any Res	et during self-	timed programr	ning in normal
	operation	, or an improp	er write attemp	ot)			
h it 0				ite Excelete bit			
DIT 2		Program/Data	EEPROM W				
	0 = Inhibits w	rite cycles to F	lash program/	data EEPROM			
bit 1	WR: Write Co	ntrol bit					
	1 = Initiates a	data EEPRON	/l erase/write c	ycle or a progra	am memory era	ase cycle or writ	e cycle.
	(The ope	ration is self-tir	ned and the bi	it is cleared by	hardware onc	e write is compl	ete.
	0 = Write cyc	le to the EEPF	Set (not cleare ROM is comple	ed) by soliware	.)		
bit 0	RD: Read Co	ntrol bit	·				
	1 = Initiates a	n EEPROM re	ad (Read takes	s one cycle. RD	is cleared by I	hardware. The F	RD bit can only
	be set (no	ot cleared) by s	oftware. RD bi	t cannot be set	when EEPGD	= 1 or CFGS =	1.)
	v = Does not	initiate an EEI	-KOW read				

# **Note 1:** When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.

# 14.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events, and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains three Enhanced Capture/Compare/PWM modules (ECCP1, ECCP2, and ECCP3) and two standard Capture/Compare/PWM modules (CCP4 and CCP5).

The Capture and Compare functions are identical for all CCP/ECCP modules. The difference between CCP and ECCP modules are in the Pulse-Width Modulation (PWM) function. In CCP modules, the standard PWM function is identical. In ECCP modules, the Enhanced PWM function has either full-bridge or half-bridge PWM output. Full-bridge ECCP modules have four available I/O pins while half-bridge ECCP modules and can be configured as standard PWM modules. See Table 14-1 to determine the CCP/ECCP functionality available on each device in this family.

- Note 1: In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.
  - 2: Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to ECCP1, ECCP2, ECCP3, CCP4 and CCP5. Register names, module signals, I/O pins, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

Device Name	ECCP1	ECCP2	ECCP3	CCP4	CCP5
PIC18(L)F23K22 PIC18(L)F24K22 PIC18(L)F25K22 PIC18(L)F25K22 PIC18(L)F26K22	Enhanced PWM Full-Bridge	Enhanced PWM Half-Bridge	Enhanced PWM Half-Bridge	Standard PWM	Standard PWM (Special Event Trigger)
PIC18(L)F43K22 PIC18(L)F44K22 PIC18(L)F45K22 PIC18(L)F46K22	Enhanced PWM Full-Bridge	Enhanced PWM Full-Bridge	Enhanced PWM Half-Bridge	Standard PWM	Standard PWM (Special Event Trigger)

## FIGURE 15-4: SPI MASTER AND MULTIPLE SLAVE CONNECTION



#### 15.2.1 SPI MODE REGISTERS

The MSSPx module has five registers for SPI mode operation. These are:

- MSSPx STATUS register (SSPxSTAT)
- MSSPx Control register 1 (SSPxCON1)
- MSSPx Control register 3 (SSPxCON3)
- MSSPx Data Buffer register (SSPxBUF)
- MSSPx Address register (SSPxADD)
- MSSPx Shift register (SSPxSR) (Not directly accessible)

SSPxCON1 and SSPxSTAT are the control and STATUS registers in SPI mode operation. The SSPxCON1 register is readable and writable. The lower 6 bits of the SSPxSTAT are read-only. The upper two bits of the SSPxSTAT are read/write.

In one SPI Master mode, SSPxADD can be loaded with a value used in the Baud Rate Generator. More information on the Baud Rate Generator is available in **Section 15.7 "Baud Rate Generator"**.

SSPxSR is the shift register used for shifting data in and out. SSPxBUF provides indirect access to the SSPxSR register. SSPxBUF is the buffer register to which data bytes are written, and from which data bytes are read.

In receive operations, SSPxSR and SSPxBUF together create a buffered receiver. When SSPxSR receives a complete byte, it is transferred to SSPxBUF and the SSPxIF interrupt is set.

During transmission, the SSPxBUF is not buffered. A write to SSPxBUF will write to both SSPxBUF and SSPxSR.

### 15.2.2 SPI MODE OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPxCON1<5:0> and SSPxSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCKx is the clock output)
- Slave mode (SCKx is the clock input)
- Clock Polarity (Idle state of SCKx)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCKx)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

To enable the serial port, SSPx Enable bit, SSPxEN of the SSPxCON1 register, must be set. To reset or reconfigure SPI mode, clear the SSPxEN bit, re-initialize the SSPxCONx registers and then set the SSP<u>xEN</u> bit. This configures the SDIx, SDOx, SCKx and SSx pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- SDIx must have corresponding TRIS bit set
- SDOx must have corresponding TRIS bit cleared
- SCKx (Master mode) must have corresponding TRIS bit cleared
- SCKx (Slave mode) must have corresponding TRIS bit set
- SSx must have corresponding TRIS bit set



# FIGURE 15-19:

PIC18(L)F2X/4XK22

### 15.5.8 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the  $I^2C$  bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the  $I^2C$  protocol, defined as address 0x00. When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically  $\overline{ACK}$  the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 15-24 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCLx. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.



### FIGURE 15-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE

#### 15.5.9 SSPx MASK REGISTER

An SSPx Mask (SSPxMSK) register (Register 15-6) is available in I<sup>2</sup>C Slave mode as a mask for the value held in the SSPxSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSPx operation until written with a mask value.

The SSPx Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSPx mask has no effect during the reception of the first (high) byte of the address.

#### 15.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDAx or SCLx are sampled low at the beginning of the Start condition (Figure 15-33).
- b) SCLx is sampled low before SDAx is asserted low (Figure 15-34).

During a Start condition, both the SDAx and the SCLx pins are monitored.

If the SDAx pin is already low, or the SCLx pin is already low, then all of the following occur:

- · the Start condition is aborted,
- the BCLxIF flag is set and
- the MSSPx module is reset to its Idle state (Figure 15-33).

The Start condition begins with the SDAx and SCLx pins deasserted. When the SDAx pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCLx pin is sampled low while SDAx is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDAx pin is sampled low during this count, the BRG is reset and the SDAx line is asserted early (Figure 15-35). If, however, a '1' is sampled on the SDAx pin, the SDAx pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCLx pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCLx pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDAx before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

# FIGURE 15-33: BUS COLLISION DURING START CONDITION (SDAx ONLY)



Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	_	_	ANSA5	—	ANSA3	ANSA2	ANSA1	ANSA0	149
ANSELB	—	_	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1 <sup>(1)</sup>	ANSB0 <sup>(1)</sup>	150
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	_	_	150
ANSELD	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1 <sup>(2)</sup>	ANSD0 <sup>(2)</sup>	150
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	109
IPR1	_	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	121
IPR2	OSCFIP	C1IP	C2IP	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	122
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	CTMUIP	TMR5GIP	TMR3GIP	TMR1GIP	123
PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	117
PIE2	OSCFIE	C1IE	C2IE	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	118
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	CTMUIE	TMR5GIE	TMR3GIE	TMR1GIE	119
PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	112
PIR2	OSCFIF	C1IF	C2IF	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	113
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	CTMUIF	TMR5GIF	TMR3GIF	TMR1GIF	114
PMD1	MSSP2MD	MSSP1MD	_	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD	53
SSP1ADD	SSP1 Addre	ss Register in	I <sup>2</sup> C Slave n	node. SSP1	Baud Rate	Reload Reg	ister in I <sup>2</sup> C M	laster mode.	258
SSP1BUF			SSP1 Re	eceive Buffe	er/Transmit	Register			—
SSP1CON1	WCOL	SSPOV	SSPEN	CKP		SSPI	M<3:0>		253
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	255
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	256
SSP1MSK			S	SP1 MASK	Register bi	ts			257
SSP1STAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	252
SSP2ADD	SSP2 Addre	ss Register in	I <sup>2</sup> C Slave n	node. SSP2	Baud Rate	e Reload Reg	ister in I <sup>2</sup> C M	laster mode.	258
SSP2BUF			SSP2 Re	eceive Buffe	er/Transmit	Register			—
SSP2CON1	WCOL	SSPOV	SSPEN	CKP		SSPI	M<3:0>	0	253
SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	255
SSP2CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	256
SSP2MSK			S	SP1 MASK	Register bi	ts	1	1	257
SSP2STAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	252
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1 <sup>(1)</sup>	TRISB0 <sup>(1)</sup>	151
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	151
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1 <sup>(2)</sup>	TRISD0 <sup>(2)</sup>	151

# TABLE 15-2: REGISTERS ASSOCIATED WITH I<sup>2</sup>C OPERATION

**Legend:** Shaded bits are not used by the MSSPx in  $I^2C$  mode.

Note 1: PIC18(L)F2XK22 devices.

2: PIC18(L)F4XK22 devices.

# 16.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 16-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

#### 16.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 16-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREGx register.

#### 16.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTAx register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTAx register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTAx register enables the EUSART and automatically configures the TXx/CKx I/O pin as an output. If the TXx/CKx pin is shared with an analog peripheral the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

**Note:** The TXxIF transmitter interrupt flag is set when the TXEN enable bit is set.

#### 16.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREGx register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREGx is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREGx until the Stop bit of the previous character has been transmitted. The pending character in the TXREGx is then transferred to the TSR in one TCY immediately following the Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREGx.

#### 16.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the CKTXP bit of the BAUDCONx register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the CKTXP bit to '1' will invert the transmit data resulting in low true idle and data bits. The CKTXP bit controls transmit data polarity only in Asynchronous mode. In Synchronous mode the CKTXP bit has a different function.

#### 16.1.1.4 Transmit Interrupt Flag

The TXxIF interrupt flag bit of the PIR1/PIR3 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREGx. In other words, the TXxIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREGx. The TXxIF flag bit is not cleared immediately upon writing TXREGx. TXxIF becomes valid in the second instruction cycle following the write execution. Polling TXxIF immediately following the TXREGx write will return invalid results. The TXxIF bit is read-only, it cannot be set or cleared by software.

The TXxIF interrupt can be enabled by setting the TXxIE interrupt enable bit of the PIE1/PIE3 register. However, the TXxIF flag bit will be set whenever the TXREGx is empty, regardless of the state of TXxIE enable bit.

To use interrupts when transmitting data, set the TXxIE bit only when there is more data to send. Clear the TXxIE interrupt enable bit upon writing the last character of the transmission to the TXREGx.

# 16.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (HFINTOSC). However, the HFINTOSC frequency may drift as VDD or temperature changes, and this directly affects the asynchronous baud rate. Two methods may be used to adjust the baud rate clock, but both require a reference clock source of some kind.

The first (preferred) method uses the OSCTUNE register to adjust the HFINTOSC output. Adjusting the value in the OSCTUNE register allows for fine resolution changes to the system clock source. See **Section 2.6** "Internal Clock Modes" for more information.

The other method adjusts the value in the Baud Rate Generator. This can be done automatically with the Auto-Baud Detect feature (see **Section 16.4.1 "Auto-Baud Detect"**). There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

## **18.2 Comparator Control**

Each comparator has a separate control and Configuration register: CM1CON0 for Comparator C1 and CM2CON0 for Comparator C2. In addition, Comparator C2 has a second control register, CM2CON1, for controlling the interaction with Timer1 and simultaneous reading of both comparator outputs.

The CM1CON0 and CM2CON0 registers (see Register 18-1) contain the control and status bits for the following:

- Enable
- Input selection
- Reference selection
- Output selection
- Output polarity
- Speed selection

#### 18.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

#### 18.2.2 COMPARATOR INPUT SELECTION

The CxCH<1:0> bits of the CMxCON0 register direct one of four analog input pins to the comparator inverting input.

Note:	To us inputs	e CxIN+ an s, the appro	d C12INx- p priate bits n	ins as ai nust be :	nalog set in
	the	ANSEL	register	and	the
	corre	sponding T	RIS bits mus	st also b	e set
	to dis	able the ou	tput drivers.		

#### 18.2.3 COMPARATOR REFERENCE SELECTION

Setting the CxR bit of the CMxCON0 register directs an internal voltage reference or an analog input pin to the non-inverting input of the comparator. See **Section 21.0 "Fixed Voltage Reference (FVR)"** for more information on the Internal Voltage Reference module.

#### 18.2.4 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CM2CON1 register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- · Corresponding TRIS bit must be cleared
- CxON bit of the CMxCON0 register must be set

- Note 1: The CxOE bit overrides the PORT data latch. Setting the CxON has no impact on the port override.
  - 2: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

#### 18.2.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 18-1 shows the output state versus input conditions, including polarity control.

#### TABLE 18-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVIN - > CxVIN +	0	0
CxVIN- < CxVIN+	0	1
CxVIN - > CxVIN +	1	1
CxVIN- < CxVIN+	1	0

# 18.2.6 COMPARATOR SPEED SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the normal speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

# 18.3 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 27.0 "Electrical Specifications"** for more details.

# 18.4 Comparator Interrupt Operation

The comparator interrupt flag will be set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusiveor gate (see Figure 18-2). The first latch is updated with the comparator output value, when the CMxCON0 register is read or written. The value is latched on the third cycle of the system clock, also known as Q3. This first latch retains the comparator value until another read or write of the CMxCON0 register occurs or a Reset takes place. The second latch is updated with the comparator output value on every first cycle of the system clock, also known as Q1. When the output value of the comparator changes, the second latch is updated and the output values of both latches no longer match one another, resulting in a mismatch condition. The latch outputs are fed directly into the inputs of an exclusive-or gate. This mismatch condition is detected by the exclusive-or gate and sent to the interrupt circuitry. The mismatch condition will persist until the first latch value is updated by performing a read of the CMxCON0 register or the comparator output returns to the previous state.

- Note 1: A write operation to the CMxCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.
  - **2:** Comparator interrupts will operate correctly regardless of the state of CxOE.

When the mismatch condition occurs, the comparator interrupt flag is set. The interrupt flag is triggered by the edge of the changing value coming from the exclusiveor gate. This means that the interrupt flag can be reset once it is triggered without the additional step of reading or writing the CMxCON0 register to clear the mismatch latches. When the mismatch registers are cleared, an interrupt will occur upon the comparator's return to the previous state, otherwise no interrupt will be generated.

Software will need to maintain information about the status of the comparator output, as read from the CMxCON0 register, or CM2CON1 register, to determine the actual change that has occurred. See Figures 18-3 and 18-4.

The CxIF bit of the PIR2 register is the comparator interrupt flag. This bit must be reset by software by clearing it to '0'. Since it is also possible to write a '1' to this register, an interrupt can be generated.

In mid-range Compatibility mode the CxIE bit of the PIE2 register and the PEIE/GIEL and GIE/GIEH bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CxIF bit of the PIR2 register will still be set if an interrupt condition occurs.

# 18.4.1 PRESETTING THE MISMATCH LATCHES

The comparator mismatch latches can be preset to the desired state before the comparators are enabled. When the comparator is off the CxPOL bit controls the CxOUT level. Set the CxPOL bit to the desired CxOUT non-interrupt level while the CxON bit is cleared. Then, configure the desired CxPOL level in the same instruction that the CxON bit is set. Since all register writes are performed as a read-modify-write, the mismatch latches will be cleared during the instruction read phase and the actual configuration of the CxON and CxPOL bits will be occur in the final write phase.

FIGURE 18-3:

#### COMPARATOR INTERRUPT TIMING W/O CMxCON0 READ





COMPARATOR INTERRUPT TIMING WITH CMxCON0 READ



- Note 1: If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF interrupt flag of the PIR2 register may not get set.
  - 2: When either comparator is first enabled, bias circuitry in the comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

<sup>© 2010-2016</sup> Microchip Technology Inc.

# 20.0 SR LATCH

The module consists of a single SR latch with multiple Set and Reset inputs as well as separate latch outputs. The SR latch module includes the following features:

- Programmable input selection
- SR latch output is available internally/externally
- Selectable Q and  $\overline{Q}$  output
- Firmware Set and Reset

The SR latch can be used in a variety of analog applications, including oscillator circuits, one-shot circuit, hysteretic controllers, and analog timing applications.

# 20.1 Latch Operation

The latch is a Set-Reset latch that does not depend on a clock source. Each of the Set and Reset inputs are active-high. The latch can be set or reset by:

- Software control (SRPS and SRPR bits)
- Comparator C1 output (sync\_C1OUT)
- Comparator C2 output (sync\_C2OUT)
- SRI Pin
- Programmable clock (DIVSRCLK)

The SRPS and the SRPR bits of the SRCON0 register may be used to set or reset the SR latch, respectively. The latch is Reset-dominant. Therefore, if both Set and Reset inputs are high, the latch will go to the Reset state. Both the SRPS and SRPR bits are self resetting which means that a single write to either of the bits is all that is necessary to complete a latch Set or Reset operation.

The output from Comparator C1 or C2 can be used as the Set or Reset inputs of the SR latch. The output of either Comparator can be synchronized to the Timer1 clock source. See Section 18.0 "Comparator Module" and Section 12.0 "Timer1/3/5 Module with Gate Control" for more information.

An external source on the SRI pin can be used as the Set or Reset inputs of the SR latch.

An internal clock source, DIVSRCLK, is available and it can periodically set or reset the SR latch. The SRCLK<2:0> bits in the SRCON0 register are used to select the clock source period. The SRSCKE and SRRCKE bits of the SRCON1 register enable the clock source to set or reset the SR latch, respectively.

# 20.2 Latch Output

The SRQEN and SRNQEN bits of the SRCON0 register control the Q and  $\overline{Q}$  latch outputs. Both of the SR latch outputs may be directly output to I/O pins at the same time. Control is determined by the state of bits SRQEN and SRNQEN in the SRCON0 register.

The applicable TRIS bit of the corresponding port must be cleared to enable the port pin output driver.

# 20.3 DIVSRCLK Clock Generation

The DIVSRCLK clock signal is generated from the peripheral clock which is pre-scaled by a value determined by the SRCLK<2:0> bits. See Figure 20-2 and Table 20-1 for additional detail.

# 20.4 Effects of a Reset

Upon any device Reset, the SR latch is not initialized, and the SRQ and SRNQ outputs are unknown. The user's firmware is responsible to initialize the latch output before enabling it to the output pins.

BRA	۱.	Unconditional Branch					
Synta	ax:	BRA n					
Oper	ands:	-1024 $\leq$ n $\leq$	$-1024 \le n \le 1023$				
Oper	ation:	(PC) + 2 + 2	$2n \rightarrow PC$				
Statu	s Affected:	None					
Enco	ding:	1101	0nnn	nnnn	nnnn		
the PC. Since the PC will have incre- mented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a 2-cycle instruction.					ve incre- ruction, the - 2n. This ction.		
Word	ls:	1					
Cycle	es:	2					
QC	ycle Activity:						
	Q1	Q2	C	23	Q4		
	Decode	Read litera	al Pro	cess ata	Write to PC		
	No	No	١	lo	No		
	operation	operation	oper	ration	operation		

Example:	HERE	BRA	Jump
Before Instruction	on		
PC	=	address	(HERE)
After Instruction	I		
PC	=	address	(Jump)

BSF	Bit Set f					
Syntax:	BSF f, b {	,a}				
Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ 0 \leq b \leq 7 \\ a \in [0,1] \end{array}$	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0,1]$				
Operation:	$1 \rightarrow f < b >$					
Status Affected:	None					
Encoding:	1000	bbba	ffff	ffff		
	If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank. If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.					
Words:	1					
Cycles:	1					
Q Cycle Activity:						
Q1	Q2	Q3	3	Q4		
Decode	Read register 'f'	Proce Dat	ess a re	Write gister 'f'		
Example:	BSF F	'LAG_RE	G, 7, 1			

FLAG\_REG = 0Ah After Instruction FLAG\_REG = 8Ah

DS40001412G-page 372

### 27.11.3 TIMING DIAGRAMS AND SPECIFICATIONS



#### TABLE 27-7: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Мах	Units	Conditions
1A	Fosc	External CLKIN	DC	0.5	MHz	EC, ECIO Oscillator mode (low power)
		Frequency <sup>(1)</sup>	DC	16	MHz	EC, ECIO Oscillator mode (medium power)
			DC	64	MHz	EC, ECIO Oscillator mode (high power)
		Oscillator Frequency <sup>(1)</sup>	DC	4	MHz	RC Oscillator mode
			5	200	kHz	LP Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			4	4	MHz	HS Oscillator mode, VDD < 2.7V
			4	16	MHz	HS Oscillator mode, $VDD \ge 2.7V$ , Medium-Power mode (HSMP)
			4	20	MHz	HS Oscillator mode, $VDD \ge 2.7V$ , High-Power mode (HSHP)
1	Tosc	External CLKIN Period <sup>(1)</sup>	2.0 62.5	_	μS ns	EC, ECIO Oscillator mode (low power)
			02.0		110	EC, ECIO Oscillator mode (high power)
			15.6		ns	
		Oscillator Period <sup>(1)</sup>	250	—	ns	RC Oscillator mode
			5	200	μs	LP Oscillator mode
			0.25 250	10 250	μs ns	XT Oscillator mode HS Oscillator mode, VDD < 2.7V
			62.5	250	ns	HS Oscillator mode, $VDD \ge 2.7V$ , Medium-Power mode (HSMP)
			50	250	ns	HS Oscillator mode, $VDD \ge 2.7V$ , High-Power mode (HSHP)
2	Тсү	Instruction Cycle Time <sup>(1)</sup>	62.5	_	ns	TCY = 4/FOSC
3	TosL,	External Clock in (OSC1)	2.5	_	μs	LP Oscillator mode
	TosH	High or Low Time	30	_	ns	XT Oscillator mode
			10	_	ns	HS Oscillator mode
4	TosR,	External Clock in (OSC1)	_	50	ns	LP Oscillator mode
	TosF	Rise or Fall Time	—	20	ns	XT Oscillator mode
			_	7.5	ns	HS Oscillator mode

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
F10	Fosc	Oscillator Frequency Range	4	5	MHz	VDD < 2.7V, -40°C to +85°C
			4	4	MHz	VDD < 2.7V, +85°C to +125°C
			4	16	MHz	$2.7V \le VDD$ , -40°C to +85°C
			4	12	MHz	2.7V ≤ VDD, +85°C to +125°C
F11	Fsys	On-Chip VCO System Frequency	16	20	MHz	VDD < 2.7V, -40°C to +85°C
			16	16	MHz	VDD < 2.7V, +85°C to +125°C
			16	64	MHz	$2.7V \le VDD$ , -40°C to +85°C
			16	48	MHz	2.7V ≤ VDD, +85°C to +125°C
F12	t <sub>rc</sub>	PLL Start-up Time (Lock Time)	_	2	ms	

## TABLE 27-8: PLL CLOCK TIMING SPECIFICATIONS

## TABLE 27-9: AC CHARACTERISTICS:INTERNAL OSCILLATORS ACCURACY PIC18(L)F46K22

Standard Operating Conditions (unless otherwise stated)							
Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$							

Param. No.	Characteristics	Freq. Tolerance	Min	Тур†	Max	Units	Conditions
OA1	Internal Calibrated	± 2%	_	16.0	—	MHz	$0^{\circ}C \leq \text{Ta} \leq \textbf{+60}^{\circ}C, \; \text{Vdd} \geq 2.5 \text{V}$
	HFINTOSC Frequency <sup>(1)</sup>	$\pm$ 3%	—	16.0	—	MHz	+60°C $\leq$ TA $\leq$ +85°C, VDD $\geq$ 2.5V
		$\pm$ 5%	—	16.0	—	MHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$
OA2	Internal Calibrated	± 2%	_	500	—	kHz	$0^{\circ}C \leq \text{Ta} \leq \textbf{+60^{\circ}C}, \ \text{Vdd} \geq 2.5 \text{V}$
	MFINTOSC Frequency <sup>(1)</sup>	$\pm$ 3%	—	500	—	kHz	+60°C $\leq$ Ta $\leq$ +85°C, Vdd $\geq$ 2.5V
		$\pm$ 5%	—	500	—	kHz	$-40^{\circ}C \leq TA \leq +125^{\circ}C$
OA3	Internal Calibrated LFINTOSC Frequency <sup>(1)</sup>	± 20%	_	31	_	kHz	$-40^{\circ}C \leq \text{Ta} \leq +125^{\circ}C$

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1  $\mu$ F and 0.01  $\mu$ F values in parallel are recommended.

























© 2010-2016 Microchip Technology Inc.