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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf23k22-i-sp

TABLE 1-1: DEVICE FEATURES

Features	PIC18F23K22 PIC18LF23K22	PIC18F24K22 PIC18LF24K22	PIC18F25K22 PIC18(L)F25K22	PIC18F26K22 PIC18LF26K22	PIC18F43K22 PIC18LF43K22	PIC18F44K22 PIC18LF44K22	PIC18F45K22 PIC18LF45K22	PIC18F46K22 PIC18LF46K22
Program Memory (Bytes)	8192	16384	32768	65536	8192	16384	32768	65536
Program Memory (Instructions)	4096	8192	16384	32768	4096	8192	16384	32768
Data Memory (Bytes)	512	768	1536	3896	512	768	1536	3896
Data EEPROM Memory (Bytes)	256	256	256	1024	256	256	256	1024
I/O Ports	A, B, C, E ⁽¹⁾	A, B, C, E ⁽¹⁾	A, B, C, E ⁽¹⁾	A, B, C, E ⁽¹⁾	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E	A, B, C, D, E
Capture/Compare/PWM Modules (CCP)	2	2	2	2	2	2	2	2
Enhanced CCP Modules (ECCP) - Half Bridge	2	2	2	2	1	1	1	1
Enhanced CCP Modules (ECCP) - Full Bridge	1	1	1	1	2	2	2	2
10-bit Analog-to-Digital Module (ADC)	2 internal 17 input	2 internal 17 input	2 internal 17 input	2 internal 17 input	2 internal 28 input	2 internal 28 input	2 internal 28 input	2 internal 28 input
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 40-pin UQFN 44-pin QFN 44-pin TQFP	40-pin PDIP 40-pin UQFN 44-pin QFN 44-pin TQFP	40-pin PDIP 40-pin UQFN 44-pin QFN 44-pin TQFP	40-pin PDIP 40-pin UQFN 44-pin QFN 44-pin TQFP
Interrupt Sources	33							
Timers (16-bit)	4							
Serial Communications	2 MSSP, 2 EUSART							
SR Latch	Yes							
Charge Time Measurement Unit Module (CTMU)	Yes							
Programmable High/Low-Voltage Detect (HLVD)	Yes							
Programmable Brown-out Reset (BOR)	Yes							
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Overflow, Stack Underflow (PWRT, OST), MCLR, WDT							
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled							
Operating Frequency	DC - 64 MHz							

Note 1: PORTE contains the single RE3 read-only bit.

2.9 Effects of Power-Managed Modes on the Various Clock Sources

For more information about the modes discussed in this section see **Section 3.0 “Power-Managed Modes”**. A quick reference list is also available in Table 3-1.

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin, if used by the oscillator) will stop oscillating.

In secondary clock modes (SEC_RUN and SEC_IDLE), the secondary oscillator (SOSC) is operating and providing the device clock. The secondary oscillator may also run in all power-managed modes if required to clock Timer1, Timer3 or Timer5.

In internal oscillator modes (INTOSC_RUN and INTOSC_IDLE), the internal oscillator block provides the device clock source. The 31.25 kHz LFINTOSC output can be used directly to provide the clock and may be enabled to support various special features, regardless of the power-managed mode (see **Section 24.3 “Watchdog Timer (WDT)”**, **Section 2.12 “Two-Speed Clock Start-up Mode”** and **Section 2.13 “Fail-Safe Clock Monitor”** for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up). The HFINTOSC and MFINTOSC outputs may be used directly to clock the device or may be divided down by the postscaler. The HFINTOSC and MFINTOSC outputs are disabled when the clock is provided directly from the LFINTOSC output.

When the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The LFINTOSC is required to support WDT operation. Other features may be operating that do not require a device clock source (i.e., SSP slave, PSP, INTn pins and others). Peripherals that may add significant current consumption are listed in **Section 27.8 “DC Characteristics: Input/Output Characteristics, PIC18(L)F2X/4XK22”**.

2.10 Power-up Delays

Power-up delays are controlled by two timers, so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 4.6 “Device Reset Timers”**.

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on power-up. It is enabled by clearing (= 0) the PWRTEN Configuration bit.

The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (LP, XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the PLL is enabled with external oscillator modes, the device is kept in Reset for an additional 2 ms, following the OST delay, so the PLL can lock to the incoming clock frequency.

There is a delay of interval T_{CSD}, following POR, while the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC, RC or INTOSC modes are used as the primary clock source.

When the HFINTOSC is selected as the primary clock, the main system clock can be delayed until the HFINTOSC is stable. This is user selectable by the HFOFST bit of the CONFIG3H Configuration register. When the HFOFST bit is cleared, the main system clock is delayed until the HFINTOSC is stable. When the HFOFST bit is set, the main system clock starts immediately.

In either case, the HFIOFS bit of the OSCCON register can be read to determine whether the HFINTOSC is operating and stable.

2.11.3 CLOCK SWITCH TIMING

When switching between one oscillator and another, the new oscillator may not be operating which saves power (see Figure 2-9). If this is the case, there is a delay after the SCS<1:0> bits of the OSCCON register are modified before the frequency change takes place. The OSTS and IOFS bits of the OSCCON register will reflect the current active status of the external and HFINTOSC oscillators. The timing of a frequency selection is as follows:

1. SCS<1:0> bits of the OSCCON register are modified.
2. The old clock continues to operate until the new clock is ready.
3. Clock switch circuitry waits for two consecutive rising edges of the old clock after the new clock ready signal goes true.
4. The system clock is held low starting at the next falling edge of the old clock.
5. Clock switch circuitry waits for an additional two rising edges of the new clock.
6. On the next falling edge of the new clock the low hold on the system clock is released and new clock is switched in as the system clock.
7. Clock switch is complete.

See Figure 2-1 for more details.

If the HFINTOSC is the source of both the old and new frequency, there is no start-up delay before the new frequency is active. This is because the old and new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

Start-up delay specifications are located in **Section 27.0 “Electrical Specifications”**, under AC Specifications (Oscillator Module).

2.12 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the HFINTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note: Executing a <code>SLEEP</code> instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCCON register to remain clear.

When the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 2.5.1 “Oscillator Start-up Timer (OST)”**). The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit of the OSCCON register is set, program execution switches to the external oscillator.

2.12.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is enabled when all of the following settings are configured as noted:

- Two-Speed Start-up mode is enabled when the IESO of the CONFIG1H Configuration register is set.
- SCS<1:0> (of the OSCCON register) = 00.
- FOSC<2:0> bits of the CONFIG1H Configuration register are configured for LP, XT or HS mode.

Two-Speed Start-up mode becomes active after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

PIC18(L)F2X/4XK22

TABLE 4-2: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up ⁽²⁾ and Brown-out		Exit from Power-Managed Mode
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	
HSPLL	$66 \text{ ms}^{(1)} + 1024 \text{ TOSC} + 2 \text{ ms}^{(2)}$	$1024 \text{ TOSC} + 2 \text{ ms}^{(2)}$	$1024 \text{ TOSC} + 2 \text{ ms}^{(2)}$
HS, XT, LP	$66 \text{ ms}^{(1)} + 1024 \text{ TOSC}$	1024 TOSC	1024 TOSC
EC, ECIO	$66 \text{ ms}^{(1)}$	—	—
RC, RCIO	$66 \text{ ms}^{(1)}$	—	—
INTIO1, INTIO2	$66 \text{ ms}^{(1)}$	—	—

Note 1: 66 ms (65.5 ms) is the nominal Power-up Timer (PWRT) delay.

Note 2: 2 ms is the nominal time required for the PLL to lock.

FIGURE 4-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD} , V_{DD} RISE < T_{PWRT})

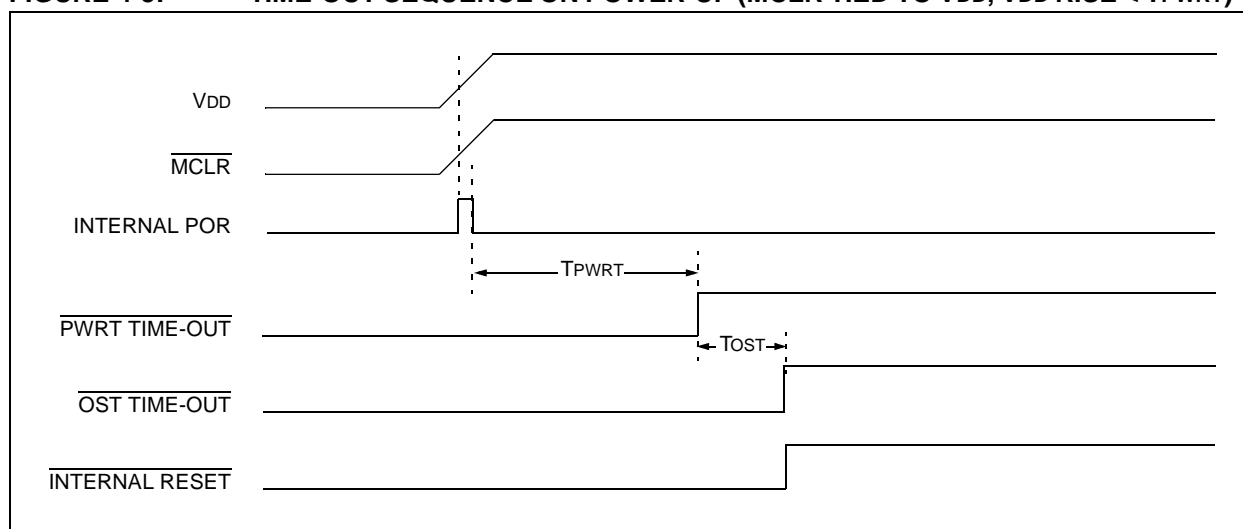
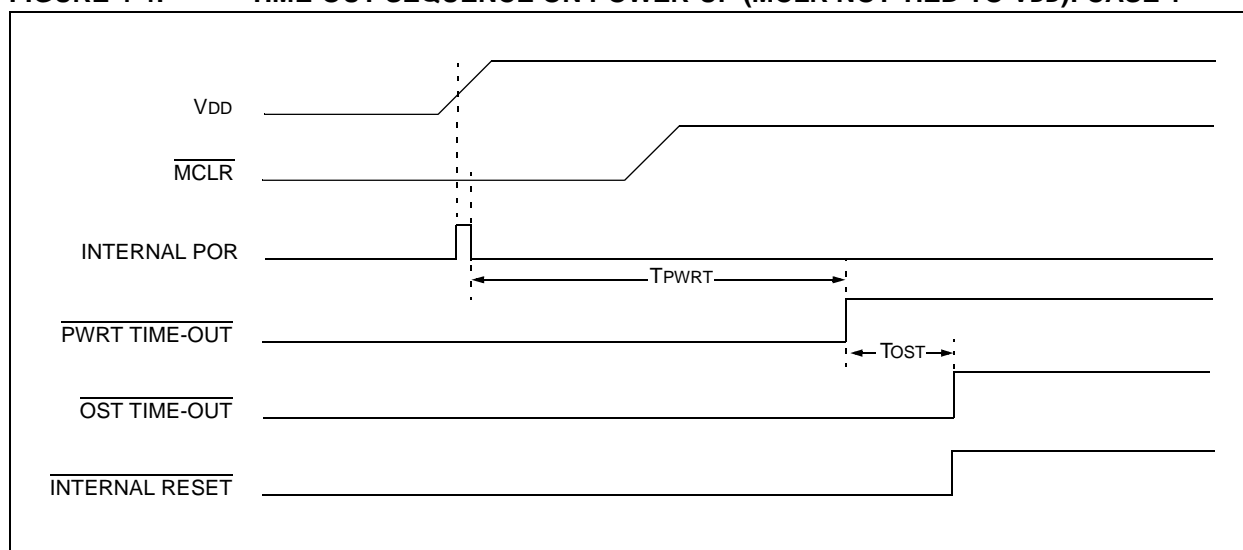


FIGURE 4-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1



PIC18(L)F2X/4XK22

TABLE 5-2: REGISTER FILE SUMMARY FOR PIC18(L)F2X/4XK22 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	
FD1h	WDTCON	—	—	—	—	—	—	—	SWDTEN	---- --0	
FD0h	RCON	IPEN	SBOREN	—	RI	TO	PD	POR	BOR	01-1 1100	
FCFh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	
FCEh	TMR1L	Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	
FCDh	T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1SOSCEN	T1SYN \overline{C}	T1RD16	TMR1ON	0000 0000	
FCCh	T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GSS<1:0>		0000 xx00	
FCBh	SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000 0000	
FCAh	SSP1MSK	SSP1 MASK Register bits								1111 1111	
FC9h	SSP1BUF	SSP1 Receive Buffer/Transmit Register								xxxx xxxx	
FC8h	SSP1ADD	SSP1 Address Register in I ² C Slave Mode. SSP1 Baud Rate Reload Register in I ² C Master Mode								0000 0000	
FC7h	SSP1STAT	SMP	CKE	D/ \overline{A}	P	S	R/ \overline{W}	UA	BF	0000 0000	
FC6h	SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				0000 0000	
FC5h	SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	
FC4h	ADRESH	A/D Result, High Byte								xxxx xxxx	
FC3h	ADRESL	A/D Result, Low Byte								xxxx xxxx	
FC2h	ADCON0	—	CHS<4:0>					GO/ \overline{DONE}	ADON	--00 0000	
FC1h	ADCON1	TRIGSEL	—	—	—	PVCFG<1:0>		NVCFG<1:0>		0--- 0000	
FC0h	ADCON2	ADFM	—	ACQT<2:0>			ADCS<2:0>				0-00 0000
FBFh	CCPR1H	Capture/Compare/PWM Register 1, High Byte								xxxx xxxx	
FBEh	CCPR1L	Capture/Compare/PWM Register 1, Low Byte								xxxx xxxx	
FBDh	CCP1CON	P1M<1:0>		DC1B<1:0>		CCP1M<3:0>				0000 0000	
FBCh	TMR2	Timer2 Register								0000 0000	
FBBh	PR2	Timer2 Period Register								1111 1111	
FBAh	T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000	
FB9h	PSTR1CON	—	—	—	STR1SYNC	STR1D	STR1C	STR1B	STR1A	---0 0001	
FB8h	BAUDCON1	ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN	0100 0-00	
FB7h	PWM1CON	P1RSEN	P1DC<6:0>							0000 0000	
FB6h	ECCP1AS	CCP1ASE	CCP1AS<2:0>			PSS1AC<1:0>		PSS1BD<1:0>		0000 0000	
FB4h	T3GCON	TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/ DONE	T3GVAL	T3GSS<1:0>		0000 0x00	
FB3h	TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								xxxx xxxx	
FB2h	TMR3L	Least Significant Byte of the 16-bit TMR3 Register								xxxx xxxx	
FB1h	T3CON	TMR3CS<1:0>		T3CKPS<1:0>		T3SOSCEN	T3SYN \overline{C}	T3RD16	TMR3ON	0000 0000	
FB0h	SPBRGH1	EUSART1 Baud Rate Generator, High Byte								0000 0000	
FAFh	SPBRG1	EUSART1 Baud Rate Generator, Low Byte								0000 0000	
FAEh	RCREG1	EUSART1 Receive Register								0000 0000	
FADh	TXREG1	EUSART1 Transmit Register								0000 0000	
FACh	TXSTA1	CSRC	TX9	TXEN	SYNC	SEnDB	BRGH	TRMT	TX9D	0000 0010	
FABh	RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	
FAAh	EEADRH ⁽⁵⁾	—	—	—	—	—	—	EEADR<9:8>		---- --00	
FA9h	EEADR	EEADR<7:0>								0000 0000	
FA8h	EEDATA	EEPROM Data Register								0000 0000	
FA7h	EECON2	EEPROM Control Register 2 (not a physical register)								---- --00	
FA6h	EECON1	EEPGD	CFG5	—	FREE	WRERR	WREN	WR	RD	xx-0 x000	
FA5h	IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	CTMUIP	TMR5GIP	TMR3GIP	TMR1GIP	0000 0000	
FA4h	PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	CTMUIF	TMR5GIF	TMR3GIF	TMR1GIF	0000 0000	
FA3h	PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	CTMUIE	TMR5GIE	TMR3GIE	TMR1GIE	0000 0000	

Legend: x = unknown, u = unchanged, — = unimplemented, α = value depends on condition

- Note**
- 1: PIC18(L)F4XK22 devices only.
 - 2: PIC18(L)F2XK22 devices only.
 - 3: PIC18(L)F23/24K22 and PIC18(L)F43/44K22 devices only.
 - 4: PIC18(L)F26K22 and PIC18(L)F46K22 devices only.

PIC18(L)F2X/4XK22

TABLE 5-2: REGISTER FILE SUMMARY FOR PIC18(L)F2X/4XK22 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
F3Ah	ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	1111 11--
F39h	ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	--11 1111
F38h	ANSELA	—	—	ANSA5	—	ANSA3	ANSA2	ANSA1	ANSA0	--1- 1111

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

- Note**
- 1: PIC18(L)F4XK22 devices only.
 - 2: PIC18(L)F2XK22 devices only.
 - 3: PIC18(L)F23/24K22 and PIC18(L)F43/44K22 devices only.
 - 4: PIC18(L)F26K22 and PIC18(L)F46K22 devices only.

PIC18(L)F2X/4XK22

12.1 Timer1/3/5 Operation

The Timer1/3/5 module is a 16-bit incrementing counter which is accessed through the TMRxH:TMRxL register pair. Writes to TMRxH or TMRxL directly update the counter.

When used with an internal clock source, the module is a timer and increments on every instruction cycle. When used with an external clock source, the module can be used as either a timer or counter and increments on every selected edge of the external source.

Timer1/3/5 is enabled by configuring the TMRxON and TMRxGE bits in the TxCON and TxGCON registers, respectively. Table 12-1 displays the Timer1/3/5 enable selections.

TABLE 12-1: TIMER1/3/5 ENABLE SELECTIONS

TMRxON	TMRxGE	Timer1/3/5 Operation
0	0	Off
0	1	Off
1	0	Always On
1	1	Count Enabled

12.2 Clock Source Selection

The TMRxCS<1:0> and TxSOSCEN bits of the TxCON register are used to select the clock source for Timer1/3/5. The dedicated Secondary Oscillator circuit can be used as the clock source for Timer1, Timer3 and Timer5, simultaneously. Any of the TxSOSCEN bits will enable the Secondary Oscillator circuit and select it as the clock source for that particular timer. Table 12-2 displays the clock source selections.

TABLE 12-2: CLOCK SOURCE SELECTIONS

TMRxCS1	TMRxCS0	TxSOSCEN	Clock Source
0	1	x	System Clock (Fosc)
0	0	x	Instruction Clock (Fosc/4)
1	0	0	External Clocking on TxCKI Pin
1	0	1	Osc.Circuit On SOSCI/SOSCO Pins

12.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMRxH:TMRxL register pair will increment on multiples of Fosc as determined by the Timer1/3/5 prescaler.

When the Fosc internal clock source is selected, the Timer1/3/5 register value will increment by four counts every instruction clock cycle. Due to this condition, a 2 LSB error in resolution will occur when reading the Timer1/3/5 value. To utilize the full resolution of Timer1/3/5, an asynchronous input signal must be used to gate the Timer1/3/5 clock input.

The following asynchronous sources may be used:

- Asynchronous event on the TxG pin to Timer1/3/5 Gate
- C1 or C2 comparator input to Timer1/3/5 Gate

12.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1/3/5 module may work as a timer or a counter.

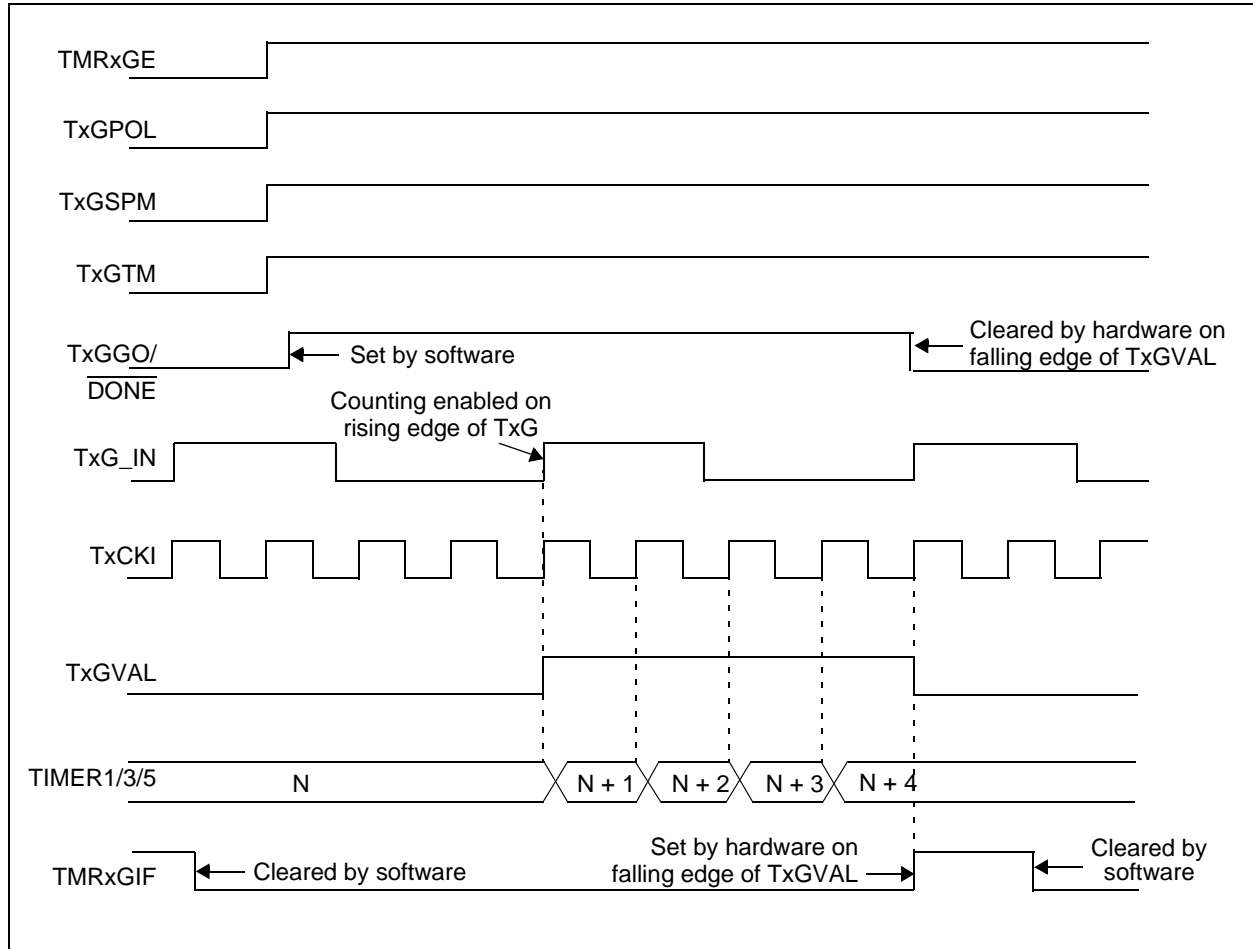
When enabled to count, Timer1/3/5 is incremented on the rising edge of the external clock input of the TxCKI pin. This external clock source can be synchronized to the microcontroller system clock or it can run asynchronously.

When used as a timer with a clock oscillator, an external 32.768 kHz crystal can be used in conjunction with the dedicated secondary internal oscillator circuit.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions:

- Timer1/3/5 enabled after POR
- Write to TMRxH or TMRxL
- Timer1/3/5 is disabled
- Timer1/3/5 is disabled (TMRxON = 0) when TxCKI is high then Timer1/3/5 is enabled (TMRxON=1) when TxCKI is low.

FIGURE 12-7: TIMER1/3/5 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



12.12 Peripheral Module Disable

When a peripheral module is not used or inactive, the module can be disabled by setting the Module Disable bit in the PMD registers. This will reduce power consumption to an absolute minimum. Setting the PMD bits holds the module in Reset and disconnects the module's clock source. The Module Disable bits for Timer1 (TMR1MD), Timer3 (TMR3MD) and Timer5 (TMR5MD) are in the PMD0 Register. See **Section 3.0 "Power-Managed Modes"** for more information.

REGISTER 12-2: TXGCON: TIMER1/3/5 GATE CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	R/W-0/u	R/W-0/u
TMRxGE	TxGPOL	TxGTM	TxGSPM	TxGGO/DONE	TxGVAL	TxGSS<1:0>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7	TMRxGE: Timer1/3/5 Gate Enable bit If TMRxON = 0 : This bit is ignored If TMRxON = 1 : 1 = Timer1/3/5 counting is controlled by the Timer1/3/5 gate function 0 = Timer1/3/5 counts regardless of Timer1/3/5 gate function
bit 6	TxGPOL: Timer1/3/5 Gate Polarity bit 1 = Timer1/3/5 gate is active-high (Timer1/3/5 counts when gate is high) 0 = Timer1/3/5 gate is active-low (Timer1/3/5 counts when gate is low)
bit 5	TxGTM: Timer1/3/5 Gate Toggle Mode bit 1 = Timer1/3/5 Gate Toggle mode is enabled 0 = Timer1/3/5 Gate Toggle mode is disabled and toggle flip-flop is cleared Timer1/3/5 gate flip-flop toggles on every rising edge.
bit 4	TxGSPM: Timer1/3/5 Gate Single-Pulse Mode bit 1 = Timer1/3/5 gate Single-Pulse mode is enabled and is controlling Timer1/3/5 gate 0 = Timer1/3/5 gate Single-Pulse mode is disabled
bit 3	TxGGO/DONE: Timer1/3/5 Gate Single-Pulse Acquisition Status bit 1 = Timer1/3/5 gate single-pulse acquisition is ready, waiting for an edge 0 = Timer1/3/5 gate single-pulse acquisition has completed or has not been started This bit is automatically cleared when TxGSPM is cleared.
bit 2	TxGVAL: Timer1/3/5 Gate Current State bit Indicates the current state of the Timer1/3/5 gate that could be provided to TMRxH:TMRxL. Unaffected by Timer1/3/5 Gate Enable (TMRxGE).
bit 1-0	TxGSS<1:0>: Timer1/3/5 Gate Source Select bits 00 = Timer1/3/5 Gate pin 01 = Timer2/4/6 Match PR2/4/6 output (See Table 12-5 for proper timer match selection) 10 = Comparator 1 optionally synchronized output (sync_C1OUT) 11 = Comparator 2 optionally synchronized output (sync_C2OUT)

PIC18(L)F2X/4XK22

REGISTER 14-5: ECCPxAS: CCPX AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCPxASE	CCPxAS<2:0>			PSSxAC<1:0>		PSSxBD<1:0>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **CCPxASE:** CCPx Auto-shutdown Event Status bit
if PxRSEN = 1;
1 = An Auto-shutdown event occurred; CCPxASE bit will automatically clear when event goes away;
CCPx outputs in shutdown state
0 = CCPx outputs are operating
if PxRSEN = 0;
1 = An Auto-shutdown event occurred; bit must be cleared in software to restart PWM;
CCPx outputs in shutdown state
0 = CCPx outputs are operating
- bit 6-4 **CCPxAS<2:0>:** CCPx Auto-Shutdown Source Select bits ⁽¹⁾
000 = Auto-shutdown is disabled
001 = Comparator C1 (async_C1OUT) – output high will cause shutdown event
010 = Comparator C2 (async_C2OUT) – output high will cause shutdown event
011 = Either Comparator C1 or C2 – output high will cause shutdown event
100 = FLT0 pin – low level will cause shutdown event
101 = FLT0 pin – low level or Comparator C1 (async_C1OUT) – high level will cause shutdown event
110 = FLT0 pin – low level or Comparator C2 (async_C2OUT) – high level will cause shutdown event
111 = FLT0 pin – low level or Comparators C1 or C2 – high level will cause shutdown event
- bit 3-2 **PSSxAC<1:0>:** Pins PxA and PxC Shutdown State Control bits
00 = Drive pins PxA and PxC to '0'
01 = Drive pins PxA and PxC to '1'
1x = Pins PxA and PxC tri-state
- bit 1-0 **PSSxBD<1:0>:** Pins PxB and PxD Shutdown State Control bits
00 = Drive pins PxB and PxD to '0'
01 = Drive pins PxB and PxD to '1'
1x = Pins PxB and PxD tri-state

Note 1: If C1SYNC or C2SYNC bits in the CM2CON1 register are enabled, the shutdown will be delayed by Timer1.

15.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCKx. When the last bit is latched, the SSPxIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCKx pin. The Idle state is determined by the CKP bit of the SSPxCON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCKx pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCKx pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake up from Sleep.

15.2.4.1 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 15-7 shows the block diagram of a typical daisy-chain connection when operating in SPI Mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSPxCON3 register will enable writes to the SSPxBUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

15.2.5 SLAVE SELECT SYNCHRONIZATION

The Slave Select can also be used to synchronize communication. The Slave Select line is held high until the master device is ready to communicate. When the Slave Select line is pulled low, the slave knows that a new transmission is starting.

If the slave fails to receive the communication properly, it will be reset at the end of the transmission, when the Slave Select line returns to a high state. The slave is then ready to receive a new transmission when the Slave Select line is pulled low again. If the Slave Select line is not used, there is a risk that the slave will eventually become out of sync with the master. If the slave misses a bit, it will always be one bit off in future transmissions. Use of the Slave Select line allows the slave and master to align themselves at the beginning of each transmission (Figure 15-8).

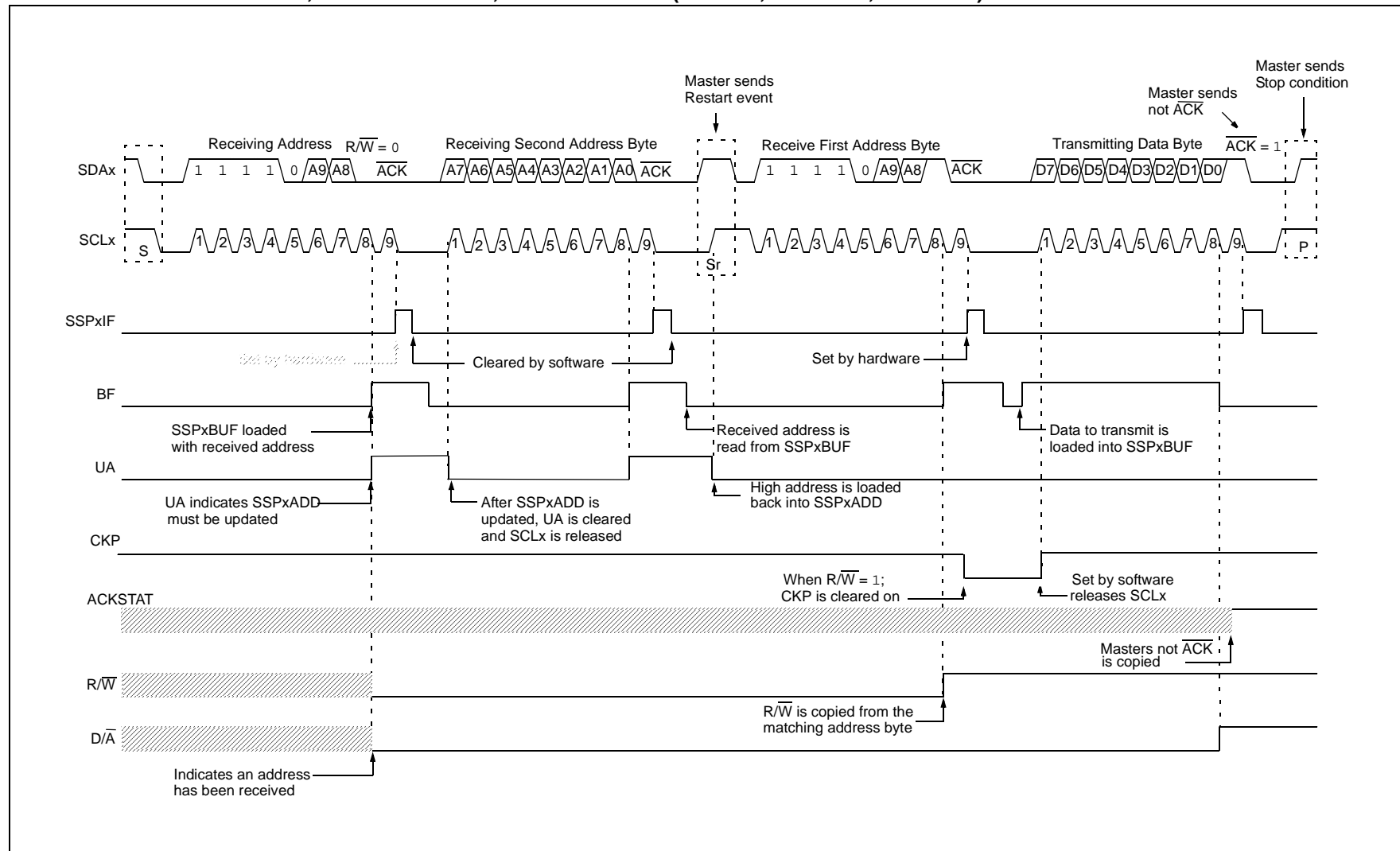
The \overline{SSx} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SSx} pin control enabled (SSPxCON1<3:0> = 0100).

When the \overline{SSx} pin is low, transmission and reception are enabled and the SDOx pin is driven.

When the \overline{SSx} pin goes high, the SDOx pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

- Note 1:** When the SPI is in Slave mode with \overline{SSx} pin control enabled (SSPxCON1<3:0> = 0100), the SPI module will reset if the \overline{SSx} pin is set to VDD.
- 2:** When the SPI is used in Slave mode with CKE set; the user must enable \overline{SSx} pin control.
- 3:** While operated in SPI Slave mode the SMP bit of the SSPxSTAT register must remain clear.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the \overline{SSx} pin to a high level or clearing the SSPxEN bit.

FIGURE 15-22: I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)

15.7 Baud Rate Generator

The MSSPx module has a Baud Rate Generator available for clock generation in both I²C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPxADD register (Register 15-7). When a write occurs to SSPxBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

An internal signal “Reload” in Figure 15-40 triggers the value from SSPxADD to be loaded into the BRG counter.

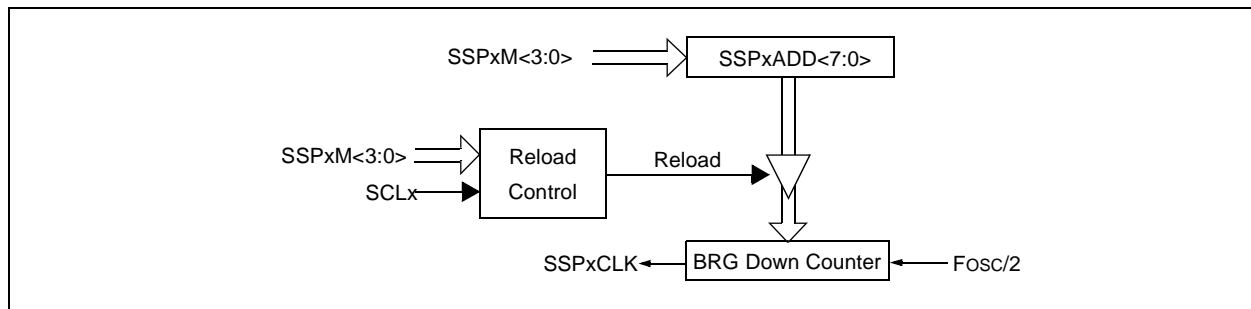
This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSPx is being operated in.

Table 15-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD.

EQUATION 15-1: F_{CLOCK} FORMULA

$$F_{CLOCK} = \frac{F_{OSC}}{(SSPxADD + 1)(4)}$$

FIGURE 15-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

TABLE 15-3: MSSPx CLOCK RATE W/BRG

Fosc	Fcy	BRG Value	F _{CLOCK} (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz ⁽¹⁾
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz ⁽¹⁾
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

PIC18(L)F2X/4XK22

REGISTER 15-5: SSPxCON3: SSPx CONTROL REGISTER 3

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **ACKTIM:** Acknowledge Time Status bit (I²C mode only)⁽³⁾
 1 = Indicates the I²C bus is in an Acknowledge sequence, set on 8th falling edge of SCLx clock
 0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCLx clock
- bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I²C mode only)
 1 = Enable interrupt on detection of Stop condition
 0 = Stop detection interrupts are disabled⁽²⁾
- bit 5 **SCIE:** Start Condition Interrupt Enable bit (I²C mode only)
 1 = Enable interrupt on detection of Start or Restart conditions
 0 = Start detection interrupts are disabled⁽²⁾
- bit 4 **BOEN:** Buffer Overwrite Enable bit
In SPI Slave mode:⁽¹⁾
 1 = SSPxBUF updates every time that a new data byte is shifted in ignoring the BF bit
 0 = If new byte is received with BF bit of the SSPxSTAT register already set, SSPxOV bit of the SSPxCON1 register is set, and the buffer is not updated
In I²C Master mode:
 This bit is ignored.
In I²C Slave mode:
 1 = SSPxBUF is updated and \overline{ACK} is generated for a received address/data byte, ignoring the state of the SSPxOV bit only if the BF bit = 0.
 0 = SSPxBUF is only updated when SSPxOV is clear
- bit 3 **SDAHT:** SDAx Hold Time Selection bit (I²C mode only)
 1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
 0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx
- bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)
 If on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCLxIF bit of the PIR2 register is set, and bus goes idle
 1 = Enable slave bus collision interrupts
 0 = Slave bus collision interrupts are disabled
- bit 1 **AHEN:** Address Hold Enable bit (I²C Slave mode only)
 1 = Following the 8th falling edge of SCLx for a matching received address byte; CKP bit of the SSPxCON1 register will be cleared and the SCLx will be held low.
 0 = Address holding is disabled

- Note 1:** For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPxOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSPxBUF.
- 2:** This bit has no effect in Slave modes for which Start and Stop condition detection is explicitly listed as enabled.
- 3:** The ACKTIM Status bit is active only when the AHEN bit or DHEN bit is set.

17.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

17.1.1 PORT CONFIGURATION

The ANSELx and TRISx registers configure the A/D port pins. Any port pin needed as an analog input should have its corresponding ANSx bit set to disable the digital input buffer and TRISx bit set to disable the digital output driver. If the TRISx bit is cleared, the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the ANSx bits and the TRIS bits.

Note 1: When reading the PORT register, all pins with their corresponding ANSx bit set read as cleared (a low level). However, analog conversion of pins configured as digital inputs (ANSx bit cleared and TRISx bit set) will be accurately converted.

- 2: Analog levels on any pin with the corresponding ANSx bit cleared may cause the digital input buffer to consume current out of the device's specification limits.
- 3: The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the bits in ANSELB are reset.

17.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 17.2 "ADC Operation"** for more information.

17.1.3 ADC VOLTAGE REFERENCE

The PVCFG<1:0> and NVCFG<1:0> bits of the ADCON1 register provide independent control of the positive and negative voltage references.

The positive voltage reference can be:

- VDD
- the fixed voltage reference (FVR BUF2)
- an external voltage source (VREF+)

The negative voltage reference can be:

- VSS
- an external voltage source (VREF-)

17.1.4 SELECTING AND CONFIGURING ACQUISITION TIME

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set.

Acquisition time is set with the ACQT<2:0> bits of the ADCON2 register. Acquisition delays cover a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there is no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT<2:0> = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT<2:0> bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. When an acquisition time is programmed, there is no indication of when the acquisition time ends and the conversion begins.

TABLE 25-1: OPCODE FIELD DESCRIPTIONS

Field	Description
a	RAM access bit a = 0: RAM location in Access RAM (BSR register is ignored) a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7).
BSR	Bank Select Register. Used to select the current RAM bank.
C, DC, Z, OV, N	ALU Status bits: C arry, D igit C arry, Z ero, O verflow, N egative.
d	Destination select bit d = 0: store result in WREG d = 1: store result in file register f
dest	Destination: either the WREG register or the specified register file location.
f	8-bit Register file address (00h to FFh) or 2-bit FSR designator (0h to 3h).
f _s	12-bit Register file address (000h to FFFh). This is the source address.
f _d	12-bit Register file address (000h to FFFh). This is the destination address.
GIE	Global Interrupt Enable bit.
k	Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value).
label	Label name.
mm	The mode of the TBLPTR register for the table read and table write instructions. Only used with table read and table write instructions:
*	No change to register (such as TBLPTR with table reads and writes)
++	Post-Increment register (such as TBLPTR with table reads and writes)
*-	Post-Decrement register (such as TBLPTR with table reads and writes)
++	Pre-Increment register (such as TBLPTR with table reads and writes)
n	The relative address (2's complement number) for relative branch instructions or the direct address for CALL/BRANCH and RETURN instructions.
PC	Program Counter.
PCL	Program Counter Low Byte.
PCH	Program Counter High Byte.
PCLATH	Program Counter High Byte Latch.
PCLATU	Program Counter Upper Byte Latch.
PD	Power-down bit.
PRODH	Product of Multiply High Byte.
PRODL	Product of Multiply Low Byte.
s	Fast Call/Return mode select bit s = 0: do not update into/from shadow registers s = 1: certain registers loaded into/from shadow registers (Fast mode)
TBLPTR	21-bit Table Pointer (points to a Program Memory location).
TABLAT	8-bit Table Latch.
TO	Time-out bit.
TOS	Top-of-Stack.
u	Unused or unchanged.
WDT	Watchdog Timer.
WREG	Working register (accumulator).
x	Don't care ('0' or '1'). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
z _s	7-bit offset value for indirect addressing of register files (source).
z _d	7-bit offset value for indirect addressing of register files (destination).
{ }	Optional argument.
[text]	Indicates an indexed address.
(text)	The contents of text.
[expr]<n>	Specifies bit n of the register indicated by the pointer expr.
→	Assigned to.
< >	Register bit field.
∈	In the set of.
italics	User defined term (font is Courier).

TABLE 25-2: PIC18(L)F2X/4XK22 INSTRUCTION SET (CONTINUED)

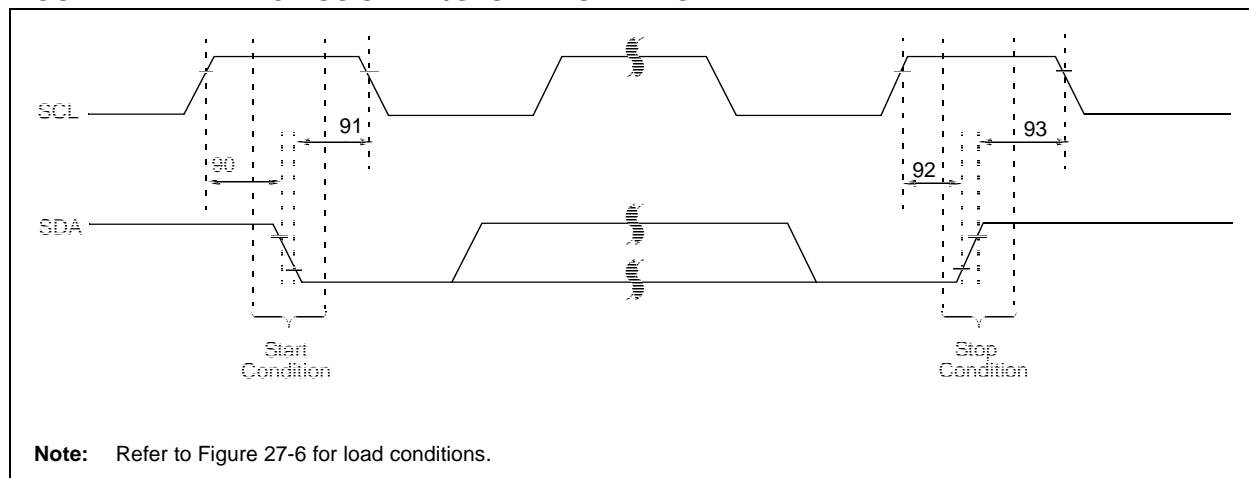
Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected	Notes	
			MSb		LSb				
LITERAL OPERATIONS									
ADDLW	k	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N	
ANDLW	k	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N	
IORLW	k	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N	
LFSR	f, k	Move literal (12-bit) 2nd word to FSR(f) 1st word	2	1110	1110	00ff	kkkk	None	
MOVLB	k	Move literal to BSR<3:0>	1	0000	0001	0000	kkkk	None	
MOVLW	k	Move literal to WREG	1	0000	1110	kkkk	kkkk	None	
MULLW	k	Multiply literal with WREG	1	0000	1101	kkkk	kkkk	None	
RETLW	k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
SUBLW	k	Subtract WREG from literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N	
XORLW	k	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N	
DATA MEMORY ↔ PROGRAM MEMORY OPERATIONS									
TBLRD*	Table Read	2	0000	0000	0000	1000	None		
TBLRD*+	Table Read with post-increment		0000	0000	0000	1001	None		
TBLRD*-	Table Read with post-decrement		0000	0000	0000	1010	None		
TBLRD*+	Table Read with pre-increment		0000	0000	0000	1011	None		
TBLWT*	Table Write	2	0000	0000	0000	1100	None		
TBLWT*+	Table Write with post-increment		0000	0000	0000	1101	None		
TBLWT*-	Table Write with post-decrement		0000	0000	0000	1110	None		
TBLWT*+	Table Write with pre-increment		0000	0000	0000	1111	None		

- Note 1:** When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.
- 3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.
- 4:** Some instructions are two-word instructions. The second word of these instructions will be executed as a `NOP` unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

TABLE 27-14: SPI MODE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS} \downarrow$ to SCK \downarrow or SCK \uparrow Input	T _{CY}	—	ns	
71	TscH	SCK Input High Time Continuous	25	—	ns	
72	TscL	SCK Input Low Time Continuous	30	—	ns	
73	TdiV2scH, TdiV2scL	Setup Time of SDI Data Input to SCK Edge	25	—	ns	
74	Tsch2diL, TscL2diL	Hold Time of SDI Data Input to SCK Edge	25	—	ns	
75	TdoR	SDO Data Output Rise Time	—	30	ns	
76	TdoF	SDO Data Output Fall Time	—	20	ns	
77	TssH2doZ	$\overline{SS} \uparrow$ to SDO Output High-Impedance	10	50	ns	
78	TscR	SCK Output Rise Time (Master mode)	—	30	ns	
79	TscF	SCK Output Fall Time (Master mode)	—	20	ns	
80	Tsch2doV, TscL2doV	SDO Data Output Valid after SCK Edge	—	20 60	ns ns	SPI Master Mode SPI Slave Mode
81	TdoV2scH, TdoV2scL	SDO Data Output Setup to SCK Edge	T _{CY}	—	ns	
82	TssL2doV	SDO Data Output Valid after $\overline{SS} \downarrow$ Edge	—	60	ns	
83	Tsch2ssH, TscL2ssH	$\overline{SS} \uparrow$ after SCK edge	1.5 T _{CY} + 40	—	ns	

FIGURE 27-17: I²C BUS START/STOP BITS TIMING



PIC18(L)F2X/4XK22

FIGURE 28-44: PIC18LF2X/4XK22 TYPICAL I_{DD} : RC_IDLE HF-INTOSC with PLL

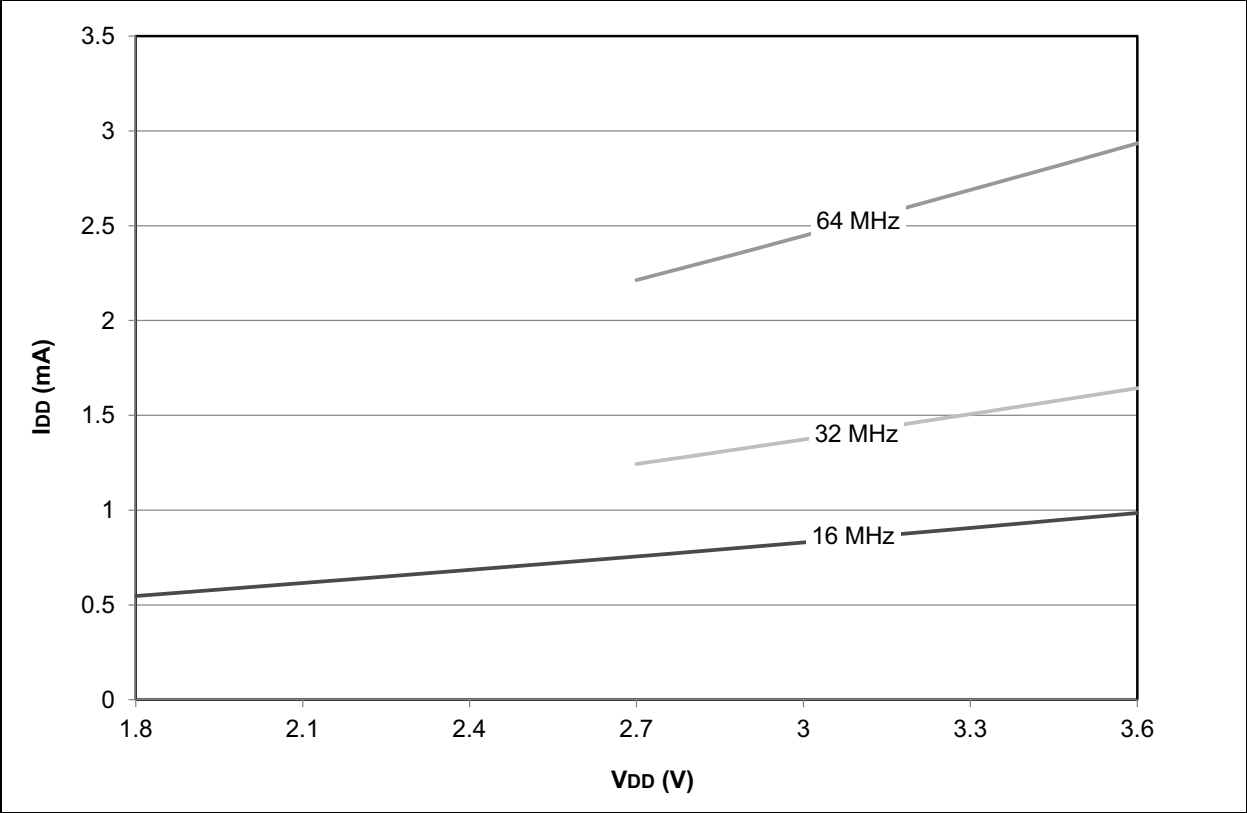


FIGURE 28-45: PIC18LF2X/4XK22 MAXIMUM I_{DD} : RC_IDLE HF-INTOSC with PLL

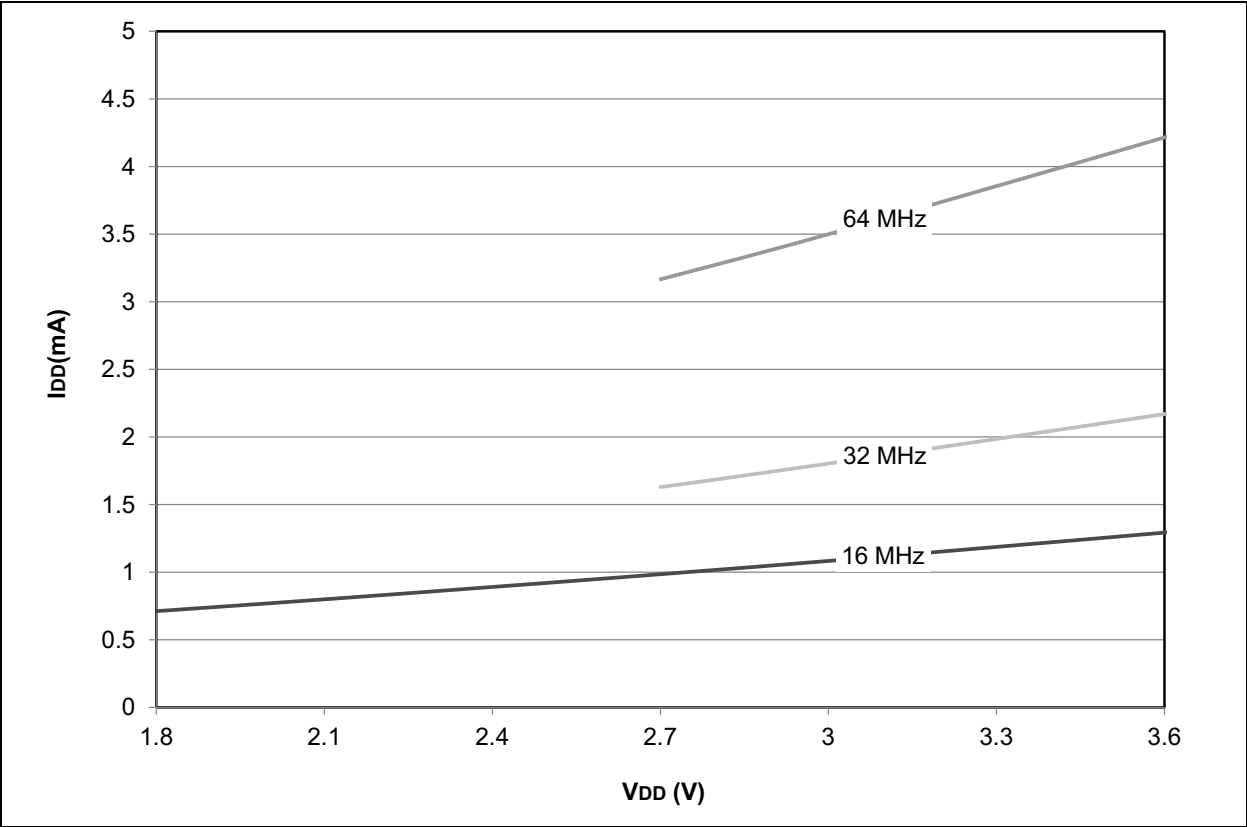


FIGURE 28-62: PIC18F2X/4XK22 TYPICAL I_{DD} : PRI_IDLE EC MEDIUM POWER

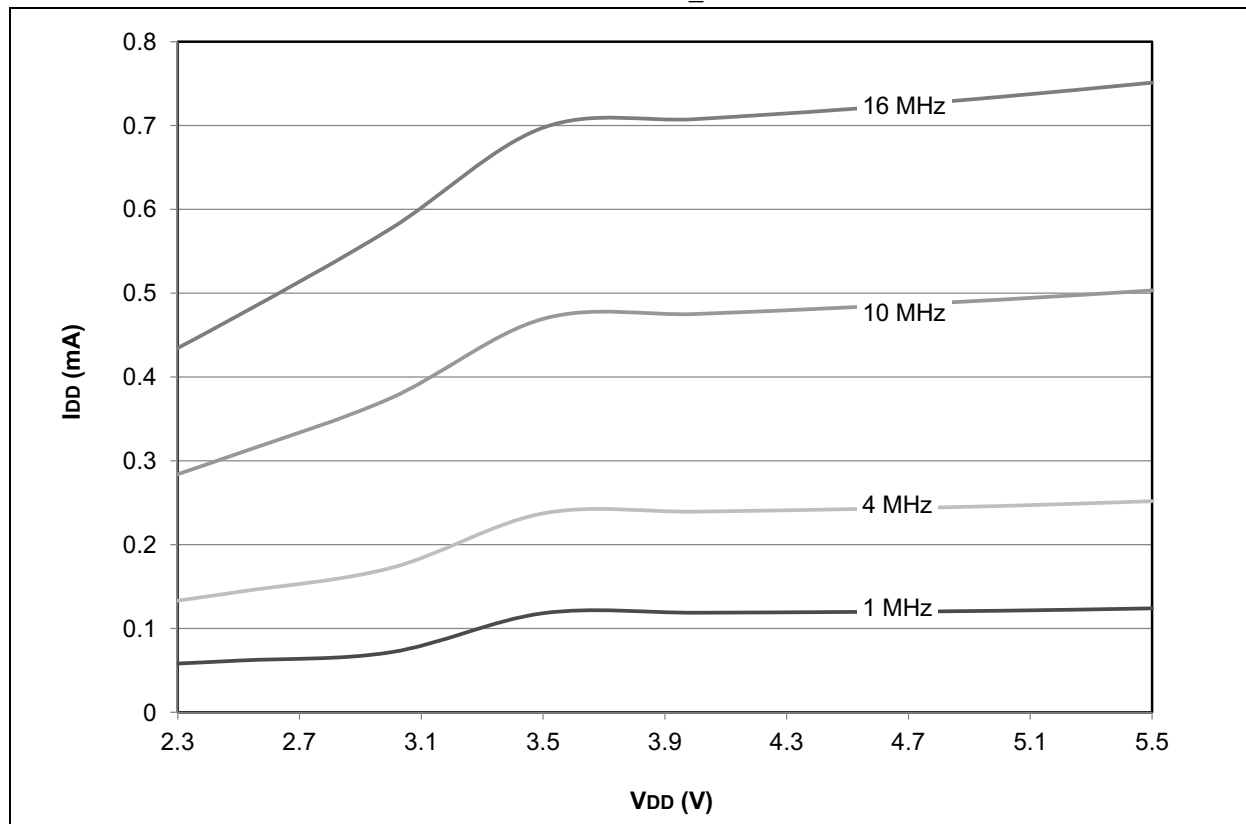


FIGURE 28-63: PIC18F2X/4XK22 MAXIMUM I_{DD} : PRI_IDLE EC MEDIUM POWER

