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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf25k22-e-ss

TABLE 1-3: PIC18(L)F4XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Number				Pin Name	Pin Type	Buffer Type	Description
PDIP	TQFP	QFN	UQFN				
18	37	37	33	RC3/SCK1/SCL1/AN15			
				RC3	I/O	ST	Digital I/O.
				SCK1	I/O	ST	Synchronous serial clock input/output for SPI mode (MSSP).
				SCL1	I/O	ST	Synchronous serial clock input/output for I^2C mode (MSSP).
				AN15	I	Analog	Analog input 15.
23	42	42	38	RC4/SDI1/SDA1/AN16			
				RC4	I/O	ST	Digital I/O.
				SDI1	I	ST	SPI data in (MSSP).
				SDA1	I/O	ST	I^2C data I/O (MSSP).
				AN16	I	Analog	Analog input 16.
24	43	43	39	RC5/SDO1/AN17			
				RC5	I/O	ST	Digital I/O.
				SDO1	O	—	SPI data out (MSSP).
				AN17	I	Analog	Analog input 17.
25	44	44	40	RC6/TX1/CK1/AN18			
				RC6	I/O	ST	Digital I/O.
				TX1	O	—	EUSART asynchronous transmit.
				CK1	I/O	ST	EUSART synchronous clock (see related RXx/DTx).
				AN18	I	Analog	Analog input 18.
26	1	1	1	RC7/RX1/DT1/AN19			
				RC7	I/O	ST	Digital I/O.
				RX1	I	ST	EUSART asynchronous receive.
				DT1	I/O	ST	EUSART synchronous data (see related TXx/CKx).
				AN19	I	Analog	Analog input 19.
19	38	38	34	RD0/SCK2/SCL2/AN20			
				RD0	I/O	ST	Digital I/O.
				SCK2	I/O	ST	Synchronous serial clock input/output for SPI mode (MSSP).
				SCL2	I/O	ST	Synchronous serial clock input/output for I^2C mode (MSSP).
				AN20	I	Analog	Analog input 20.
20	39	39	35	RD1/CCP4/SDI2/SDA2/AN21			
				RD1	I/O	ST	Digital I/O.
				CCP4	I/O	ST	Capture 4 input/Compare 4 output/PWM 4 output.
				SDI2	I	ST	SPI data in (MSSP).
				SDA2	I/O	ST	I^2C data I/O (MSSP).
				AN21	I	Analog	Analog input 21.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power.

Note 1: Default pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

TABLE 10-14: PORTE I/O SUMMARY

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RE0/P3A/CCP3/AN5	RE0	0	0	O	DIG	LATE<0> data output; not affected by analog input.
		1	0	I	ST	PORTE<0> data input; disabled when analog input enabled.
	P3A(1)	0	0	O	DIG	Enhanced CCP3 PWM output.
	CCP3(1)	0	0	O	DIG	Compare 3 output/PWM 3 output.
		1	0	I	ST	Capture 3 input.
	AN5	1	1	I	AN	Analog input 5.
RE1/P3B/AN6	RE1	0	0	O	DIG	LATE<1> data output; not affected by analog input.
		1	0	I	ST	PORTE<1> data input; disabled when analog input enabled.
	P3B	0	0	O	DIG	Enhanced CCP3 PWM output.
	AN6	1	1	I	AN	Analog input 6.
RE2/CCP5/AN7	RE2	0	0	O	DIG	LATE<2> data output; not affected by analog input.
		1	0	I	ST	PORTE<2> data input; disabled when analog input enabled.
	CCP5	0	0	O	DIG	Compare 5 output/PWM 5 output.
		1	0	I	ST	Capture 5 input.
	AN7	1	1	I	AN	Analog input 7.
RE3/VPP/$\overline{\text{MCLR}}$	RE3	—	—	I	ST	PORTE<3> data input; enabled when Configuration bit MCLRE = 0.
	VPP	—	—	P	AN	Programming voltage input; always available
	$\overline{\text{MCLR}}$	—	—	I	ST	Active-low Master Clear (device Reset) input; enabled when configuration bit MCLRE = 1.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C.

Note 1: Alternate pin assignment for P3A/CCP3 when Configuration bit CCP3MX is clear.

12.13 Register Definitions: Timer1/3/5 Control

REGISTER 12-1: TXCON: TIMER1/3/5 CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/0	R/W-0/u
TMRxCS<1:0>		TxCKPS<1:0>		TxSOSCEN	$\overline{\text{TxSYNC}}$	TxRD16	TMRxON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **TMRxCS<1:0>:** Timer1/3/5 Clock Source Select bits

11 = Reserved. Do not use.
10 = Timer1/3/5 clock source is pin or oscillator:
If TxSOSCEN = 0:
External clock from TxCKI pin (on the rising edge)
If TxSOSCEN = 1:
Crystal oscillator on SOSCI/SOSCO pins
01 = Timer1/3/5 clock source is system clock (FOSC)
00 = Timer1/3/5 clock source is instruction clock (FOSC/4)

bit 5-4 **TxCKPS<1:0>:** Timer1/3/5 Input Clock Prescale Select bits

11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **TxSOSCEN:** Secondary Oscillator Enable Control bit

1 = Dedicated Secondary oscillator circuit enabled
0 = Dedicated Secondary oscillator circuit disabled

bit 2 **$\overline{\text{TxSYNC}}$:** Timer1/3/5 External Clock Input Synchronization Control bit

TMRxCS<1:0> = 1X
1 = Do not synchronize external clock input
0 = Synchronize external clock input with system clock (FOSC)

TMRxCS<1:0> = 0X
This bit is ignored. Timer1/3/5 uses the internal clock when TMRxCS<1:0> = 1X.

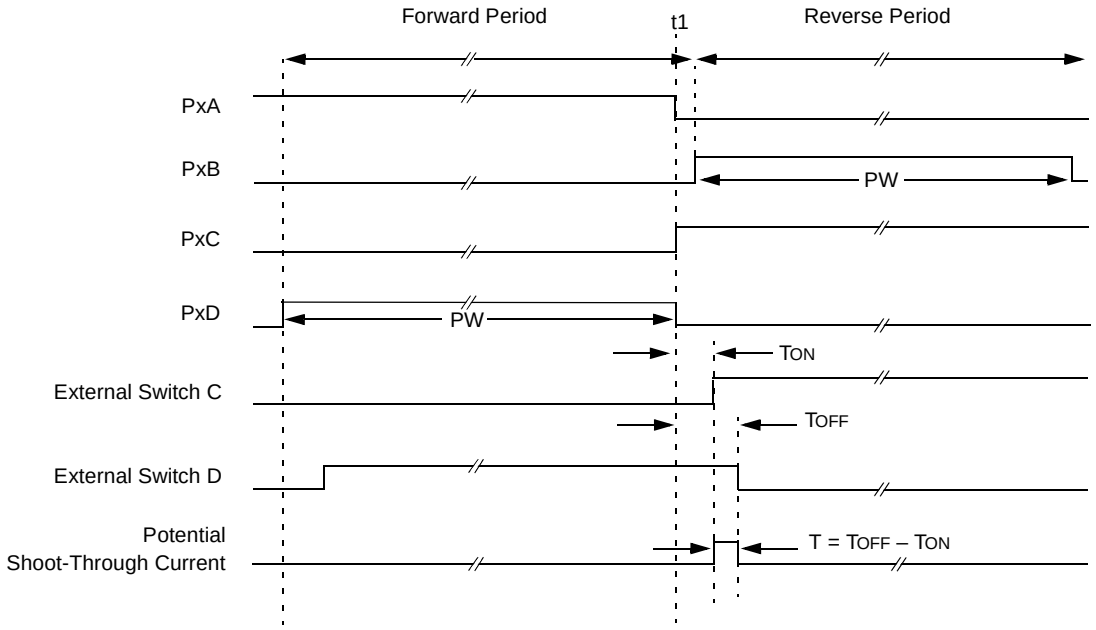
bit 1 **TxRD16:** 16-Bit Read/Write Mode Enable bit

1 = Enables register read/write of Timer1/3/5 in one 16-bit operation
0 = Enables register read/write of Timer1/3/5 in two 8-bit operation

bit 0 **TMRxON:** Timer1/3/5 On bit

1 = Enables Timer1/3/5
0 = Stops Timer1/3/5
Clears Timer1/3/5 Gate flip-flop

FIGURE 14-13: EXAMPLE OF PWM DIRECTION CHANGE AT NEAR 100% DUTY CYCLE



Note 1: All signals are shown as active-high.

2: TON is the turn-on delay of power switch QC and its driver.

3: TOFF is the turn-off delay of power switch QD and its driver.

14.4.3 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the CCPxAS<2:0> bits of the ECCPxAS register. A shutdown event may be generated by:

- A logic '0' on the INT pin
- Comparator Cx (async_CxOUT)
- Setting the CCPxASE bit in firmware

A shutdown condition is indicated by the CCPxASE (Auto-Shutdown Event Status) bit of the ECCPxAS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The CCPxASE bit is set to '1'. The CCPxASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 14.4.4 "Auto-Restart Mode"**).

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [PxA/PxC] and [PxB/PxD].

The state of each pin pair is determined by the PSSxAC<1:0> and PSSxBD<1:0> bits of the ECCPxAS register. Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

Note 1: The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

2: Writing to the CCPxASE bit is disabled while an auto-shutdown condition persists.

3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart), the PWM signal will always restart at the beginning of the next PWM period.

REGISTER 14-5: ECCPxAS: CCPX AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CCPxASE	CCPxAS<2:0>			PSSxAC<1:0>		PSSxBD<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CCPxASE:** CCPx Auto-shutdown Event Status bit
if PxRSEN = 1;
1 = An Auto-shutdown event occurred; CCPxASE bit will automatically clear when event goes away; CCPx outputs in shutdown state
0 = CCPx outputs are operating
if PxRSEN = 0;
1 = An Auto-shutdown event occurred; bit must be cleared in software to restart PWM; CCPx outputs in shutdown state
0 = CCPx outputs are operating

bit 6-4 **CCPxAS<2:0>:** CCPx Auto-Shutdown Source Select bits **(1)**
000 = Auto-shutdown is disabled
001 = Comparator C1 (async_C1OUT) – output high will cause shutdown event
010 = Comparator C2 (async_C2OUT) – output high will cause shutdown event
011 = Either Comparator C1 or C2 – output high will cause shutdown event
100 = FLT0 pin – low level will cause shutdown event
101 = FLT0 pin – low level or Comparator C1 (async_C1OUT) – high level will cause shutdown event
110 = FLT0 pin – low level or Comparator C2 (async_C2OUT) – high level will cause shutdown event
111 = FLT0 pin – low level or Comparators C1 or C2 – high level will cause shutdown event

bit 3-2 **PSSxAC<1:0>:** Pins PxA and PxC Shutdown State Control bits
00 = Drive pins PxA and PxC to '0'
01 = Drive pins PxA and PxC to '1'
1x = Pins PxA and PxC tri-state

bit 1-0 **PSSxBD<1:0>:** Pins PxB and PxD Shutdown State Control bits
00 = Drive pins PxB and PxD to '0'
01 = Drive pins PxB and PxD to '1'
1x = Pins PxB and PxD tri-state

Note 1: If C1SYNC or C2SYNC bits in the CM2CON1 register are enabled, the shutdown will be delayed by Timer1.

FIGURE 15-3: MSSPx BLOCK DIAGRAM (I^2C SLAVE MODE)

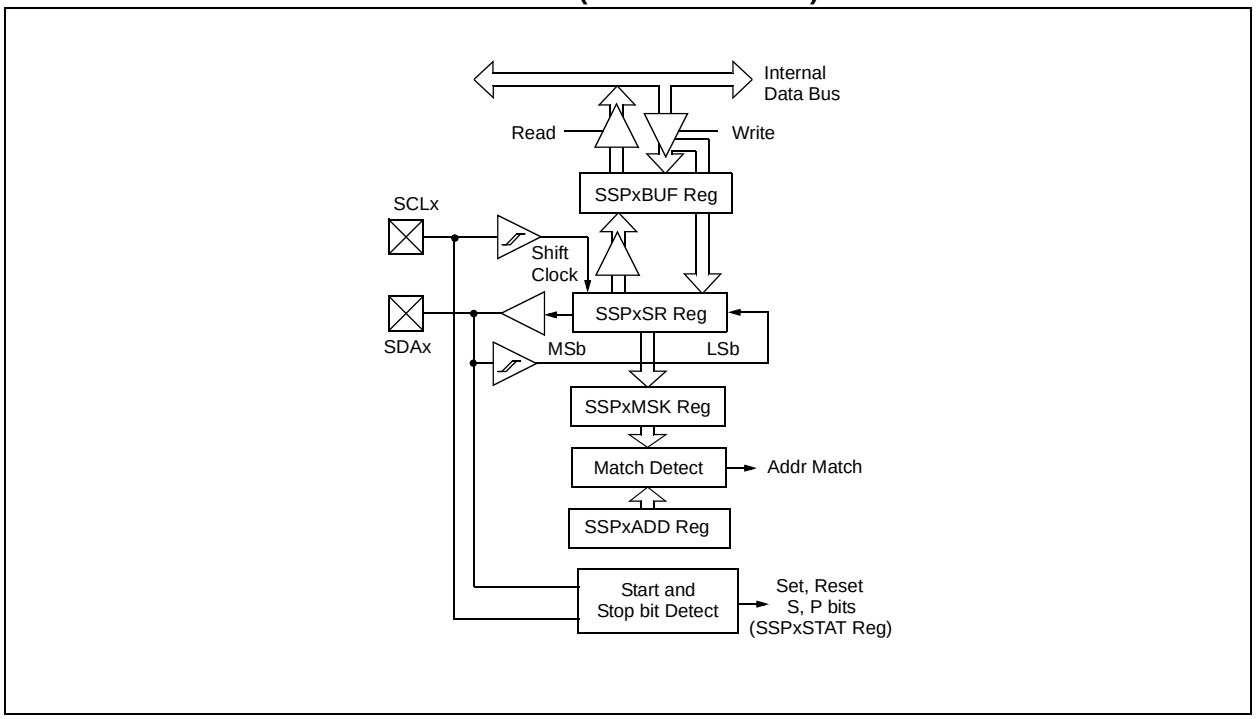


FIGURE 15-19: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)

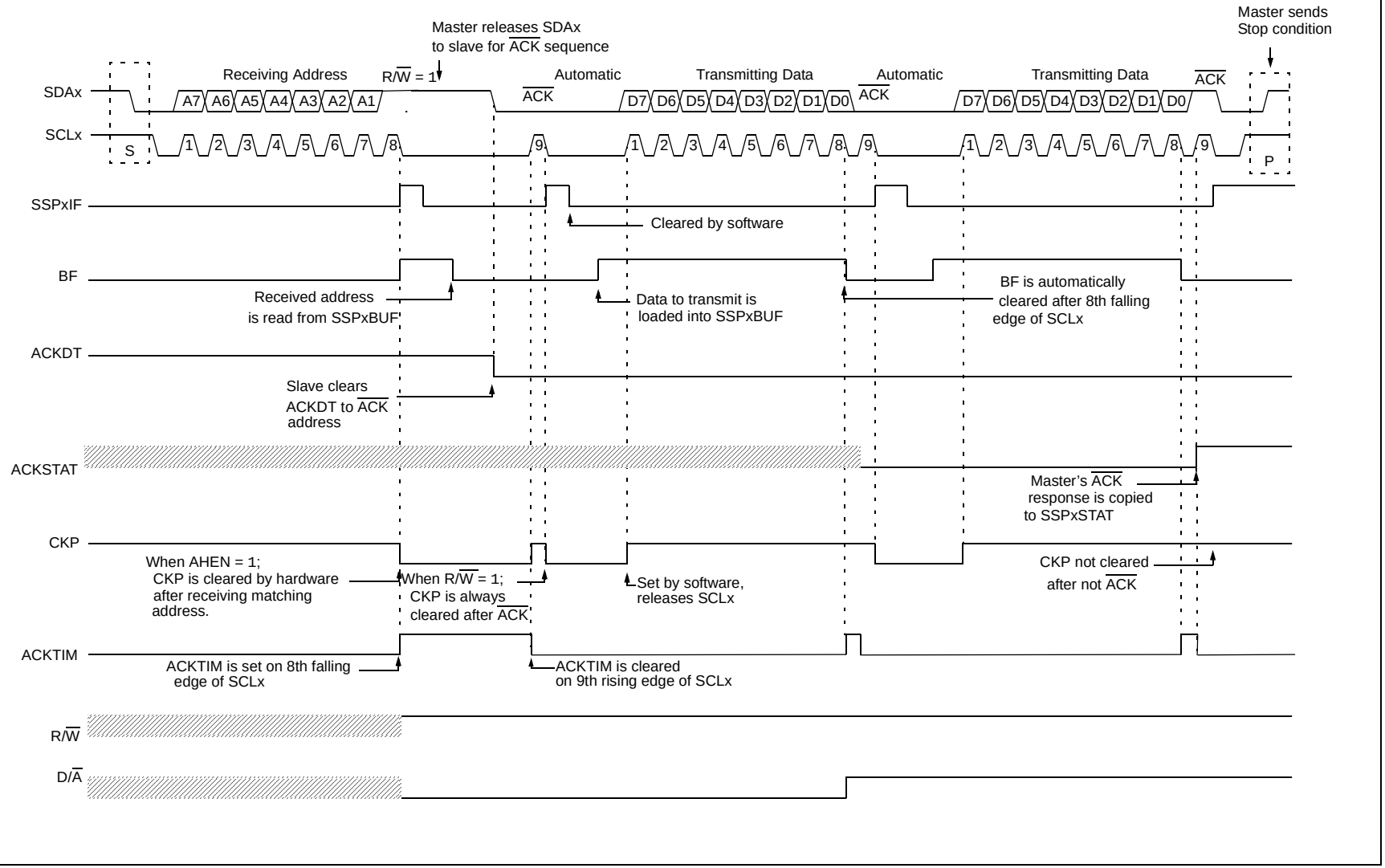


FIGURE 15-29: I^2C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)

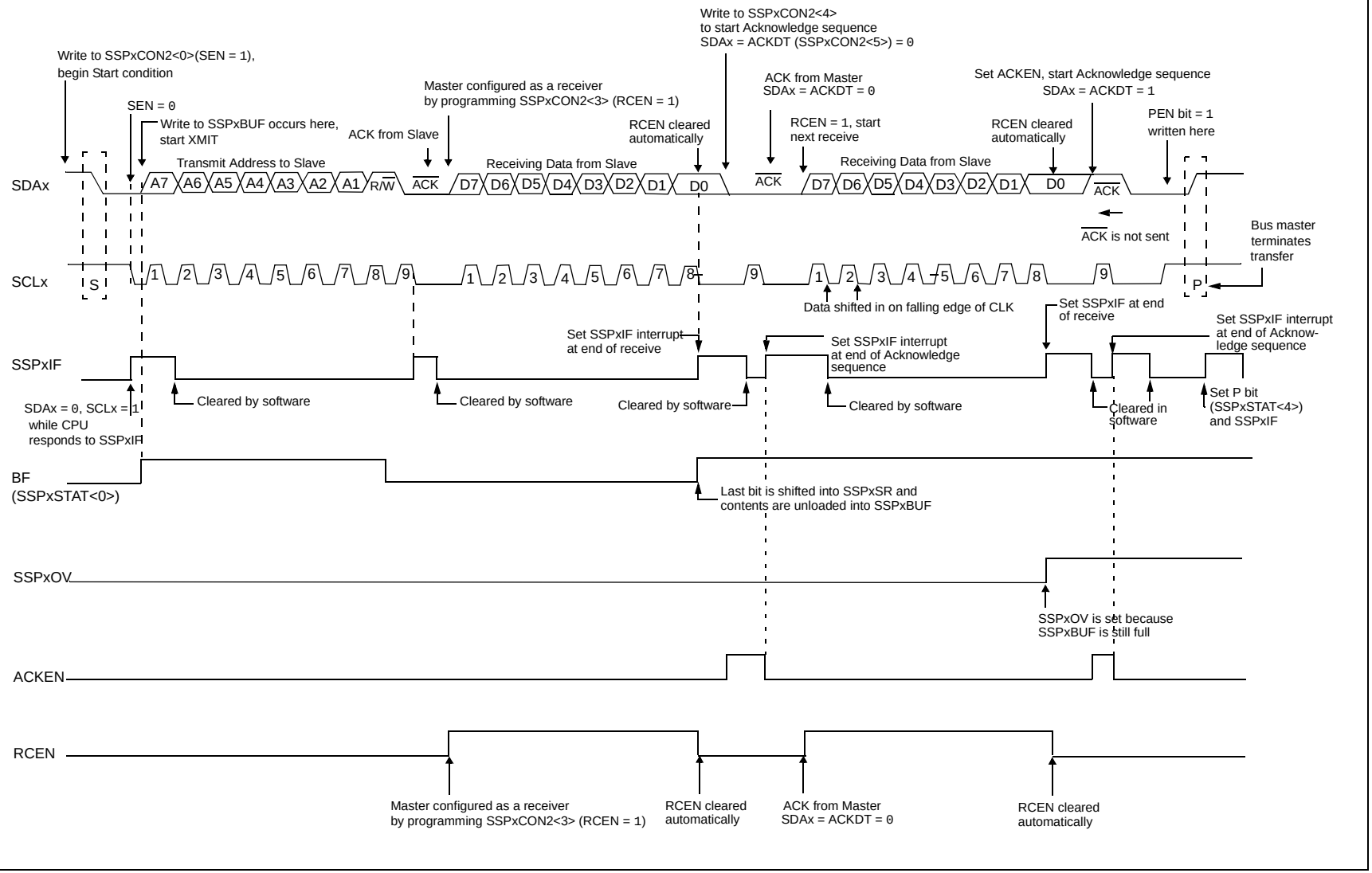
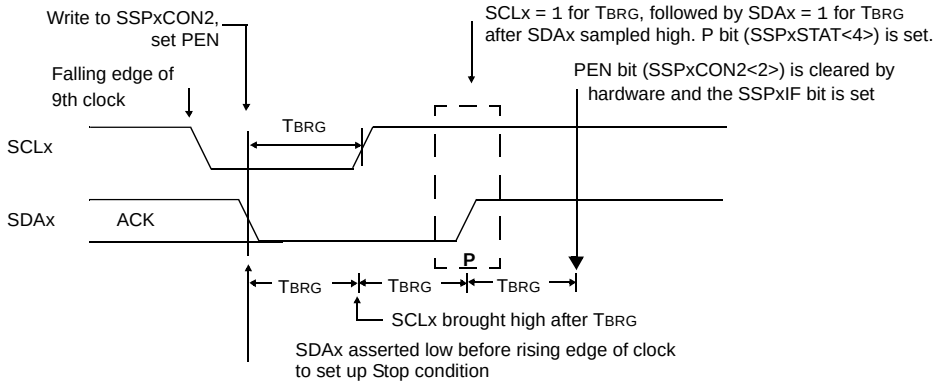


FIGURE 15-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



Note: TBRG = one Baud Rate Generator period.

15.6.10 SLEEP OPERATION

While in Sleep mode, the I^2C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSPx interrupt is enabled).

15.6.11 EFFECTS OF A RESET

A Reset disables the MSSPx module and terminates the current transfer.

15.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSPx module is disabled. Control of the I^2C bus may be taken when the P bit of the SSPxSTAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSPx interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDAx line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCLxIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

16.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

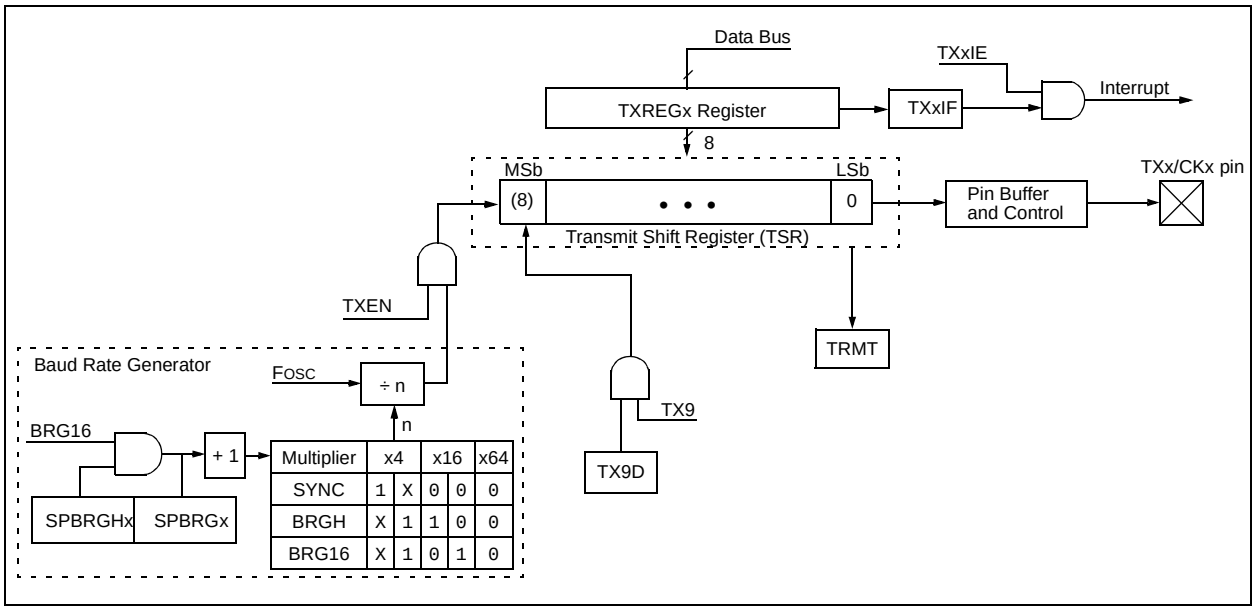
- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock and data polarity

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 16-1 and Figure 16-2.

FIGURE 16-1: EUSART TRANSMIT BLOCK DIAGRAM



16.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode would typically be used in RS-232 systems. The receiver block diagram is shown in Figure 16-2. The data is received on the RXx/DTx pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREGx register.

16.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTAx register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXSTAx register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTAx register enables the EUSART. The RXx/DTx I/O pin must be configured as an input by setting the corresponding TRIS control bit. If the RXx/DTx pin is shared with an analog peripheral the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

16.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See **Section 16.1.2.5 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RCxIF interrupt flag bit of the PIR1/PIR3 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREGx register.

Note:	If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. See **Section 16.1.2.6 "Receive Overrun Error"** for more information on overrun errors.

16.1.2.3 Receive Data Polarity

The polarity of the receive data can be controlled with the DTRXP bit of the BAUDCONx register. The default state of this bit is '0' which selects high true receive idle and data bits. Setting the DTRXP bit to '1' will invert the receive data resulting in low true idle and data bits. The DTRXP bit controls receive data polarity only in Asynchronous mode. In Synchronous mode the DTRXP bit has a different function.

The module uses the edge Status bits to control the current source output to external analog modules (such as the A/D Converter). Current is only supplied to external modules when only one (but not both) of the Status bits is set, and shuts current off when both bits are either set or cleared. This allows the CTMU to measure current only during the interval between edges. After both Status bits are set, it is necessary to clear them before another measurement is taken. Both bits should be cleared simultaneously, if possible, to avoid re-enabling the CTMU current source.

In addition to being set by the CTMU hardware, the edge Status bits can also be set by software. This is also the user's application to manually enable or disable the current source. Setting either one (but not both) of the bits enables the current source. Setting or clearing both bits at once disables the source.

19.1.5 INTERRUPTS

The CTMU sets its interrupt flag (PIR3<2>) whenever the current source is enabled, then disabled. An interrupt is generated only if the corresponding interrupt enable bit (PIE3<2>) is also set. If edge sequencing is not enabled (i.e., Edge 1 must occur before Edge 2), it is necessary to monitor the edge Status bits and determine which edge occurred last and caused the interrupt.

19.2 CTMU Module Initialization

The following sequence is a general guideline used to initialize the CTMU module:

1. Select the current source range using the IRNG bits (CTMUICON<1:0>).
2. Adjust the current source trim using the ITRIM bits (CTMUICON<7:2>).
3. Configure the edge input sources for Edge 1 and Edge 2 by setting the EDG1SEL and EDG2SEL bits (CTMUCONL<3:2 and 6:5>).
4. Configure the input polarities for the edge inputs using the EDG1POL and EDG2POL bits (CTMUCONL<4,7>). The default configuration is for negative edge polarity (high-to-low transitions).
5. Enable edge sequencing using the EDGSEQEN bit (CTMUCONH<2>). By default, edge sequencing is disabled.
6. Select the operating mode (Measurement or Time Delay) with the TGEN bit. The default mode is Time/Capacitance Measurement.
7. Discharge the connected circuit by setting the IDISSEN bit (CTMUCONH<1>); after waiting a sufficient time for the circuit to discharge, clear IDISSEN.
8. Disable the module by clearing the CTMUEN bit (CTMUCONH<7>).
9. Enable the module by setting the CTMUEN bit.
10. Clear the Edge Status bits: EDG2STAT and EDG1STAT (CTMUCONL<1:0>).
11. Enable both edge inputs by setting the EDGEN bit (CTMUCONH<3>).

Depending on the type of measurement or pulse generation being performed, one or more additional modules may also need to be initialized and configured with the CTMU module:

- Edge Source Generation: In addition to the external edge input pins, both Timer1 and the Output Compare/PWM1 module can be used as edge sources for the CTMU.
- Capacitance or Time Measurement: The CTMU module uses the A/D Converter to measure the voltage across a capacitor that is connected to one of the analog input channels.
- Pulse Generation: When generating system clock independent output pulses, the CTMU module uses Comparator 2 and the associated comparator voltage reference.

27.1 DC Characteristics: Supply Voltage, PIC18(L)F2X/4XK22

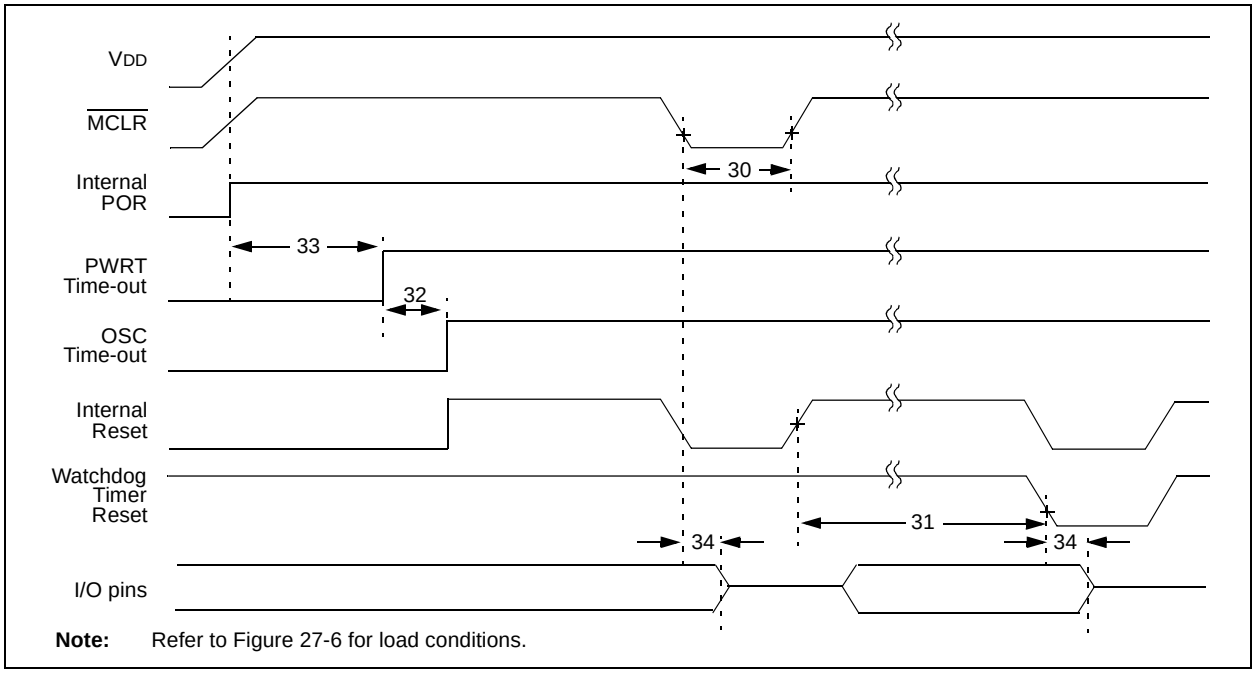
PIC18(L)F2X/4XK22				Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**	PIC18LF2X/4XK22	1.8	—	3.6	V	
			PIC18F2X/4XK22	2.3	—	5.5	V	
D002	VDR	**RAM Data Retention Voltage(1)**		1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal		—	—	0.7	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal		0.05	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	**Brown-out Reset Voltage**						
		BORV<1:0> = 11(2)		1.75	1.9	2.05	V	
		BORV<1:0> = 10		2.05	2.2	2.35	V	
		BORV<1:0> = 01		2.35	2.5	2.65	V	
		BORV<1:0> = 00(3)		2.65	2.85	3.05	V	

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: On PIC18(L)F2X/4XK22 devices with BOR enabled, operation is supported until a BOR occurs. This is valid although VDD may be below the minimum rated supply voltage.

3: With BOR enabled, full-speed operation (FOSC = 64 MHz or 48 MHz) is supported until a BOR occurs. This is valid although VDD may be below the minimum voltage for this frequency.

FIGURE 27-9: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note: Refer to Figure 27-6 for load conditions.

FIGURE 27-10: BROWN-OUT RESET TIMING

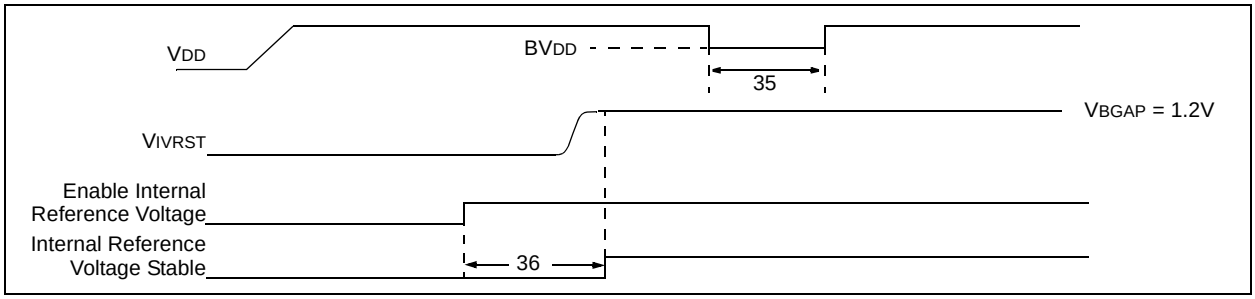


FIGURE 27-15: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)

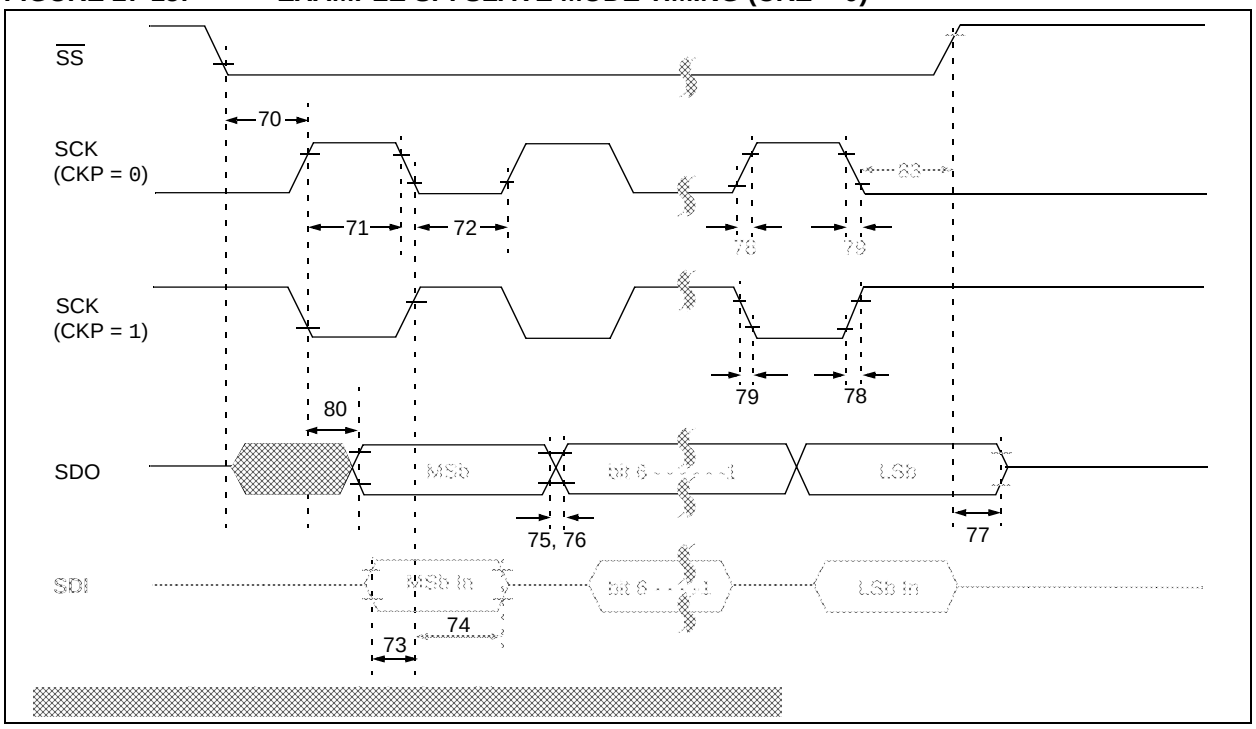


FIGURE 27-16: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)

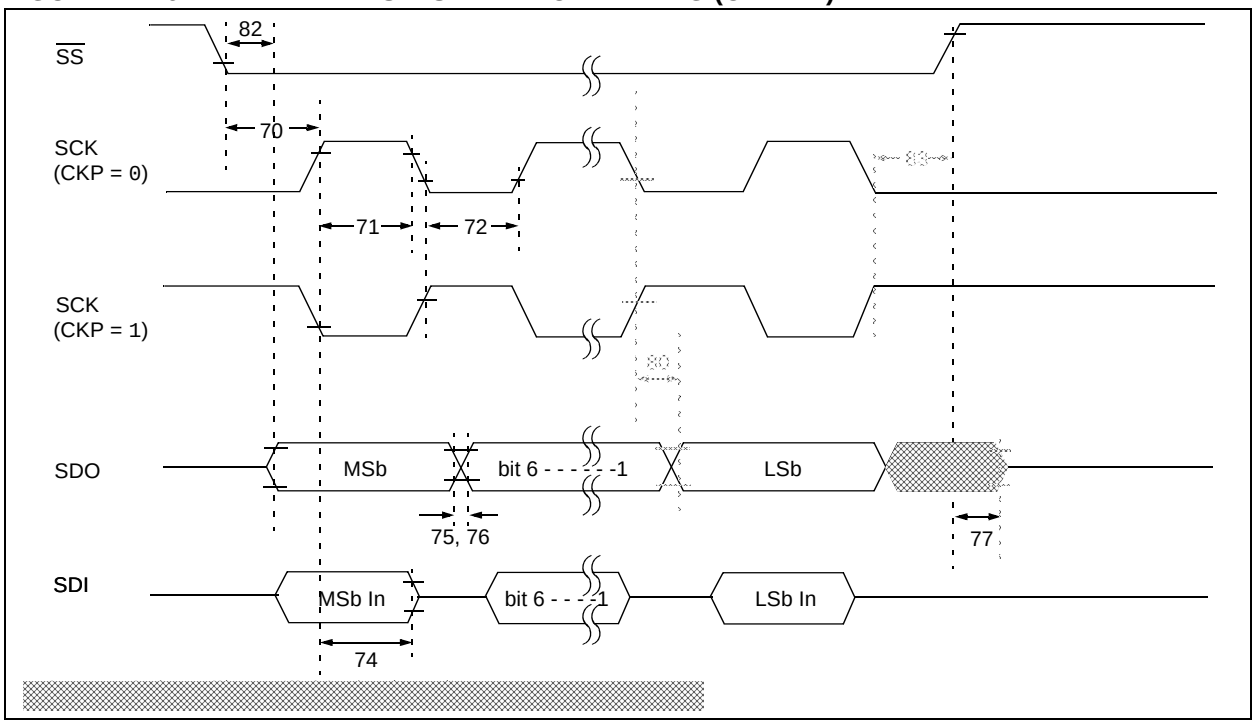


FIGURE 28-5: PIC18LF2X/4XK22 DELTA IPD BROWN-OUT RESET (BOR)

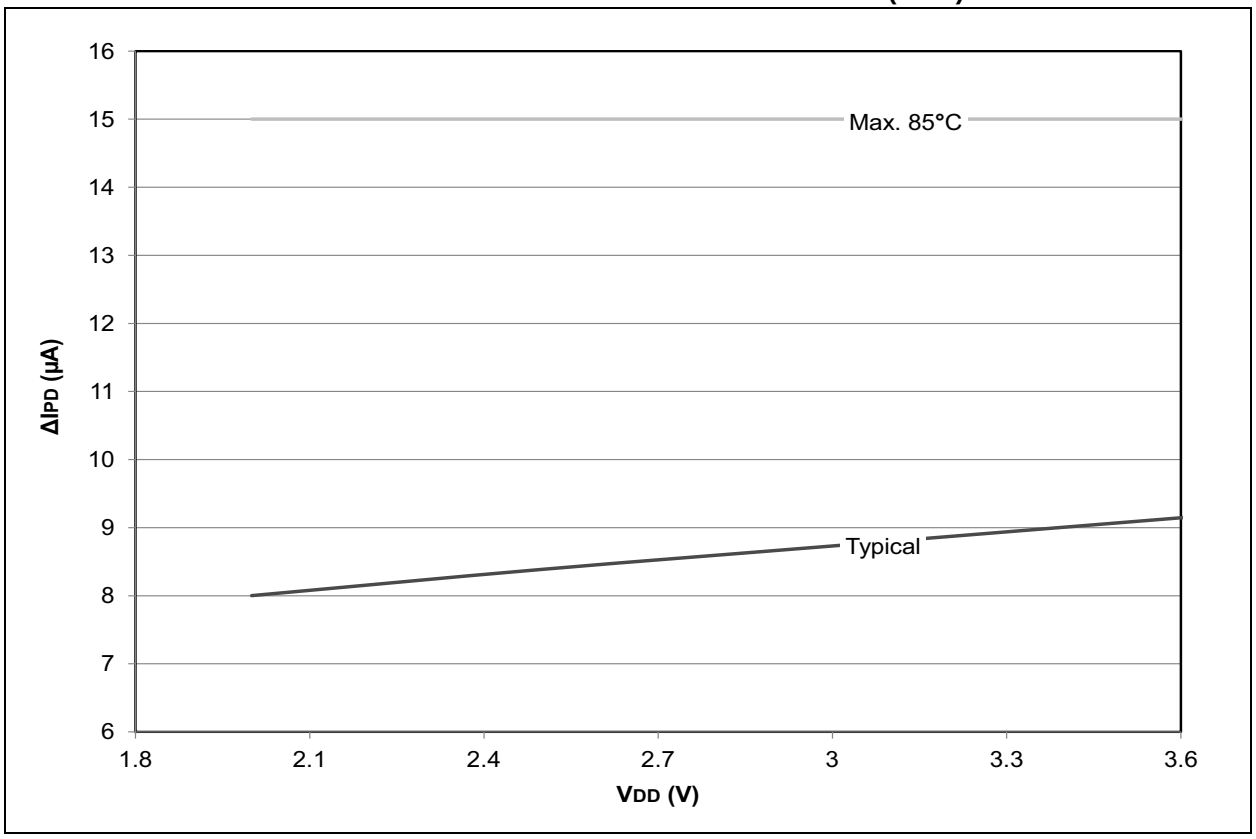


FIGURE 28-6: PIC18F2X/4XK22 DELTA IPD BROWN-OUT RESET (BOR)

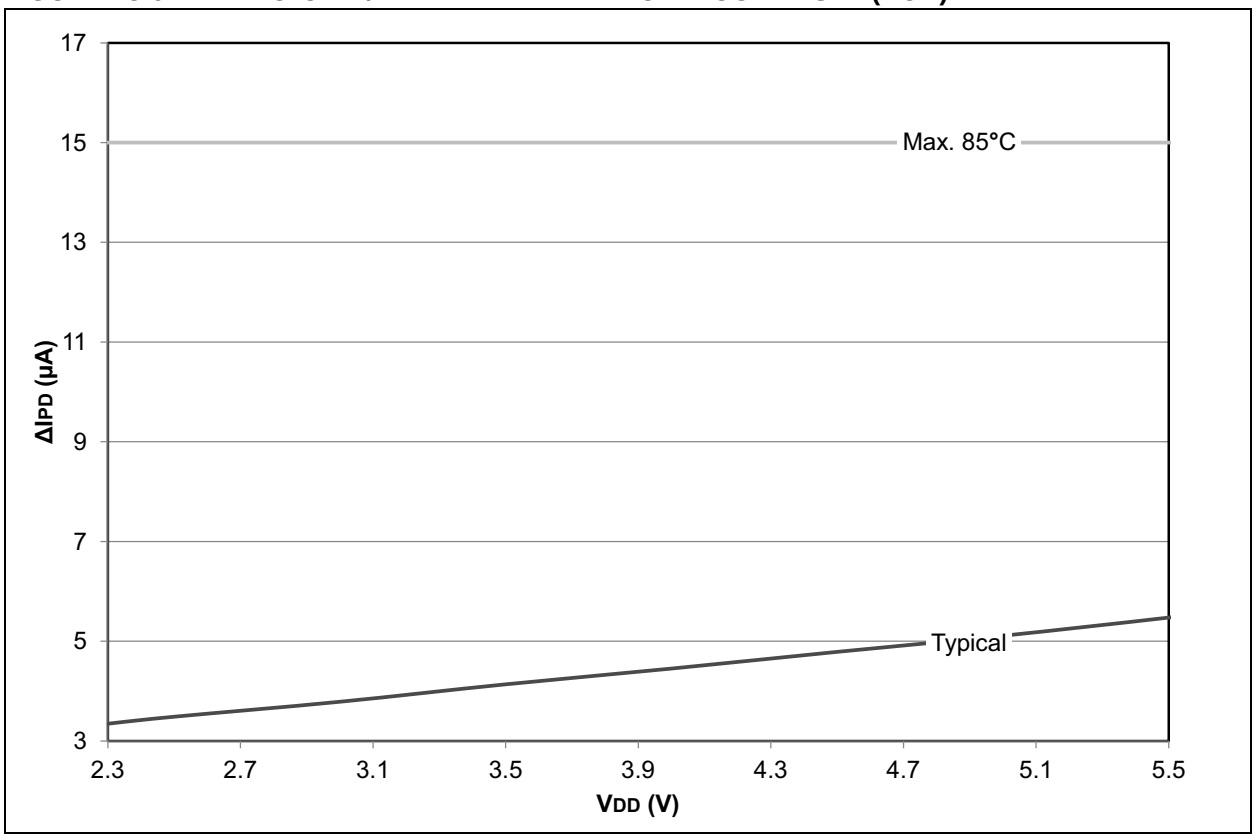


FIGURE 28-66: PIC18F2X/4XK22 TYPICAL IDD: PRI_IDLE EC HIGH POWER

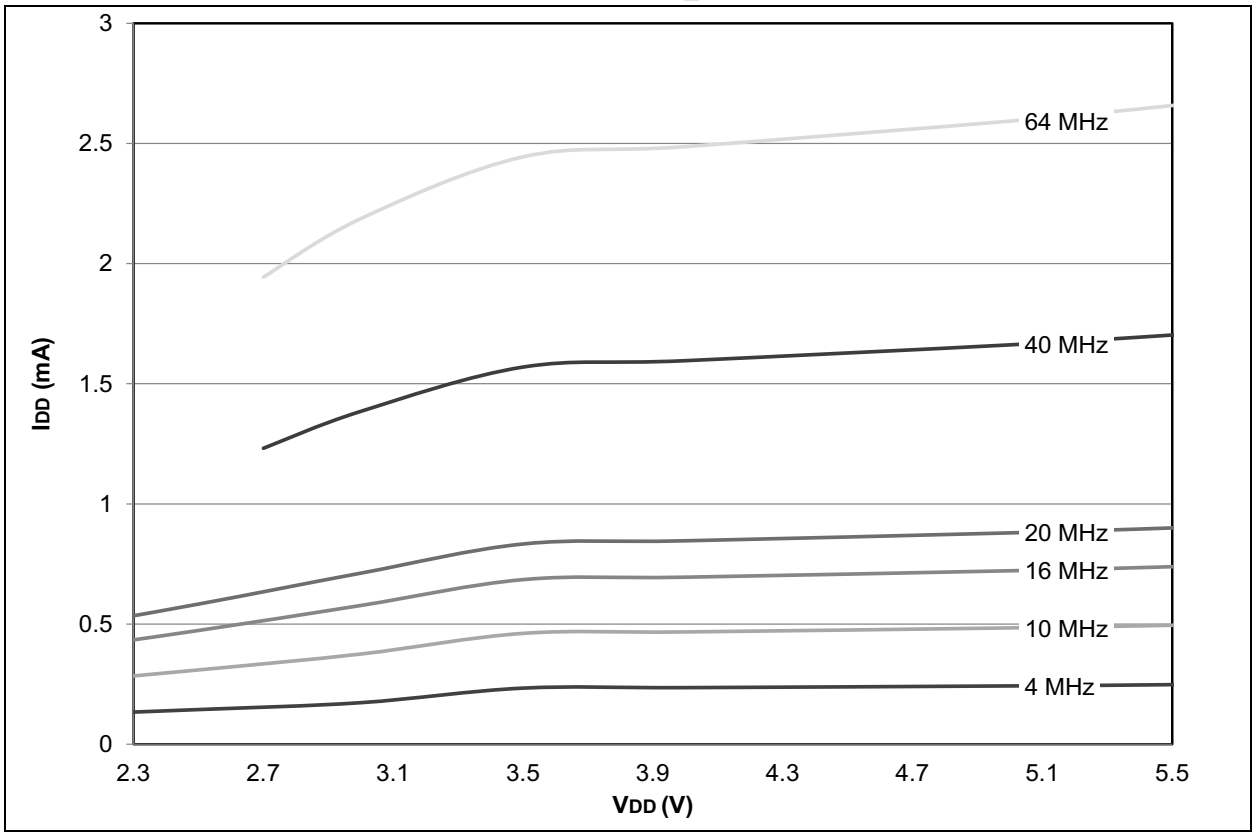


FIGURE 28-67: PIC18F2X/4XK22 MAXIMUM IDD: PRI_IDLE EC HIGH POWER

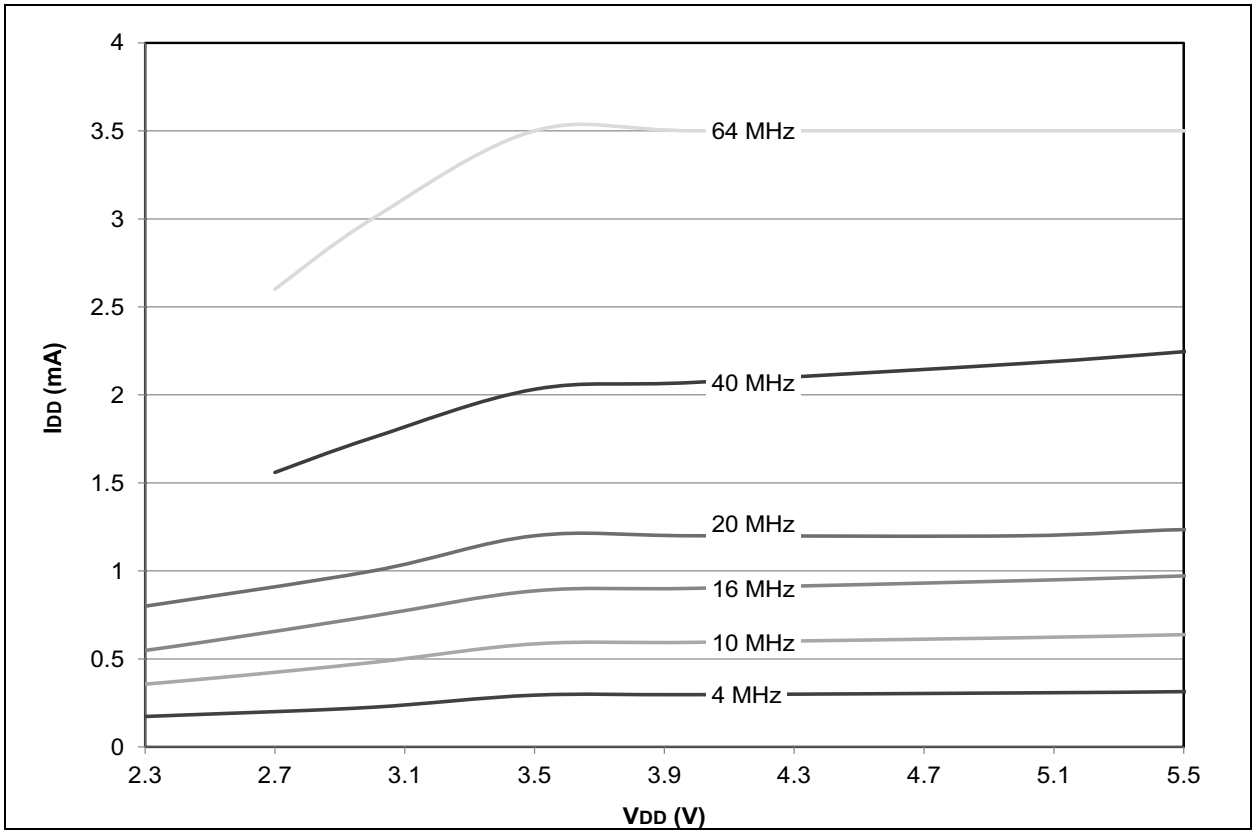
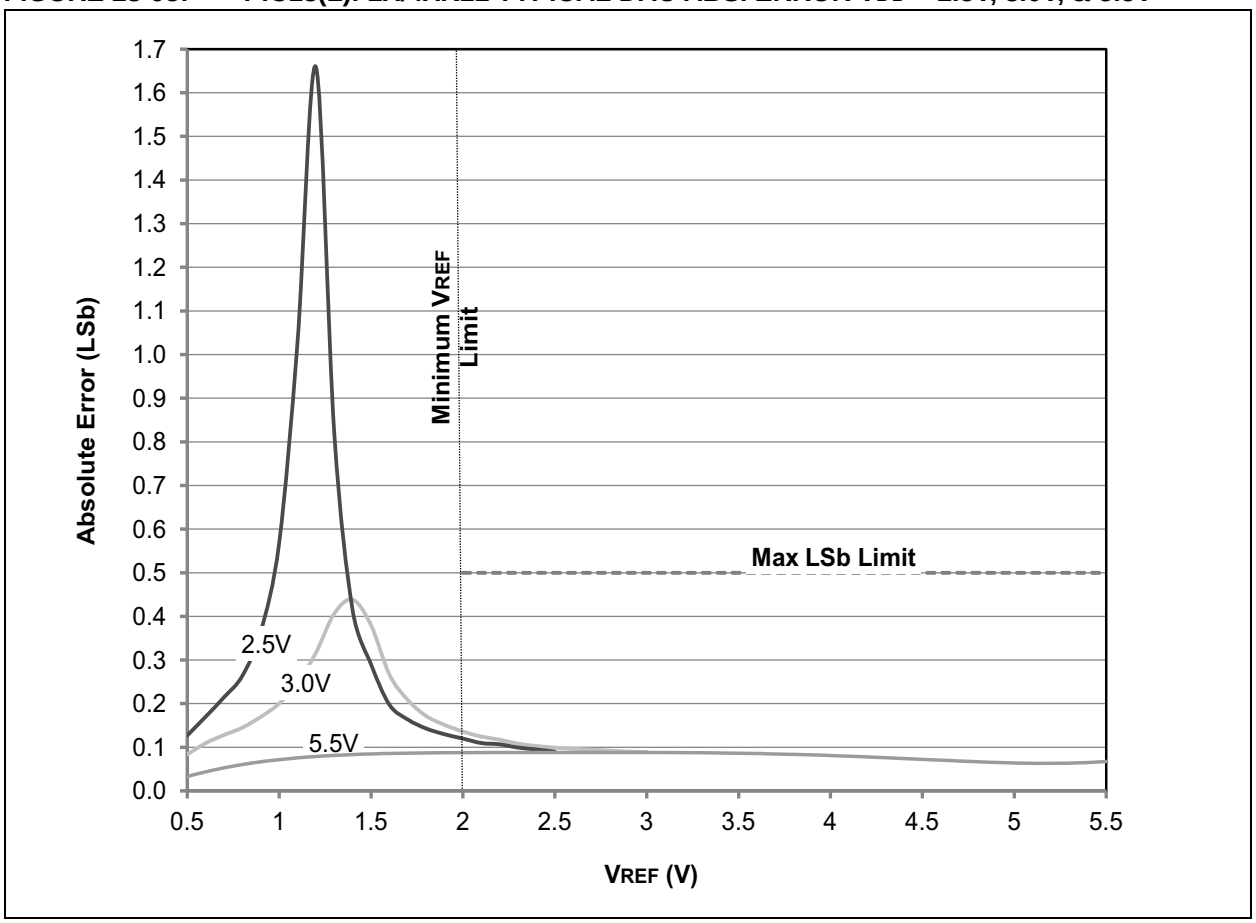
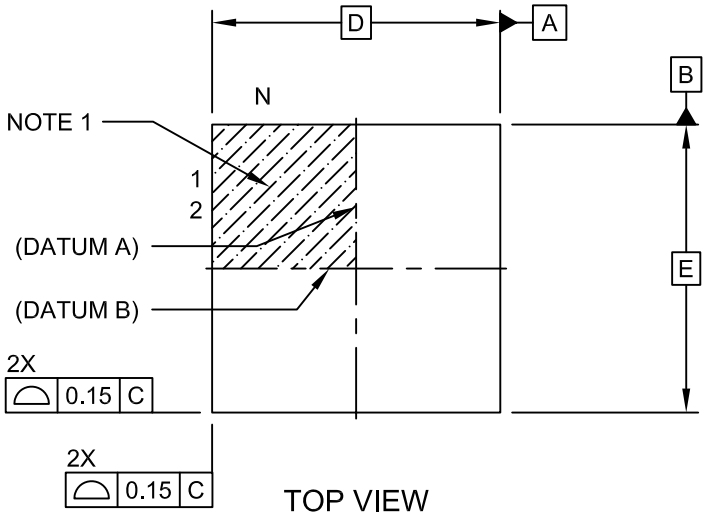


FIGURE 28-93: PIC18(L)F2X/4XK22 TYPICAL DAC ABS. ERROR V_{DD} = 2.5V, 3.0V, & 5.5V

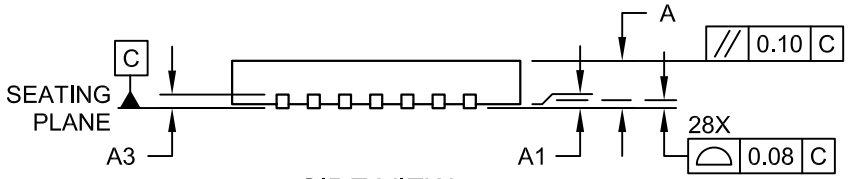


28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

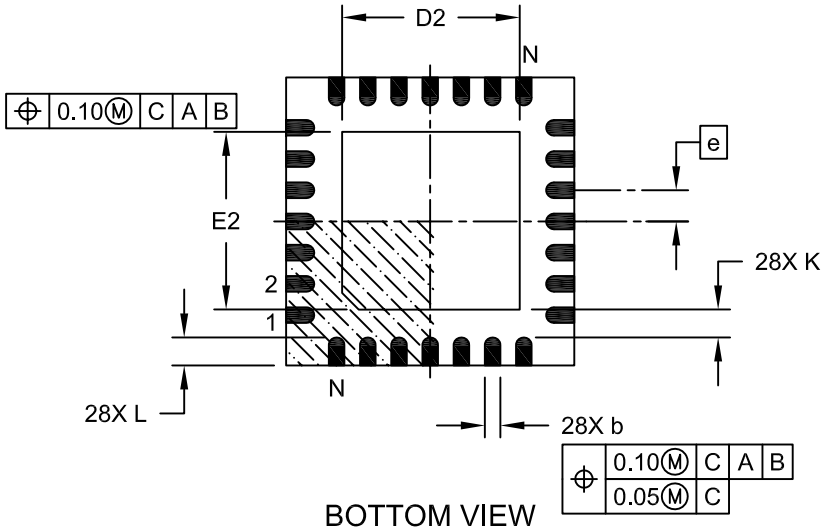
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Microchip Technology Drawing C04-105C Sheet 1 of 2

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features[1]	PIC18F23K22 PIC18LF23K22	PIC18F24K22 PIC18LF24K22	PIC18F25K22 PIC18LF25K22	PIC18F26K22 PIC18LF26K22	PIC18F43K22 PIC18LF43K22	PIC18F44K22 PIC18LF44K22	PIC18F45K22 PIC18LF45K22	PIC18F46K22 PIC18LF46K22
Program Memory (Bytes)	8192	16384	32768	65536	8192	16384	32768	65536
SRAM (Bytes)	512	768	1536	3896	512	768	1536	3896
EEPROM (Bytes)	256	256	256	1024	256	256	256	1024
Interrupt Sources	26	26	33	33	26	26	33	33
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules (CCP)	2	2	2	2	2	2	2	2
Enhanced CCP Modules (ECCP) Full Bridge	1	1	1	1	2	2	2	2
ECCP Module Half Bridge	2	2	2	2	1	1	1	1
10-bit Analog-to-Digital Module	17 input channels	17 input channels	17 input channels	17 input channels	28 input channels	28 input channels	28 input channels	28 input channels
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN

Note 1: PIC18FXXK22: operating voltage, 2.3V-5.5V.

PIC18LFXXK22: operating voltage, 1.8V-3.6V.