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Details

EXF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf25k22-i-ml

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2.9 Effects of Power-Managed Modes on the Various Clock Sources

For more information about the modes discussed in this section see **Section 3.0** "**Power-Managed Modes**". A quick reference list is also available in Table 3-1.

When PRI_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin, if used by the oscillator) will stop oscillating.

In secondary clock modes (SEC_RUN and SEC_IDLE), the secondary oscillator (SOSC) is operating and providing the device clock. The secondary oscillator may also run in all power-managed modes if required to clock Timer1, Timer3 or Timer5.

In internal oscillator modes (INTOSC_RUN and INTOSC_IDLE), the internal oscillator block provides the device clock source. The 31.25 kHz LFINTOSC output can be used directly to provide the clock and may be enabled to support various special features, regardless of the power-managed mode (see Section 24.3 "Watchdog Timer (WDT)", Section 2.12 "Two-Speed Clock Start-up Mode" and Section 2.13 "Fail-Safe Clock Monitor" for more information on WDT, Fail-Safe Clock Monitor and Two-Speed Start-up). The HFINTOSC and MFINTOSC outputs may be used directly to clock the device or may be divided down by the postscaler. The HFINTOSC and MFINTOSC outputs are disabled when the clock is provided directly from the LFINTOSC output.

When the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The LFINTOSC is required to support WDT operation. Other features may be operating that do not require a device clock source (i.e., SSP slave, PSP, INTn pins and others). Peripherals that may add significant current consumption are listed in Section 27.8 "DC Characteristics: Input/Output Characteristics, PIC18(L)F2X/4XK22".

2.10 Power-up Delays

Power-up delays are controlled by two timers, so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 4.6** "**Device Reset Timers**".

The first timer is the Power-up Timer (PWRT), which provides a fixed delay on power-up. It is enabled by clearing (= 0) the PWRTEN Configuration bit.

The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable (LP, XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the PLL is enabled with external oscillator modes, the device is kept in Reset for an additional 2 ms, following the OST delay, so the PLL can lock to the incoming clock frequency.

There is a delay of interval TCSD, following POR, while the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC, RC or INTIOSC modes are used as the primary clock source.

When the HFINTOSC is selected as the primary clock, the main system clock can be delayed until the HFINTOSC is stable. This is user selectable by the HFOFST bit of the CONFIG3H Configuration register. When the HFOFST bit is cleared, the main system clock is delayed until the HFINTOSC is stable. When the HFOFST bit is set, the main system clock starts immediately.

In either case, the HFIOFS bit of the OSCCON register can be read to determine whether the HFINTOSC is operating and stable.

IRCF<2:0>	INTSRC	MFIOSEL	Selected Oscillator	Selected Oscillator Stable when:
000	0	x	LFINTOSC	LFIOFS = 1
000	1	0	HFINTOSC	HFIOFS = 1
000	1	1	MFINTOSC	MFIOFS = 1
010 or 001	x	0	HFINTOSC	HFIOFS = 1
010 or 001	x	1	MFINTOSC	MFIOFS = 1
011 - 111	x	x	HFINTOSC	HFIOFS = 1

TABLE 3-2: INTERNAL OSCILLATOR FREQUENCY STABILITY BITS







3.4.1 PRI_IDLE MODE

This mode is unique among the three low-power Idle modes, in that it does not disable the primary device clock. For timing sensitive applications, this allows for the fastest resumption of device operation with its more accurate primary clock source, since the clock source does not have to "warm-up" or transition from another oscillator.

PRI_IDLE mode is entered from PRI_RUN mode by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set IDLEN first, then clear the SCS bits and execute SLEEP. Although the CPU is disabled, the peripherals continue to be clocked from the primary clock source specified by the FOSC<3:0> Configuration bits. The OSTS bit remains set (see Figure 3-6).

When a wake event occurs, the CPU is clocked from the primary clock source. A delay of interval TCSD is required between the wake event and when code execution starts. This is required to allow the CPU to become ready to execute instructions. After the wake-up, the OSTS bit remains set. The IDLEN and SCS bits are not affected by the wake-up (see Figure 3-7).

3.4.2 SEC_IDLE MODE

In SEC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the SOSC oscillator. This mode is entered from SEC_RUN by setting the IDLEN bit and executing a SLEEP instruction. If the device is in another Run mode, set the IDLEN bit first, then set the SCS<1:0> bits to '01' and execute SLEEP. When the clock source is switched to the SOSC oscillator, the primary oscillator is shut down, the OSTS bit is cleared and the SOSCRUN bit is set.

When a wake event occurs, the peripherals continue to be clocked from the SOSC oscillator. After an interval of TCSD following the wake event, the CPU begins executing code being clocked by the SOSC oscillator. The IDLEN and SCS bits are not affected by the wake-up; the SOSC oscillator continues to run (see Figure 3-7).

Note: The SOSC oscillator should already be running prior to entering SEC_IDLE mode. At least one of the secondary oscillator enable bits (SOSCGO, T1SOSCEN, T3SOSCEN or T5SOSCEN) must be set when the SLEEP instruction is executed. Otherwise, the main system clock will continue to operate in the previously selected mode and the corresponding IDLE mode will be entered (i.e., PRI_IDLE or RC_IDLE).



The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack (TOS) Special File Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL type instruction causes a push onto the stack; the Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack; the contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

The Stack Pointer is initialized to '00000' after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of '00000'; this is only a Reset value. Status bits indicate if the stack is full or has overflowed or has underflowed.

5.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 5-2). This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the Global Interrupt Enable (GIE) bits while accessing the stack to prevent inadvertent stack corruption.



FIGURE 5-2: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS

5.1.2.2 Return Stack Pointer (STKPTR)

The STKPTR register (Register 5-1) contains the Stack Pointer value, the STKFUL (stack full) Status bit and the STKUNF (Stack Underflow) Status bits. The value of the Stack Pointer can be 0 through 31. The Stack Pointer increments before values are pushed onto the stack and decrements after values are popped off the stack. On Reset, the Stack Pointer value will be zero. The user may read and write the Stack Pointer value. This feature can be used by a Real-Time Operating System (RTOS) for return stack maintenance.

After the PC is pushed onto the stack 31 times (without popping any values off the stack), the STKFUL bit is set. The STKFUL bit is cleared by software or by a POR.

The action that takes place when the stack becomes full depends on the state of the STVREN (Stack Overflow Reset Enable) Configuration bit. (Refer to **Section 24.1 "Configuration Bits"** for a description of the device Configuration bits.) If STVREN is set (default), the 31st push will push the (PC + 2) value onto the stack, set the STKFUL bit and reset the device. The STKFUL bit will remain set and the Stack Pointer will be set to zero.

If STVREN is cleared, the STKFUL bit will be set on the 31st push and the Stack Pointer will increment to 31. Any additional pushes will not overwrite the 31st push and STKPTR will remain at 31.

When the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC and sets the STKUNF bit, while the Stack Pointer remains at zero. The STKUNF bit will remain set until cleared by software or until a POR occurs.

Note: Returning a value of zero to the PC on an underflow has the effect of vectoring the program to the Reset vector, where the stack conditions can be verified and appropriate actions can be taken. This is not the same as a Reset, as the contents of the SFRs are not affected.

Pin	Function	TRIS Setting	ANSEL Setting	Pin Type	Buffer Type	Description
RB6/KBI2/PGC	RB6	0		0	DIG	LATB<6> data output; not affected by analog input.
		1	_	Ι	TTL	PORTB<6> data input; disabled when analog input enabled.
	IOC2	1	_	I	TTL	Interrupt-on-change pin.
	TX2 ⁽³⁾	1	_	0	DIG	EUSART asynchronous transmit data output.
	CK2 ⁽³⁾	1	_	0	DIG	EUSART synchronous serial clock output.
		1	_	I	ST	EUSART synchronous serial clock input.
	PGC	x	_	I	ST	In-Circuit Debugger and ICSP [™] programming clock input.
RB7/KBI3/PGD	RB7	0		0	DIG	LATB<7> data output; not affected by analog input.
		1	—	Ι	TTL	PORTB<7> data input; disabled when analog input enabled.
	IOC3	1	—	I	TTL	Interrupt-on-change pin.
	RX2 ^{(2), (3)}	1	—	I	ST	EUSART asynchronous receive data input.
	DT2 ^{(2), (3)}	1		0	DIG	EUSART synchronous serial data output.
		1	_	I	ST	EUSART synchronous serial data input.
	PGD	x	—	0	DIG	In-Circuit Debugger and ICSP [™] programming data output.
		x		I	ST	In-Circuit Debugger and ICSP [™] programming data input.

TABLE 10-5: PORTB I/O SUMMARY (CONTINUED)

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C .

Note 1: Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

3: Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

TABLE 10-8: PORTC I/O SUMMARY

Pin Name	Function	TRIS Setting	ANSEL setting	Pin Type	Buffer Type	Description
RC0/P2B/T3CKI/T3G/	RC0	0	—	0	DIG	LATC<0> data output; not affected by analog input.
T1CKI/SOSCO		1	—	Ι	ST	PORTC<0> data input; disabled when analog input enabled.
	P2B ⁽²⁾	0	—	0	DIG	Enhanced CCP2 PWM output 2.
	T3CKI ⁽¹⁾	1	_	Ι	ST	Timer3 clock input.
	T3G	1	_	Ι	ST	Timer3 external clock gate input.
	T1CKI	1	_	I	ST	Timer1 clock input.
	SOSCO	х	_	0	XTAL	Secondary oscillator output.
RC1/P2A/CCP2/SOSCI	RC1	0	_	0	DIG	LATC<1> data output; not affected by analog input.
		1		Ι	ST	PORTC<1> data input; disabled when analog input enabled.
	P2A	0	_	0	DIG	Enhanced CCP2 PWM output 1.
	CCP2 ⁽¹⁾	0	_	0	DIG	Compare 2 output/PWM 2 output.
		1	_	Ι	ST	Capture 2 input.
	SOSCI	х	_	Ι	XTAL	Secondary oscillator input.
RC2/CTPLS/P1A/	RC2	0	0	0	DIG	LATC<2> data output; not affected by analog input.
CCP1/T5CKI/AN14		1	0	Ι	ST	PORTC<2> data input; disabled when analog input enabled.
	CTPLS	0	0	0	DIG	CTMU pulse generator output.
	P1A	0	0	0	DIG	Enhanced CCP1 PWM output 1.
	CCP1	0	0	0	DIG	Compare 1 output/PWM 1 output.
		1	0	I	ST	Capture 1 input.
	T5CKI	1	0	Ι	ST	Timer5 clock input.
	AN14	1	1	Ι	AN	Analog input 14.
RC3/SCK1/SCL1/AN15	RC3	0	0	0	DIG	LATC<3> data output; not affected by analog input.
		1	0	Ι	ST	PORTC<3> data input; disabled when analog input enabled.
	SCK1	0	0	0	DIG	MSSP1 SPI Clock output.
		1	0	Ι	ST	MSSP1 SPI Clock input.
	SCL1	0	0	0	DIG	MSSP1 I ² C Clock output.
		1	0	I	l ² C	MSSP1 I ² C Clock input.
	AN15	1	1	Ι	AN	Analog input 15.
RC4/SDI1/SDA1/AN16	RC4	0	0	0	DIG	LATC<4> data output; not affected by analog input.
		1	0	Ι	ST	PORTC<4> data input; disabled when analog input enabled.
	SDI1	1	0	I	ST	MSSP1 SPI data input.
	SDA1	0	0	0	DIG	MSSP1 I ² C data output.
		1	0	I	I ² C	MSSP1 I ² C data input.
	AN16	1	1	I	AN	Analog input 16.

Legend: AN = Analog input or output; TTL = TTL compatible input; $HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; <math>I^2C$ = Schmitt Trigger input with I^2C .

Note 1: Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

3: Function on PORTD and PORTE for PIC18(L)F4XK22 devices.

FIGURE 11-2: TIMER0 BLOCK DIAGRAM (16-BIT MODE)



11.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not directly readable or writable; its value is set by the PSA and T0PS<2:0> bits of the T0CON register which determine the prescaler assignment and prescale ratio.

Clearing the PSA bit assigns the prescaler to the Timer0 module. When the prescaler is assigned, prescale values from 1:2 through 1:256 in integer power-of-2 increments are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF TMR0, MOVWF TMR0, BSF TMR0, etc.) clear the prescaler count.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count but will not change the prescaler assignment.

11.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control and can be changed "on-the-fly" during program execution.

11.5 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or from FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF flag bit. The interrupt can be masked by clearing the TMR0IE bit of the INTCON register. Before re-enabling the interrupt, the TMR0IF bit must be cleared by software in the Interrupt Service Routine.

Since Timer0 is shut down in Sleep mode, the TMR0 interrupt cannot awaken the processor from Sleep.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	109
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2		TMR0IP		RBIP	110
T0CON	TMR0ON T08BIT T0CS T0SE PSA T0PS<2:0>								154
TMR0H	Timer0 Register, High Byte								—
TMR0L	Timer0 Register, Low Byte								_
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	151

TABLE 11-1: REGISTERS ASSOCIATED WITH TIMER0

Legend: — = unimplemented locations, read as '0'. Shaded bits are not used by Timer0.

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	R/W-0/u	R/W-0/u			
TMRxGE	TxGPOL	TxGTM	TxGSPM	TxGGO/DONE	TxGVAL	TxGSS	6<1:0>			
bit 7	·						bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplemer	nted bit, read a	as '0'				
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value at POR and BOR/Value at all other Resets						
'1' = Bit is set		'0' = Bit is cle	ared	HC = Bit is cleared by hardware						
bit 7 TMRxGE: Timer1/3/5 Gate Enable bit <u>If TMRxON = 0</u> : This bit is ignored <u>If TMRxON = 1</u> : 1 = Timer1/3/5 counting is controlled by the Timer1/3/5 gate function 0 = Timer1/3/5 counts regardless of Timer1/3/5 gate function bit 6 TxGPOL: Timer1/3/5 Gate Polarity bit										
bit 6	it 6 TxGPOL: Timer1/3/5 Gate Polarity bit 1 = Timer1/3/5 gate is active-high (Timer1/3/5 counts when gate is high) 0 = Timer1/3/5 gate is active-low (Timer1/3/5 counts when gate is low)									
bit 5	TxGTM: Time 1 = Timer1/3 0 = Timer1/3 Timer1/3/5 ga	er1/3/5 Gate To /5 Gate Toggle /5 Gate Toggle ate flip-flop togg	ggle Mode bit mode is enab mode is disat gles on every r	led bled and toggle flip rising edge.	o-flop is cleare	d				
bit 4	TxGSPM: Tin 1 = Timer1/3 0 = Timer1/3	ner1/3/5 Gate 3 /5 gate Single- /5 gate Single-	Single-Pulse M Pulse mode is Pulse mode is	lode bit enabled and is co disabled	ontrolling Time	r1/3/5 gate				
bit 3	TxGGO/DONE: Timer1/3/5 Gate Single-Pulse Acquisition Status bit 1 = Timer1/3/5 gate single-pulse acquisition is ready, waiting for an edge 0 = Timer1/3/5 gate single-pulse acquisition has completed or has not been started This bit is automatically cleared when TxGSPM is cleared.									
bit 2	TxGVAL: Timer1/3/5 Gate Current State bit Indicates the current state of the Timer1/3/5 gate that could be provided to TMRxH:TMRxL. Unaffected by Timer1/3/5 Gate Enable (TMRxGE).									
bit 1-0	TxGSS<1:0>: Timer1/3/5 Gate Source Select bits 00 = Timer1/3/5 Gate pin 01 = Timer2/4/6 Match PR2/4/6 output (See Table 12-5 for proper timer match selection) 10 = Comparator 1 optionally synchronized output (sync_C1OUT) 11 = Comparator 2 optionally synchronized output (sync_C2OUT)									

REGISTER 12-2: TXGCON: TIMER1/3/5 GATE CONTROL REGISTER

15.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a chip select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCKx)
- Serial Data Out (SDOx)
- Serial Data In (SDIx)
- Slave Select (SSx)

Figure 15-1 shows the block diagram of the MSSPx module when operating in SPI Mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 15-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 15-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDOx output pin which is connected to, and received by, the slave's SDIx input pin. The slave device transmits information out on its SDOx output pin, which is connected to, and received by, the master's SDIx input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register. During each SPI clock cycle, a full-duplex data transmission occurs. This means that at the same time, the slave device is sending out the MSb from its shift register and the master device is reading this bit from that same line and saving it as the LSb of its shift register.

After 8 bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.

15.6.4 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition (Figure 15-26), the user sets the Start Enable bit, SEN, of the SSPxCON2 register. If the SDAx and SCLx pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and starts its count. If SCLx and SDAx are both sampled high when the Baud Rate Generator times out (TBRG), the SDAx pin is driven low. The action of the SDAx being driven low while SCLx is high is the Start condition and causes the S bit of the SSPxSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and resumes its count.

When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPxCON2 register will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDAx line held low and the Start condition is complete.

- Note 1: If at the beginning of the Start condition, the SDAx and SCLx pins are already sampled low, or if during the Start condition, the SCLx line is sampled low before the SDAx line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLxIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.
 - 2: The Philips I²C Specification states that a bus collision cannot occur on a Start.



FIGURE 15-26: FIRST START BIT TIMING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
BAUDCON1	ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN	271
BAUDCON2	ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN	271
PMD0	UART2MD	UART1MD	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	52
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	270
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	270
SPBRG1	EUSART1 Baud Rate Generator, Low Byte								
SPBRGH1			EUSART1	Baud Rate (Generator, Hi	gh Byte			_
SPBRG2			EUSART2	Baud Rate C	Generator, Lo	w Byte			_
SPBRGH2	EUSART2 Baud Rate Generator, High Byte								_
PIR1	_	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	112
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	CTMUIF	TMR5GIF	TMR3GIF	TMR1GIF	114
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	269
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	269

TABLE 16-4: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Legend: — = unimplemented, read as '0'. Shaded bits are not used by the BRG.

TABLE 16-5: BAUD RATES FOR ASYNCHRONOUS MODES

		SYNC = 0, BRGH = 0, BRG16 = 0											
BAUD	Fos	c = 64.00	0 MHz	Fos	Fosc = 18.432 MHz			Fosc = 16.000 MHz			Fosc = 11.0592 MHz		
RATE	Actual Rate	% Error	SPBRxG value (decimal)	Actual Rate	% Error	SPBRGx value (decimal)	Actual Rate	% Error	SPBRGx value (decimal)	Actual Rate	% Error	SPBRGx value (decimal)	
300	—	_	_	_	_	_	_	_	_	_	_	_	
1200	_	_	_	1200	0.00	239	1202	0.16	207	1200	0.00	143	
2400	_	_	_	2400	0.00	119	2404	0.16	103	2400	0.00	71	
9600	9615	0.16	103	9600	0.00	29	9615	0.16	25	9600	0.00	17	
10417	10417	0.00	95	10286	-1.26	27	10417	0.00	23	10165	-2.42	16	
19.2k	19.23k	0.16	51	19.20k	0.00	14	19.23k	0.16	12	19.20k	0.00	8	
57.6k	58.82k	2.12	16	57.60k	0.00	7	—	_	_	57.60k	0.00	2	
115.2k	111.11k	-3.55	8	—	_	_	—	—	_	—	_	_	

		SYNC = 0, BRGH = 0, BRG16 = 0										
BAUD	Fos	Fosc = 8.000 MHz Fosc =		sc = 4.00	0 MHz	Fos	c = 3.6864	4 MHz	Fosc = 1.000 MHz			
RATE	Actual Rate	% Error	SPBRGx value (decimal)	Actual Rate	% Error	SPBRGx value (decimal)	Actual Rate	% Error	SPBRGx value (decimal)	Actual Rate	% Error	SPBRGx value (decimal)
300	—	_	_	300	0.16	207	300	0.00	191	300	0.16	51
1200	1202	0.16	103	1202	0.16	51	1200	0.00	47	1202	0.16	12
2400	2404	0.16	51	2404	0.16	25	2400	0.00	23	—	—	_
9600	9615	0.16	12	—	_	_	9600	0.00	5	—	_	_
10417	10417	0.00	11	10417	0.00	5	—	_	_	_	_	_
19.2k	_	_	_	_	_	_	19.20k	0.00	2	_	_	_
57.6k	—	_	—	—	_	—	57.60k	0.00	0	—	—	—
115.2k	—	—	—	—	_	—	—	—	—	—	—	—







22.7 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the VREFCON1 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

22.8 Effects of a Reset

A device Reset affects the following:

- DAC is disabled
- DAC output voltage is removed from the DACOUT pin
- The DACR<4:0> range select bits are cleared

22.9 Register Definitions: DAC Control

REGISTER 22-1: VREFCON1: VOLTAGE REFERENCE CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	U-0	R/W-0 R/W-0		U-0	R/W-0
DACEN	DACLPS	DACOE	—	DACPSS<1:0>		—	DACNSS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	DACEN: DAC Enable bit 1 = DAC is enabled 0 = DAC is disabled
bit 6	DACLPS: DAC Low-Power Voltage Source Select bit
	1 = DAC Positive reference source selected0 = DAC Negative reference source selected
bit 5	 DACOE: DAC Voltage Output Enable bit 1 = DAC voltage level is also an output on the DACOUT pin 0 = DAC voltage level is disconnected from the DACOUT pin
bit 4	Unimplemented: Read as '0'
bit 3-2	DACPSS<1:0>: DAC Positive Source Select bits 00 = VDD 01 = VREF+ 10 = FVR BUF1 output 11 = Reserved, do not use
bit 1	Unimplemented: Read as '0'
bit 0	DACNSS: DAC Negative Source Select bits 1 = VREF- 0 = VSS

ANDWF		AND W w	AND W with f					
Synt	ax:	ANDWF	ANDWF f {,d {,a}}					
Opei	rands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]						
Oper	ration:	(W) .AND.	(f) \rightarrow dest					
Statu	is Affected:	N, Z						
Enco	oding:	0001	01da fi	ff ffff				
Description: The contents of W are AND'ed with register 'f'. If 'd' is '0', the result is stored b in W. If 'd' is '1', the result is stored b in register 'f' (default). If 'a' is '0', the Access Bank is select If 'a' is '0', the BSR is used to select GPR bank. If 'a' is '0' and the extended instruct set is enabled, this instruction opera in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 25.2.3 "Byte-Oriented an Bit-Oriented Instructions in Index Literal Offset Mode" for details								
Word	ds:	1						
Cycle	es:	1						
QC	ycle Activity:							
	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process Data	Write to destination				
<u>Exar</u>	<u>nple</u> :	ANDWF	REG, 0,	0				
Before Instruction		tion						
	W REG After Instructio	= 17h = C2h on						
	W REG	= 02h = C2h						

вс		Branch if	Branch if Carry					
Synta	ax:	BC n	BC n					
Oper	ands:	-128 ≤ n ≤ 1	27					
Oper	ation:	if CARRY b (PC) + 2 + 2	if CARRY bit is '1' (PC) + 2 + 2n \rightarrow PC					
Statu	s Affected:	None						
Enco	ding:	1110	0010 nr	inn nnnn				
Desc	ription:	If the CARR will branch. The 2's con added to the incrementer instruction, PC + 2 + 2r 2-cycle inst	If the CARRY bit is '1', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.					
Word	ls:	1	1					
Cycle	es:	1(2)	1(2)					
Q C If Ju	ycle Activity:							
	Q1	Q2	Q3	Q4				
	Decode	Read literal 'n'	Process Data	Write to PC				
	No	No	No	No				
	operation	operation	operation	operation				
lf No	o Jump:							
	Q1	Q2	Q3	Q4				
Decode		Read literal	Process	No				
		'n'	Data	operation				
<u>Exan</u>	<u>nple</u> : Before Instruc	HERE	BC 5					

PC	=	address	(HERE)	
After Instruction				
If CARRY	=	1;		
PC	=	address	(HERE +	- 12)
If CARRY	=	0;		
PC	=	address	(HERE +	2)

CLRF	Clear f				CLRW	
Syntax:	CLRF f{,;	Syntax:				
Operands:	$0 \leq f \leq 255$				Operano	
	a ∈ [0,1]				Operatio	
Operation:	$\begin{array}{l} 000h \rightarrow f \\ 1 \rightarrow Z \end{array}$					
Status Affected:	Z					
Encoding:	0110	101a	ffff	ffff	Status A	
Description:	Clears the	contents	of the spe	cified	Encodin	
	register.				Descrip	
	If 'a' is '0', t If 'a' is '1', t GPR bank.	If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.				
	If 'a' is '0' a	If 'a' is '0' and the extended instruction				
	in Indexed	Literal O	ffset Addre	essing	Cycles:	
	mode when	never f ≤	95 (5Fh).	See	Q Cycl	
	Section 25	.2.3 "By	te-Oriente	ed and		
	Literal Offs	set Mode	e" for deta	ills.		
Words:	1					
Cycles:	1				Example	
Q Cycle Activity:					Bo	
Q1	Q2	Q3	3	Q4		
Decode	Read	Proce	ess	Write	Aft	
	register 'f'	register 'f' Data register 'f'				
Example:	CLRF	FLAG_	REG, 1			
Before Instruc	tion					
FLAG_R	EG = 5A	h				
After Instructio	on EC - 00	h				
FLAG_K	LG = 00					

CLRWDT		Clear Watchdog Timer						
Synta	ax:	CLRWDT	CLRWDT					
Oper	ands:	None						
Operation:		$\begin{array}{l} 000h \rightarrow W \\ 000h \rightarrow W \\ 1 \rightarrow \overline{\text{TO}}, \\ 1 \rightarrow \overline{\text{PD}} \end{array}$	$\begin{array}{l} 000h \rightarrow WDT, \\ 000h \rightarrow WDT \text{ postscaler,} \\ 1 \rightarrow \overline{TO}, \\ 1 \rightarrow \overline{PD} \end{array}$					
Statu	s Affected:	TO, PD						
Encoding:		0000	0000	0000 0000		0100		
Description:		CLRWDT in Watchdog scaler of th PD, are se	CLRWDT instruction resets the Watchdog Timer. It also resets the post- scaler of the WDT. Status bits, $\overline{\text{TO}}$ and $\overline{\text{PD}}$, are set.					
Word	ls:	1						
Cycle	es:	1	1					
Q Cycle Activity:								
Q1		Q2	Q3	3	Q4			
	Decode	No operation	Proce Dat	ess a	op	No peration		
Exan	nple:	CLRWDT						

Before Instruction		
WDT Counter	=	?
After Instruction		
WDT Counter	=	00h
WDT Postscaler	=	0
TO	=	1
PD	=	1

26.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

26.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent[®] and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika[®]









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28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS				
Dimension	n Limits	MIN	NOM	MAX		
Number of Pins	Ν		28			
Pitch	е		0.65 BSC			
Overall Height	Α	—	-	2.00		
Molded Package Thickness	A2	1.65	1.75	1.85		
Standoff	A1	0.05	-	-		
Overall Width	Е	7.40	7.80	8.20		
Molded Package Width	E1	5.00	5.30	5.60		
Overall Length	D	9.90	10.20	10.50		
Foot Length	L	0.55	0.75	0.95		
Footprint L1		1.25 REF				
Lead Thickness	С	0.09	-	0.25		
Foot Angle	¢	0°	4°	8°		
Lead Width	b	0.22	-	0.38		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch		0.65 BSC		
Contact Pad Spacing	С		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>[X]</u> ⁽²⁾ -	¥	<u>/xx</u>	<u>xxx</u>	Exa	mple	es:
Device	Tape and Reel Option	Temperatur Range	e Package	Pattern	a) b)	PIC PDI PIC pac	18(L)F45K22-E/P 301 = Extended temp., P package, QTP pattern #301. 18F46K22-I/SO = Industrial temp., SOIC kage.
Device:	PIC18F23K22, PIC18F24K22, PIC18F25K22, PIC18F26K22, PIC18F43K22, PIC18F44K22, PIC18F45K22, PIC18F46K22,	PIC18LF23K22 PIC18LF24K22 PIC18LF25K22 PIC18LF26K22 PIC18LF43K22 PIC18LF44K22 PIC18LF46K22			c) d)	PIC pac PIC tem	18F46K22-E/P = Extended temp., PDIP kage. 18F46K22T-I/ML = Tape and reel, Industrial p., QFN package.
Tape and Reel Option:	Blank = standa T = Tape and F	urd packaging (tu Reel ^{(1),} (2)	ibe or tray)				
Temperature Range: Package:	$E = -40^{\circ}$ $I = -40^{\circ}$ $ML = QFN$ $MV = UQF$ $P = PDII$ $PT = TQF$ $SO = SOH$ $SP = Skin$ $SS = SSC$	°C to +125°C °C to +85°C °N °P (Thin Quad F C ny Plastic DIP P	(Extended) (Industrial) atpack)		Note	e 1: 2:	Tape and Reel option is available for ML, MV, PT, SO and SS packages with industrial Temperature Range only. Tape and Reel identifier only appears in catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.
Pattern:	QTP, SQTP, Co (blank otherwis	ode or Special R se)	equirements				