What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 19x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf26k22-e-sp

PIC18(L)F2X/4XK22

1.2   Other Special Features

- **Memory Endurance:** The Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 10K for program memory and 100K for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.

- **Self-programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.

- **Extended Instruction Set:** The PIC18(L)F2X/4XK22 family introduces an optional extension to the PIC18 instruction set, which adds eight new instructions and an Indexed Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as C.

- **Enhanced CCP module:** In PWM mode, this module provides one, two or four modulated outputs for controlling half-bridge and full-bridge drivers. Other features include:
  - Auto-Shutdown, for disabling PWM outputs on interrupt or other select conditions
  - Auto-Restart, to reactivate outputs once the condition has cleared
  - Output steering to selectively enable one or more of four outputs to provide the PWM signal.

- **Enhanced Addressable EUSART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).

- **10-bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reduce code overhead.

- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit postscaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 27.0 "Electrical Specifications"** for time-out periods.

- **Charge Time Measurement Unit (CTMU)**

- **SR Latch Output:**

1.3   Details on Individual Family Members

Devices in the PIC18(L)F2X/4XK22 family are available in 28-pin and 40/44-pin packages. The block diagram for the device family is shown in Figure 1-1.

The devices have the following differences:

1. Flash program memory
2. Data Memory SRAM
3. Data Memory EEPROM
4. A/D channels
5. I/O ports
6. ECCP modules (Full/Half Bridge)
7. Input Voltage Range/Power Consumption

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in the pin summary tables: Table 2 and Table 3, and I/O description tables: Table 1-2 and Table 1-3.

PIC18(L)F2X/4XK22

TABLE 1-3: **PIC18(L)F4XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Number				Pin Name	Pin Type	Buffer Type	Description
PDIP	TQFP	QFN	UQFN				
18	37	37	33	RC3/SCK1/SCL1/AN15			
				RC3	I/O	ST	Digital I/O.
				SCK1	I/O	ST	Synchronous serial clock input/output for SPI mode (MSSP).
				SCL1	I/O	ST	Synchronous serial clock input/output for I^{2}C mode (MSSP).
				AN15	I	Analog	Analog input 15.
23	42	42	38	RC4/SDI1/SDA1/AN16			
				RC4	I/O	ST	Digital I/O.
				SDI1	I	ST	SPI data in (MSSP).
				SDA1	I/O	ST	I^{2}C data I/O (MSSP).
				AN16	I	Analog	Analog input 16.
24	43	43	39	RC5/SDO1/AN17			
				RC5	I/O	ST	Digital I/O.
				SDO1	O	—	SPI data out (MSSP).
				AN17	I	Analog	Analog input 17.
25	44	44	40	RC6/TX1/CK1/AN18			
				RC6	I/O	ST	Digital I/O.
				TX1	O	—	EUSART asynchronous transmit.
				CK1	I/O	ST	EUSART synchronous clock (see related RXx/DTx).
				AN18	I	Analog	Analog input 18.
26	1	1	1	RC7/RX1/DT1/AN19			
				RC7	I/O	ST	Digital I/O.
				RX1	I	ST	EUSART asynchronous receive.
				DT1	I/O	ST	EUSART synchronous data (see related TXx/CKx).
				AN19	I	Analog	Analog input 19.
19	38	38	34	RD0/SCK2/SCL2/AN20			
				RD0	I/O	ST	Digital I/O.
				SCK2	I/O	ST	Synchronous serial clock input/output for SPI mode (MSSP).
				SCL2	I/O	ST	Synchronous serial clock input/output for I^{2}C mode (MSSP).
				AN20	I	Analog	Analog input 20.
20	39	39	35	RD1/CCP4/SDI2/SDA2/AN21			
				RD1	I/O	ST	Digital I/O.
				CCP4	I/O	ST	Capture 4 input/Compare 4 output/PWM 4 output.
				SDI2	I	ST	SPI data in (MSSP).
				SDA2	I/O	ST	I^{2}C data I/O (MSSP).
				AN21	I	Analog	Analog input 21.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power.

Note 1: Default pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

TABLE 5-2: REGISTER FILE SUMMARY FOR PIC18(L)F2X/4XK22 DEVICES (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR
FA2h	IPR2	OSCFIP	C1IP	C2IP	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	1111 1111
FA1h	PIR2	OSCFIF	C1IF	C2IF	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	0000 0000
FA0h	PIE2	OSCFIE	C1IE	C2IE	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	0000 0000
F9Fh	IPR1	—	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	-111 1111
F9Eh	PIR1	—	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	-000 0000
F9Dh	PIE1	—	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	-000 0000
F9Ch	HLVDCON	VDIRMAG	BGVST	IRVST	HLVDEN	HLVDL<3:0>				0000 0000
F9Bh	OSCTUNE	INTSRC	PLLEN	TUN<5:0>						00xx xxxx
F96h	TRISE	WPUE3	—	—	—	—	TRISE2[1]	TRISE1[1]	TRISE0[1]	1--- -111
F95h	TRISD[1]	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111
F94h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111
F93h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111
F92h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111
F8Dh	LATE[1]	—	—	—	—	—	LATE2	LATE1	LATE0	---- -xxx
F8Ch	LATD[1]	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx xxxx
F8Bh	LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx xxxx
F8Ah	LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx xxxx
F89h	LATA	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx xxxx
F84h	PORTE[2]	—	—	—	—	RE3	—	—	—	---- x---
F84h	PORTE[1]	—	—	—	—	RE3	RE2	RE1	RE0	---- x000
F83h	PORTD[1]	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	0000 0000
F82h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	0000 00xx
F81h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxx0 0000
F80h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xx0x 0000
F7Fh	IPR5	—	—	—	—	—	TMR6IP	TMR5IP	TMR4IP	---- -111
F7Eh	PIR5	—	—	—	—	—	TMR6IF	TMR5IF	TMR4IF	---- -111
F7Dh	PIE5	—	—	—	—	—	TMR6IE	TMR5IE	TMR4IE	---- -000
F7Ch	IPR4	—	—	—	—	—	CCP5IP	CCP4IP	CCP3IP	---- -000
F7Bh	PIR4	—	—	—	—	—	CCP5IF	CCP4IF	CCP3IF	---- -000
F7Ah	PIE4	—	—	—	—	—	CCP5IE	CCP4IE	CCP3IE	---- -000
F79h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH<1:0>		0000 1000
F78h	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH<1:0>		0000 1000
F77h	CM2CON1	MC1OUT	MC2OUT	C1RSEL	C2RSEL	C1HYS	C2HYS	C1SYNC	C2SYNC	0000 0000
F76h	SPBRGH2	EUSART2 Baud Rate Generator, High Byte								0000 0000
F75h	SPBRG2	EUSART2 Baud Rate Generator, Low Byte								0000 0000
F74h	RCREG2	EUSART2 Receive Register								0000 0000
F73h	TXREG2	EUSART2 Transmit Register								0000 0000
F72h	TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010
F71h	RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x
F70h	BAUDCON2	ABDOVF	RCIDL	DTRXP	CKTXP	BRG16	—	WUE	ABDEN	01x0 0-00
F6Fh	SSP2BUF	SSP2 Receive Buffer/Transmit Register								xxxx xxxx
F6Eh	SSP2ADD	SSP2 Address Register in I²C Slave Mode. SSP2 Baud Rate Reload Register in I²C Master Mode								0000 0000
F6Dh	SSP2STAT	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	0000 0000
F6Ch	SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				0000 0000
F6Bh	SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000
F6Ah	SSP2MSK	SSP1 MASK Register bits								1111 1111
F69h	SSP2CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000 0000

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition

Note 1: PIC18(L)F4XK22 devices only.
   2: PIC18(L)F2XK22 devices only.
   3: PIC18(L)F23/24K22 and PIC18(L)F43/44K22 devices only.
   4: PIC18(L)F26K22 and PIC18(L)F46K22 devices only.

PIC18(L)F2X/4XK22

REGISTER 7-1:   EECON1: DATA EEPROM CONTROL 1 REGISTER

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
S = Bit can be set by software, but not cleared		U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **EEPGD:** Flash Program or Data EEPROM Memory Select bit

1 = Access Flash program memory
0 = Access data EEPROM memory

bit 6   **CFGS:** Flash Program/Data EEPROM or Configuration Select bit

1 = Access Configuration registers
0 = Access Flash program or data EEPROM memory

bit 5   **Unimplemented:** Read as '0'

bit 4   **FREE:** Flash Row (Block) Erase Enable bit

1 = Erase the program memory block addressed by TBLPTR on the next WR command
    (cleared by completion of erase operation)
0 = Perform write-only

bit 3   **WRERR:** Flash Program/Data EEPROM Error Flag bit[1]

1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal
    operation, or an improper write attempt)
0 = The write operation completed

bit 2   **WREN:** Flash Program/Data EEPROM Write Enable bit

1 = Allows write cycles to Flash program/data EEPROM
0 = Inhibits write cycles to Flash program/data EEPROM

bit 1   **WR:** Write Control bit

1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle.
    (The operation is self-timed and the bit is cleared by hardware once write is complete.
    The WR bit can only be set (not cleared) by software.)
0 = Write cycle to the EEPROM is complete

bit 0   **RD:** Read Control bit

1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared by hardware. The RD bit can only
    be set (not cleared) by software. RD bit cannot be set when EEPGD = 1 or CFGS = 1.)
0 = Does not initiate an EEPROM read

Note 1:   When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the
        error condition.

PIC18(L)F2X/4XK22

REGISTER 9-2: INTCON2: INTERRUPT CONTROL 2 REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	U-0	R/W-1	U-0	R/W-1
$\overline{\text{RBPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **RBPU:** PORTB Pull-up Enable bit
   1 = All PORTB pull-ups are disabled
   0 = PORTB pull-ups are enabled provided that the pin is an input and the corresponding WPUB bit is set.

bit 6   **INTEDG0:** External Interrupt 0 Edge Select bit
   1 = Interrupt on rising edge
   0 = Interrupt on falling edge

bit 5   **INTEDG1:** External Interrupt 1 Edge Select bit
   1 = Interrupt on rising edge
   0 = Interrupt on falling edge

bit 4   **INTEDG2:** External Interrupt 2 Edge Select bit
   1 = Interrupt on rising edge
   0 = Interrupt on falling edge

bit 3   **Unimplemented:** Read as '0'

bit 2   **TMR0IP:** TMR0 Overflow Interrupt Priority bit
   1 = High priority
   0 = Low priority

bit 1   **Unimplemented:** Read as '0'

bit 0   **RBIP:** RB Port Change Interrupt Priority bit
   1 = High priority
   0 = Low priority

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

REGISTER 9-14:   IPR1: PERIPHERAL INTERRUPT PRIORITY REGISTER 1

U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **Unimplemented:** Read as '`0`'

bit 6   **ADIP:** A/D Converter Interrupt Priority bit

`1` = High priority
`0` = Low priority

bit 5   **RC1IP:** EUSART1 Receive Interrupt Priority bit

`1` = High priority
`0` = Low priority

bit 4   **TX1IP:** EUSART1 Transmit Interrupt Priority bit

`1` = High priority
`0` = Low priority

bit 3   **SSP1IP:** Master Synchronous Serial Port 1 Interrupt Priority bit

`1` = High priority
`0` = Low priority

bit 2   **CCP1IP:** CCP1 Interrupt Priority bit

`1` = High priority
`0` = Low priority

bit 1   **TMR2IP:** TMR2 to PR2 Match Interrupt Priority bit

`1` = High priority
`0` = Low priority

bit 0   **TMR1IP:** TMR1 Overflow Interrupt Priority bit

`1` = High priority
`0` = Low priority

13.6   Register Definitions: Timer2/4/6 Control

REGISTER 13-1:   TxCON: TIMER2/TIMER4/TIMER6 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—		TxOUTPS<3:0>			TMRxON	TxCKPS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7   **Unimplemented:** Read as '0'

bit 6-3   **TxOUTPS<3:0>:** TimerX Output Postscaler Select bits

0000 = 1:1 Postscaler
0001 = 1:2 Postscaler
0010 = 1:3 Postscaler
0011 = 1:4 Postscaler
0100 = 1:5 Postscaler
0101 = 1:6 Postscaler
0110 = 1:7 Postscaler
0111 = 1:8 Postscaler
1000 = 1:9 Postscaler
1001 = 1:10 Postscaler
1010 = 1:11 Postscaler
1011 = 1:12 Postscaler
1100 = 1:13 Postscaler
1101 = 1:14 Postscaler
1110 = 1:15 Postscaler
1111 = 1:16 Postscaler

bit 2   **TMRxON:** TimerX On bit

1 = TimerX is on
0 = TimerX is off

bit 1-0   **TxCKPS<1:0>:** Timer2-type Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

14.5 Register Definitions: ECCP Control

REGISTER 14-1: CCPxCON: STANDARD CCPx CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB<1:0>		CCPxM<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6   **Unused**

bit 5-4   **DCxB<1:0>:** PWM Duty Cycle Least Significant bits

<u>Capture mode:</u>
Unused

<u>Compare mode:</u>
Unused

<u>PWM mode:</u>
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0   **CCPxM<3:0>:** ECCPx Mode Select bits

0000 = Capture/Compare/PWM off (resets the module)
0001 = Reserved
0010 = Compare mode: toggle output on match
0011 = Reserved

0100 = Capture mode: every falling edge
0101 = Capture mode: every rising edge
0110 = Capture mode: every 4th rising edge
0111 = Capture mode: every 16th rising edge

1000 = Compare mode: set output on compare match (CCPx pin is set, CCPxIF is set)
1001 = Compare mode: clear output on compare match (CCPx pin is cleared, CCPxIF is set)
1010 = Compare mode: generate software interrupt on compare match (CCPx pin is unaffected, CCPxIF is set)
1011 = Compare mode: Special Event Trigger (CCPx pin is unaffected, CCPxIF is set)
            TimerX (selected by CxTSEL bits) is reset
            ADON is set, starting A/D conversion if A/D module is enabled[1]
11xx =: PWM mode

Note 1:   This feature is available on CCP5 only.

15.2.3 SPI MASTER MODE

The master can initiate the data transfer at any time because it controls the SCKx line. The master determines when the slave (Processor 2, Figure 15-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPxBUF register is written to. If the SPI is only going to receive, the SDOx output could be disabled (programmed as an input). The SSPxSR register will continue to shift in the signal present on the SDIx pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPxBUF register as if a normal received byte (interrupts and Status bits appropriately set).

The clock polarity is selected by appropriately programming the CKP bit of the SSPxCON1 register and the CKE bit of the SSPxSTAT register.

This then, would give waveforms for SPI communication as shown in Figure 15-6, Figure 15-8, Figure 15-9 and Figure 15-10, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- $F_{OSC}/4$ (or T_{CY})
- $F_{OSC}/16$ (or 4 * T_{CY})
- $F_{OSC}/64$ (or 16 * T_{CY})
- Timer2 output/2
- $F_{OSC}/(4 * (SSPxADD + 1))$

Figure 15-6 shows the waveforms for Master mode.

When the CKE bit is set, the SDOx data is valid before there is a clock edge on SCKx. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPxBUF is loaded with the received data is shown.

FIGURE 15-6: SPI MODE WAVEFORM (MASTER MODE)
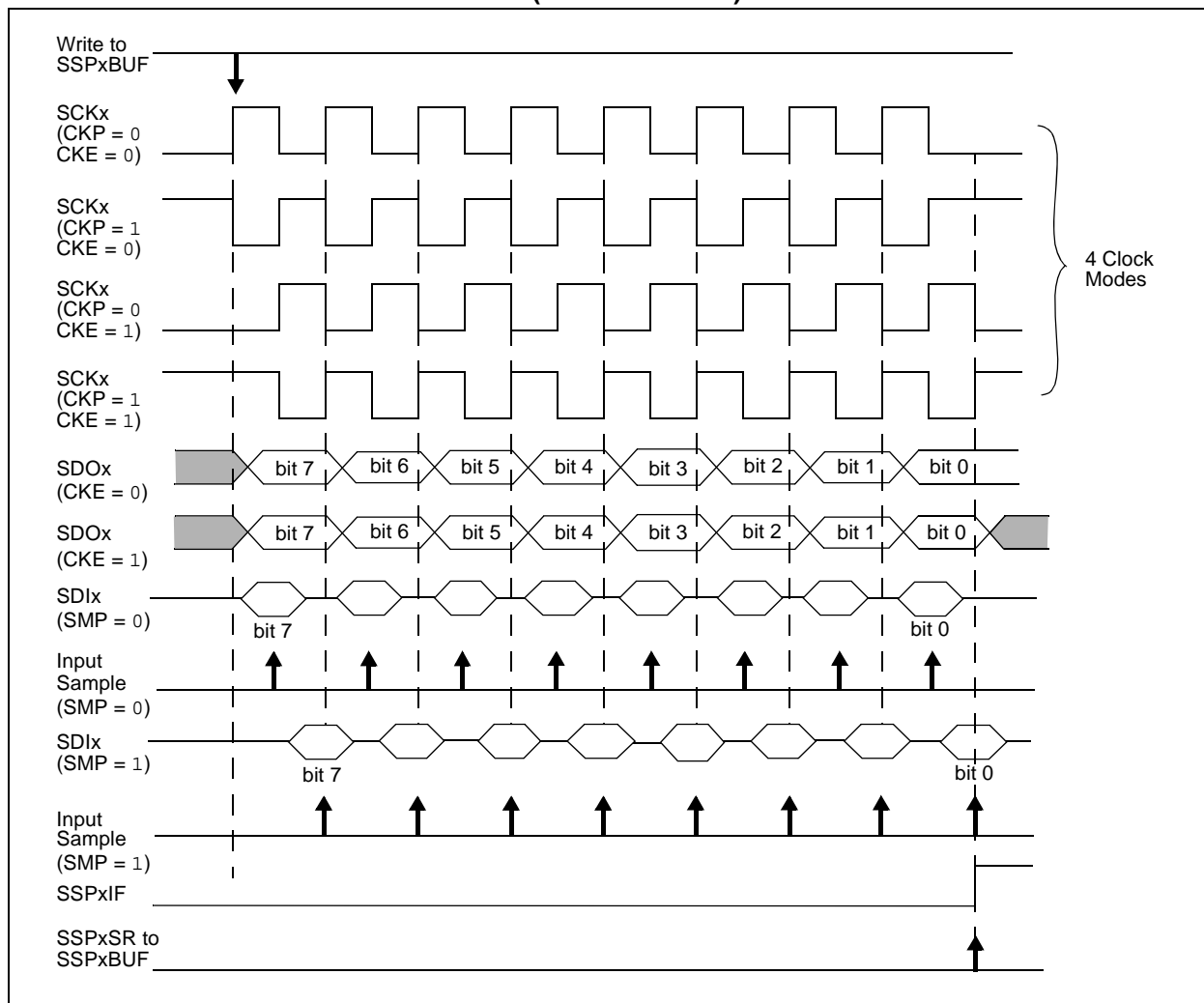
15.5.4 SLAVE MODE 10-BIT ADDRESS RECEPTION

This section describes a standard sequence of events for the MSSPx module configured as an I²C slave in 10-bit Addressing mode (Figure 15-20) and is used as a visual reference for this description.

This is a step by step process of what must be done by slave software to accomplish I²C communication.

1. Bus starts Idle.
2. Master sends Start condition; S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Master sends matching high address with R/$\overline{\text{W}}$ bit clear; UA bit of the SSPxSTAT register is set.
4. Slave sends $\overline{\text{ACK}}$ and SSPxIF is set.
5. Software clears the SSPxIF bit.
6. Software reads received address from SSPxBUF clearing the BF flag.
7. Slave loads low address into SSPxADD, releasing SCLx.
8. Master sends matching low address byte to the slave; UA bit is set.

> **Note:** Updates to the SSPxADD register are not allowed until after the $\overline{\text{ACK}}$ sequence.

9. Slave sends $\overline{\text{ACK}}$ and SSPxIF is set.

> **Note:** If the low address does not match, SSPxIF and UA are still set so that the slave software can set SSPxADD back to the high address. BF is not set because there is no match. CKP is unaffected.

10. Slave clears SSPxIF.
11. Slave reads the received matching address from SSPxBUF clearing BF.
12. Slave loads high address into SSPxADD.
13. Master clocks a data byte to the slave and clocks out the slaves $\overline{\text{ACK}}$ on the 9th SCLx pulse; SSPxIF is set.
14. If SEN bit of SSPxCON2 is set, CKP is cleared by hardware and the clock is stretched.
15. Slave clears SSPxIF.
16. Slave reads the received byte from SSPxBUF clearing BF.
17. If SEN is set the slave sets CKP to release the SCLx.
18. Steps 13-17 repeat for each received byte.
19. Master sends Stop to end the transmission.

15.5.5 10-BIT ADDRESSING WITH ADDRESS OR DATA HOLD

Reception using 10-bit addressing with AHEN or DHEN set is the same as with 7-bit modes. The only difference is the need to update the SSPxADD register using the UA bit. All functionality, specifically when the CKP bit is cleared and SCLx line is held low are the same. Figure 15-21 can be used as a reference of a slave in 10-bit addressing with AHEN set.

Figure 15-22 shows a standard waveform for a slave transmitter in 10-bit Addressing mode.

15.6.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDAx pin, arbitration takes place when the master outputs a '1' on SDAx, by letting SDAx float high and another master asserts a '0'. When the SCLx pin floats high, data should be stable. If the expected data on SDAx is a '1' and the data sampled on the SDAx pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLxIF, and reset the I^{2}C port to its Idle state (Figure 15-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDAx and SCLx lines are deasserted and the SSPxBUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I^{2}C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDAx and SCLx lines are deasserted and the respective control bits in the SSPxCON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I^{2}C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDAx and SCLx pins. If a Stop condition occurs, the SSPxIF bit will be set.

A write to the SSPxBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^{2}C bus can be taken when the P bit is set in the SSPxSTAT register, or the bus is Idle and the S and P bits are cleared.

FIGURE 15-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE
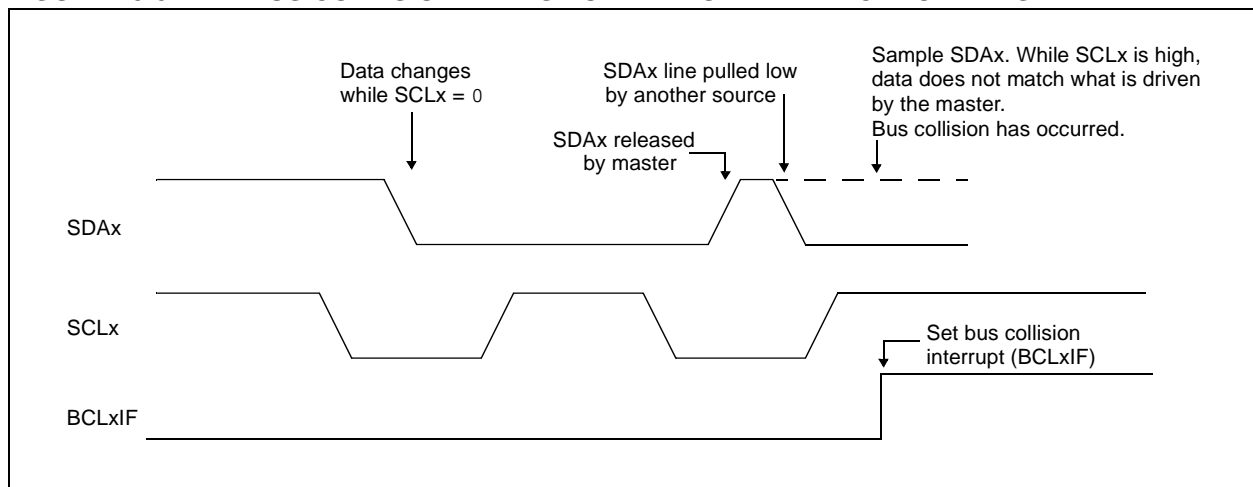
16.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock and data polarity

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 16-1 and Figure 16-2.

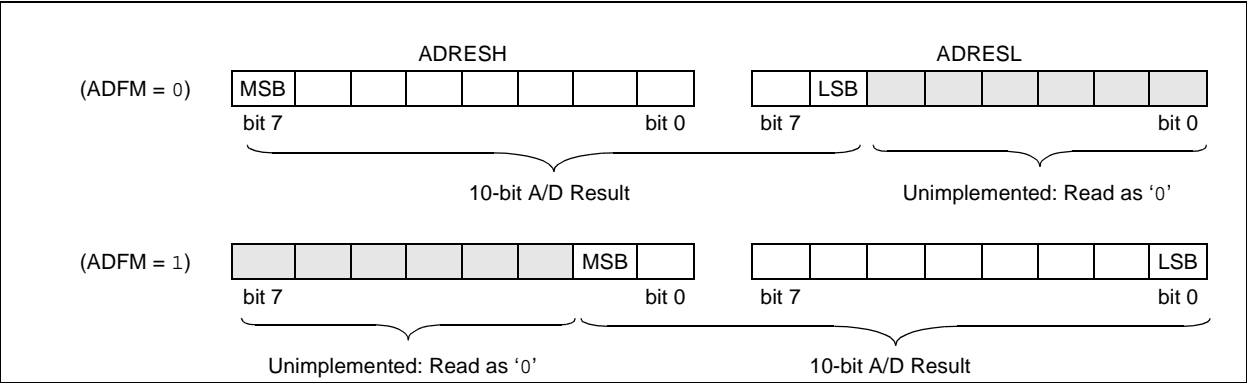**FIGURE 16-1: EUSART TRANSMIT BLOCK DIAGRAM**
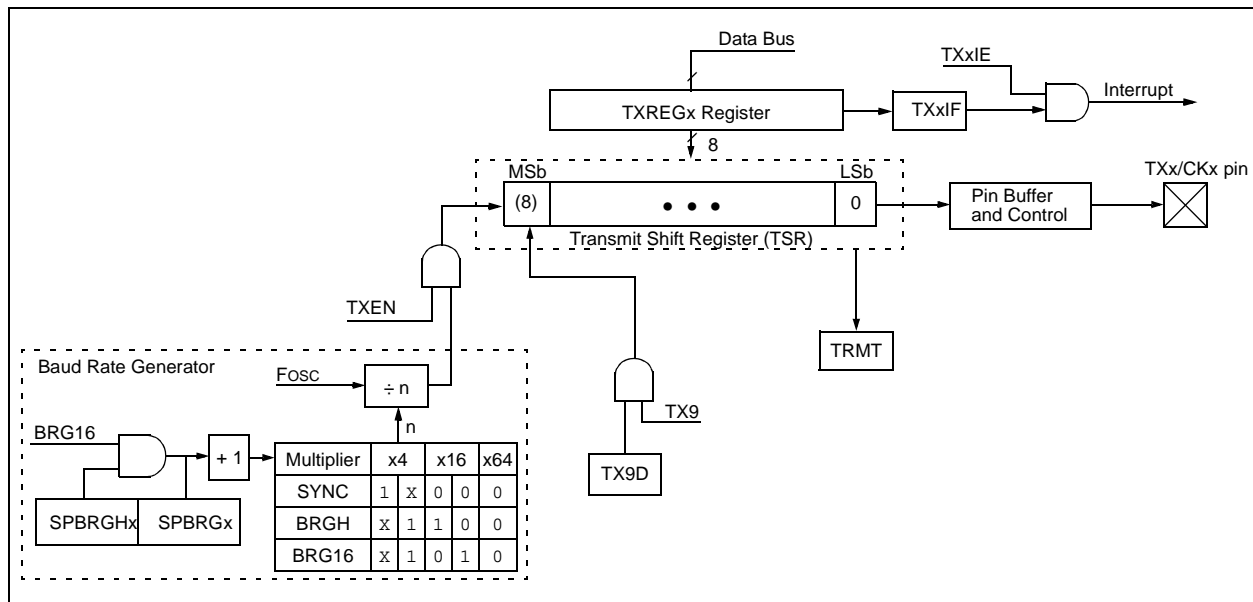
17.1.7   RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON2 register controls the output format.

Figure 17-2 shows the two output formats.

FIGURE 17-2:   **10-BIT A/D CONVERSION RESULT FORMAT**
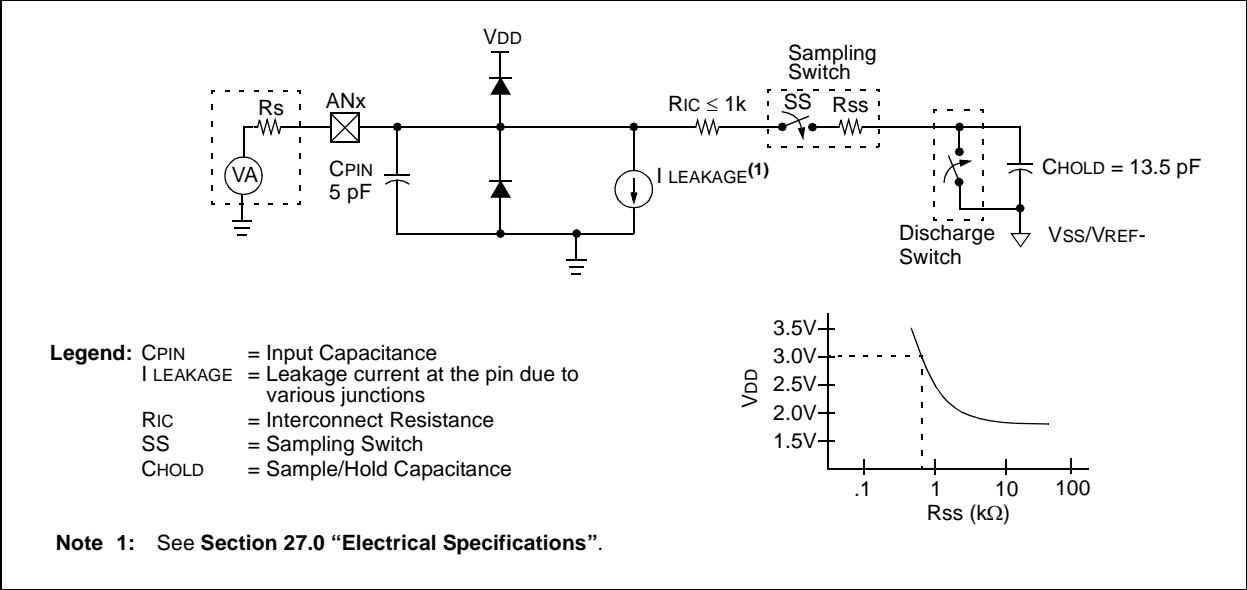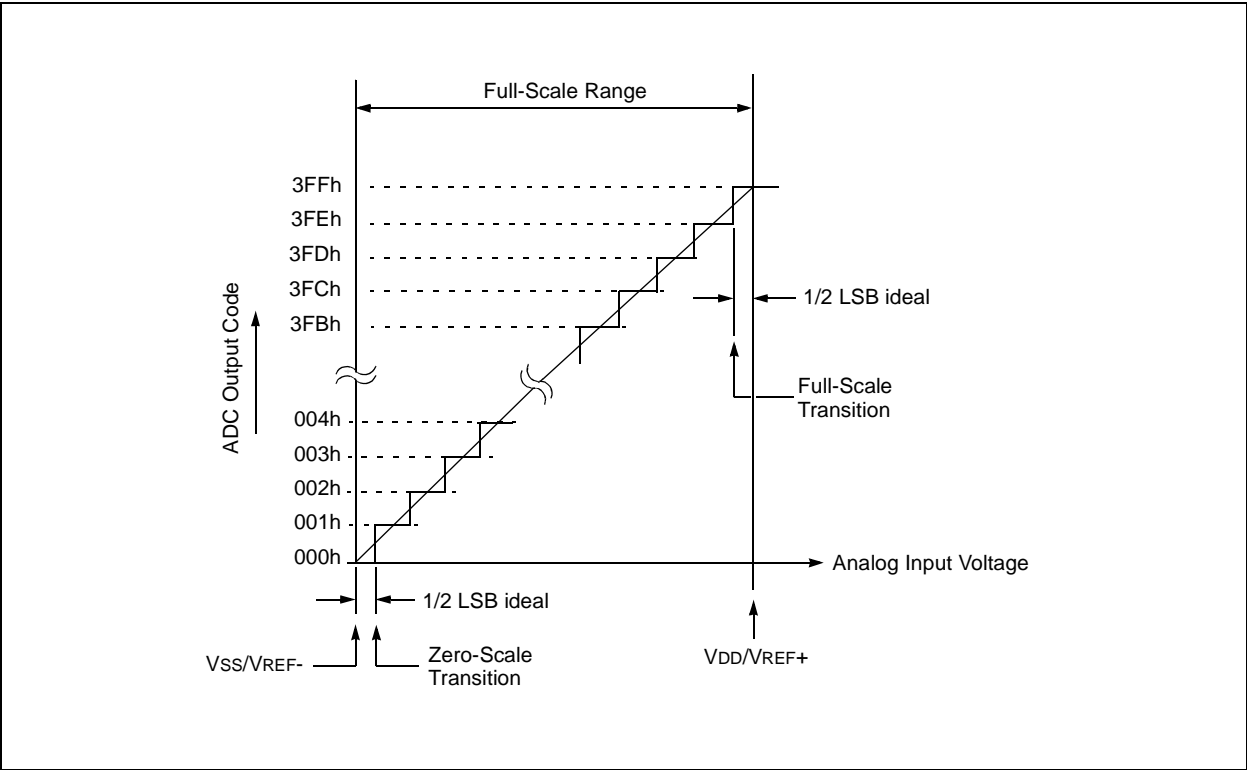
FIGURE 17-5: **ANALOG INPUT MODEL**

Legend: CPIN = Input Capacitance
I LEAKAGE = Leakage current at the pin due to various junctions
RIC = Interconnect Resistance
SS = Sampling Switch
CHOLD = Sample/Hold Capacitance

Note 1: See **Section 27.0 "Electrical Specifications"**.

FIGURE 17-6: **ADC TRANSFER FUNCTION**

PIC18(L)F2X/4XK22

19.3 Calibrating the CTMU Module

The CTMU requires calibration for precise measurements of capacitance and time, as well as for accurate time delay. If the application only requires measurement of a relative change in capacitance or time, calibration is usually not necessary. An example of this type of application would include a capacitive touch switch, in which the touch circuit has a baseline capacitance, and the added capacitance of the human body changes the overall capacitance of a circuit.

If actual capacitance or time measurement is required, two hardware calibrations must take place: the current source needs calibration to set it to a precise current, and the circuit being measured needs calibration to measure and/or nullify all other capacitance other than that to be measured.

### 19.3.1 CURRENT SOURCE CALIBRATION

The current source on the CTMU module is trimable. Therefore, for precise measurements, it is possible to measure and adjust this current source by placing a high precision resistor, RCAL, onto an unused analog channel. An example circuit is shown in Figure 19-2. The current source measurement is performed using the following steps:

1. Initialize the A/D Converter.
2. Initialize the CTMU.
3. Enable the current source by setting EDG1STAT (CTMUCONL<0>).
4. Issue settling time delay.
5. Perform A/D conversion.
6. Calculate the current source current using $I = V/R_{CAL}$, where R_{CAL} is a high precision resistance and V is measured by performing an A/D conversion.

The CTMU current source may be trimmed with the trim bits in CTMUICON using an iterative process to get an exact desired current. Alternatively, the nominal value without adjustment may be used; it may be stored by the software for use in all subsequent capacitive or time measurements.

To calculate the value for R_{CAL}, the nominal current must be chosen, and then the resistance can be calculated. For example, if the A/D Converter reference voltage is 3.3V, use 70% of full scale, or 2.31V as the desired approximate voltage to be read by the A/D Converter. If the range of the CTMU current source is selected to be 0.55 μA, the resistor value needed is calculated as $R_{CAL} = 2.31V/0.55$ μA, for a value of 4.2 MΩ. Similarly, if the current source is chosen to be 5.5 μA, R_{CAL} would be 420,000Ω, and 42,000Ω if the current source is set to 55 μA.

FIGURE 19-2: CTMU CURRENT SOURCE CALIBRATION CIRCUIT
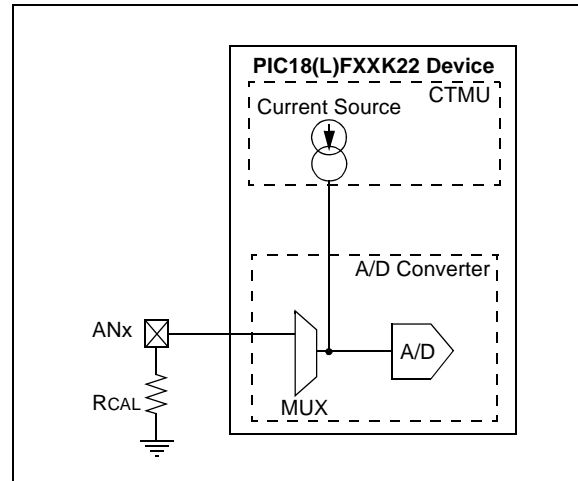
A value of 70% of full-scale voltage is chosen to make sure that the A/D Converter was in a range that is well above the noise floor. Keep in mind that if an exact current is chosen, that is to incorporate the trimming bits from CTMUICON, the resistor value of RCAL may need to be adjusted accordingly. RCAL may also be adjusted to allow for available resistor values. RCAL should be of the highest precision available, keeping in mind the amount of precision needed for the circuit that the CTMU will be used to measure. A recommended minimum would be 0.1% tolerance.

The following examples show one typical method for performing a CTMU current calibration. Example 19-1 demonstrates how to initialize the A/D Converter and the CTMU; this routine is typical for applications using both modules. Example 19-2 demonstrates one method for the actual calibration routine.

BZ	**Branch if Zero**
Syntax:	BZ n
Operands:	$-128 \le n \le 127$
Operation:	if ZERO bit is '1' (PC) + 2 + 2n $\to$ PC
Status Affected:	None

Encoding:

1110	0000	nnnn	nnnn

Description:	If the ZERO bit is '1', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.
Words:	1
Cycles:	1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE   BZ   Jump

```
Before Instruction
    PC       =    address (HERE)
After Instruction
    If ZERO  =    1;
        PC   =    address (Jump)
    If ZERO  =    0;
        PC   =    address (HERE + 2)
```

CALL	**Subroutine Call**
Syntax:	CALL k {,s}
Operands:	$0 \le k \le 1048575$ $s \in [0,1]$
Operation:	(PC) + 4 $\to$ TOS, k $\to$ PC<20:1>, if s = 1 (W) $\to$ WS, (Status) $\to$ STATUSS, (BSR) $\to$ BSRS
Status Affected:	None

Encoding:
1st word (k<7:0>)
2nd word(k<19:8>)

1110	110s	$k_7$kkk	kkkk$_0$
1111	k_{19}kkk	kkkk	kkkk$_8$

Description:	Subroutine call of entire 2-Mbyte memory range. First, return address (PC + 4) is pushed onto the return stack. If 's' = 1, the W, STATUS and BSR registers are also pushed into their respective shadow registers, WS, STATUSS and BSRS. If 's' = 0, no update occurs (default). Then, the 20-bit value 'k' is loaded into PC<20:1>. CALL is a 2-cycle instruction.
Words:	2
Cycles:	2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>,	PUSH PC to stack	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

Example: HERE   CALL   THERE, 1

```
Before Instruction
    PC        =    address (HERE)
After Instruction
    PC        =    address (THERE)
    TOS       =    address (HERE + 4)
    WS        =    W
    BSRS      =    BSR
    STATUSS   =    Status
```

TABLE 27-13:   CAPTURE/COMPARE/PWM REQUIREMENTS (ALL CCP MODULES)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
50	TccL	CCPx Input Low Time	No prescaler	0.5 T_{CY} + 20	—	ns	
			With prescaler	10	—	ns	
51	TccH	CCPx Input High Time	No prescaler	0.5 T_{CY} + 20	—	ns	
			With prescaler	10	—	ns	
52	TccP	CCPx Input Period		$\frac{3\ T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fall Time		—	25	ns	
54	TccF	CCPx Output Fall Time		—	25	ns	

PIC18(L)F2X/4XK22

FIGURE 28-52: **PIC18LF2X/4XK22 TYPICAL I_{DD}: PRI_RUN EC HIGH POWER**

FIGURE 28-52: PIC18LF2X/4XK22 TYPICAL I_{DD}: PRI_RUN EC HIGH POWER

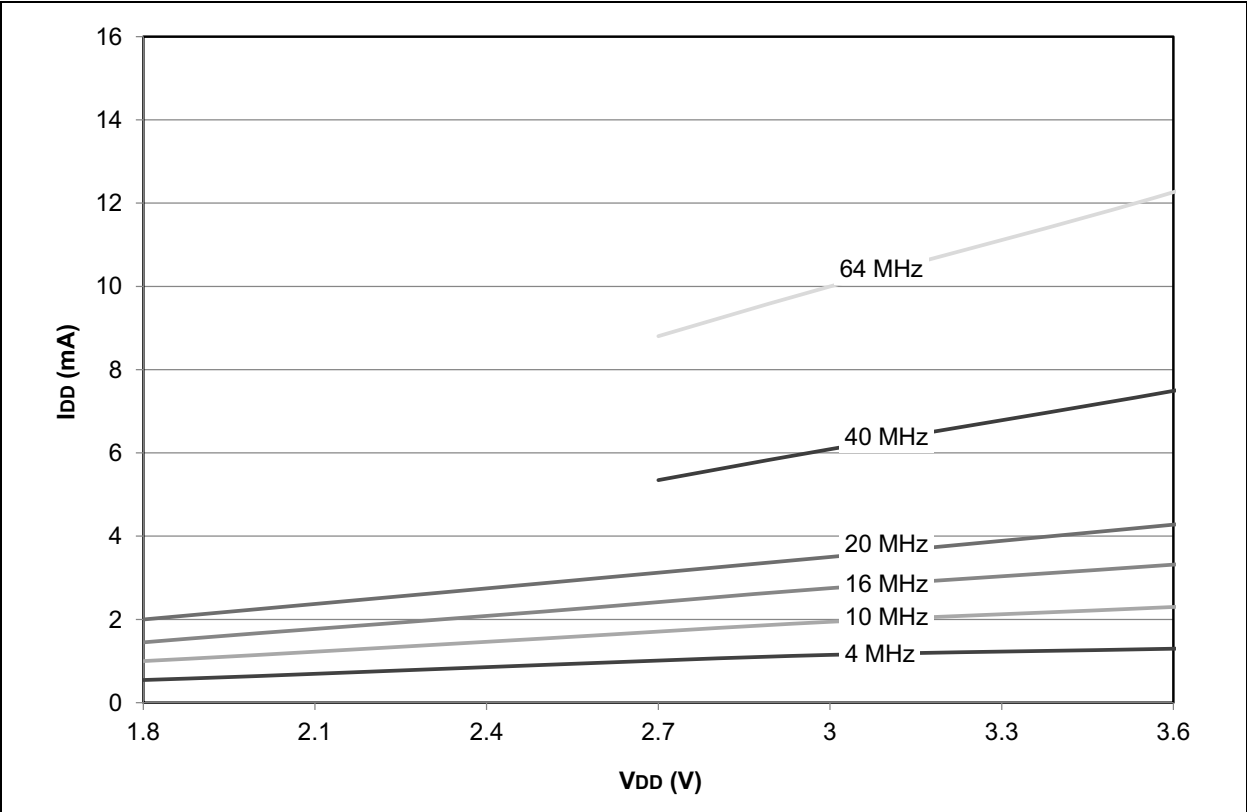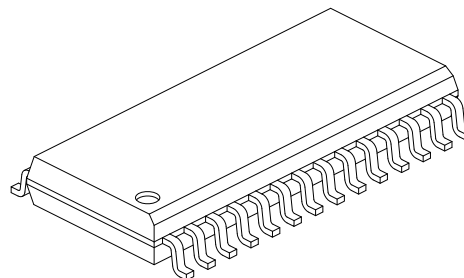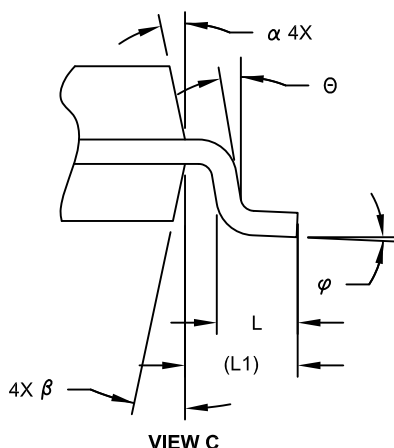**FIGURE 28-53:** PIC18LF2X/4XK22 MAXIMUM I_{DD}: PRI_RUN EC HIGH POWER

FIGURE 28-84: **PIC18(L)F2X/4XK22 PIN INPUT LEAKAGE**
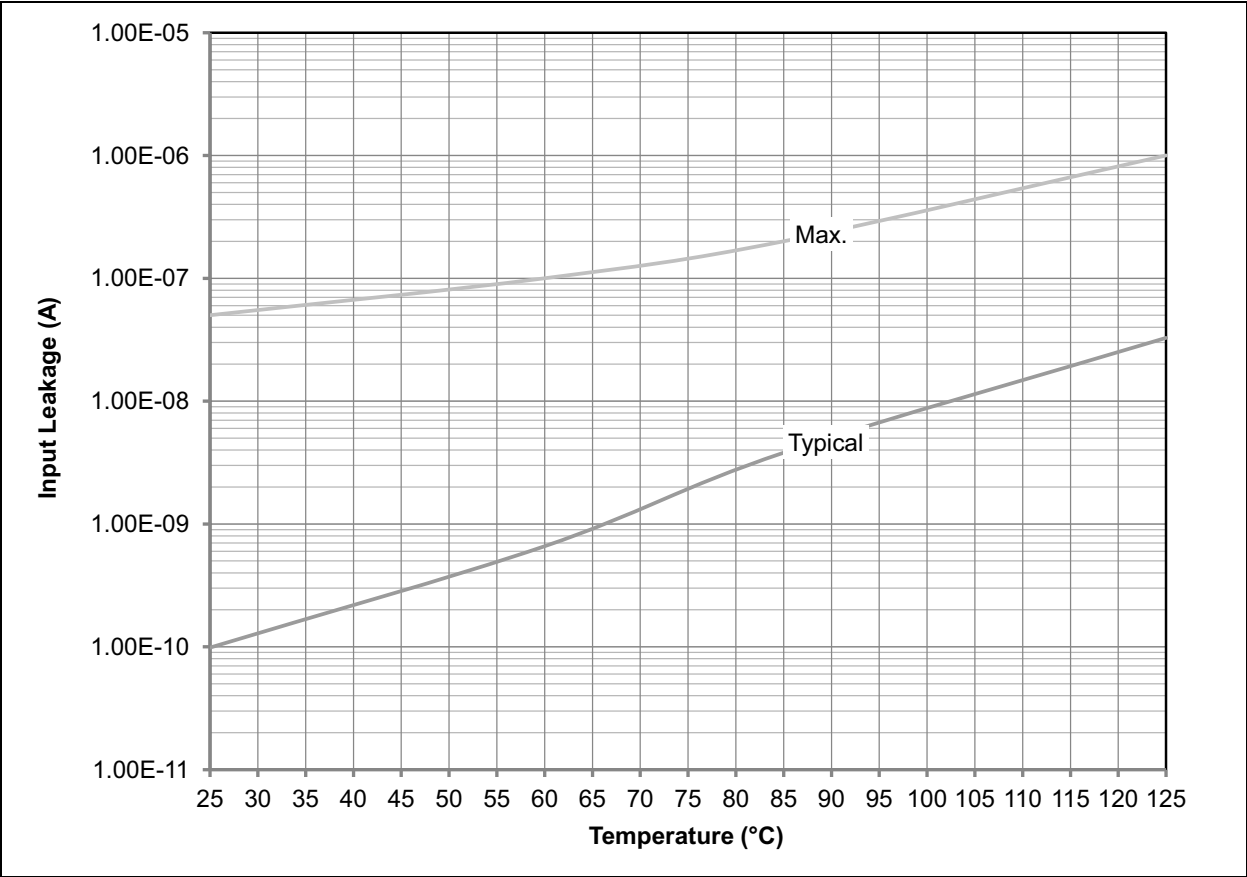
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

VIEW C

	Units		MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2