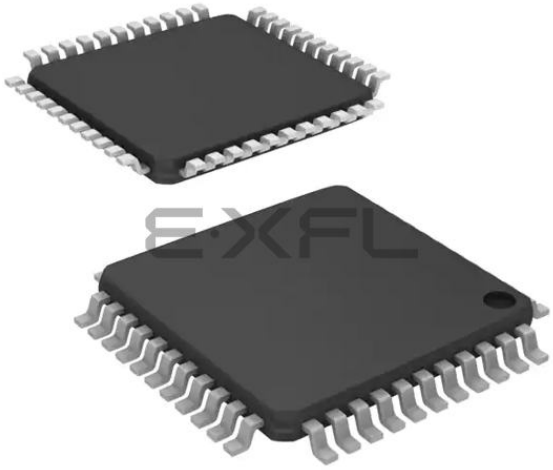

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 30x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf44k22-e-pt

TABLE 1-3: PIC18(L)F4XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Number				Pin Name	Pin Type	Buffer Type	Description
PDIP	TQFP	QFN	UQFN				
37	14	14	12	RB4/IOC0/T5G/AN11			
				RB4	I/O	TTL	Digital I/O.
				IOC0	I	TTL	Interrupt-on-change pin.
				T5G	I	ST	Timer5 external clock gate input.
				AN11	I	Analog	Analog input 11.
38	15	15	13	RB5/IOC1/P3A/CCP3/T3CKI/T1G/AN13			
				RB5	I/O	TTL	Digital I/O.
				IOC1	I	TTL	Interrupt-on-change pin.
				P3A(1)	O	CMOS	Enhanced CCP3 PWM output.
				CCP3(1)	I/O	ST	Capture 3 input/Compare 3 output/PWM 3 output.
				T3CKI(2)	I	ST	Timer3 clock input.
				T1G	I	ST	Timer1 external clock gate input.
				AN13	I	Analog	Analog input 13.
39	16	16	14	RB6/IOC2/PGC			
				RB6	I/O	TTL	Digital I/O.
				IOC2	I	TTL	Interrupt-on-change pin.
				PGC	I/O	ST	In-Circuit Debugger and ICSP™ programming clock pin.
40	17	17	15	RB7/IOC3/PGD			
				RB7	I/O	TTL	Digital I/O.
				IOC3	I	TTL	Interrupt-on-change pin.
				PGD	I/O	ST	In-Circuit Debugger and ICSP™ programming data pin.
15	32	34	30	RC0/P2B/T3CKI/T3G/T1CKI/SOSCO			
				RC0	I/O	ST	Digital I/O.
				P2B(2)	O	CMOS	Enhanced CCP1 PWM output.
				T3CKI(1)	I	ST	Timer3 clock input.
				T3G	I	ST	Timer3 external clock gate input.
				T1CKI	I	ST	Timer1 clock input.
				SOSCO	O	—	Secondary oscillator output.
16	35	35	31	RC1/P2A/CCP2/SOSCI			
				RC1	I/O	ST	Digital I/O.
				P2A(1)	O	CMOS	Enhanced CCP2 PWM output.
				CCP2(1)	I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
				SOSCI	I	Analog	Secondary oscillator input.
17	36	36	32	RC2/CTPLS/P1A/CCP1/T5CKI/AN14			
				RC2	I/O	ST	Digital I/O.
				CTPLS	O	—	CTMU pulse generator output.
				P1A	O	CMOS	Enhanced CCP1 PWM output.
				CCP1	I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
				T5CKI	I	ST	Timer5 clock input.
				AN14	I	Analog	Analog input 14.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power.

Note 1: Default pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

TABLE 1-3: PIC18(L)F4XK22 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Number				Pin Name	Pin Type	Buffer Type	Description
PDIP	TQFP	QFN	UQFN				
21	40	40	36	RD2/P2B/AN22			
				RD2	I/O	ST	Digital I/O
				P2B(1)	O	CMOS	Enhanced CCP2 PWM output.
				AN22	I	Analog	Analog input 22.
22	41	41	37	RD3/P2C/$\overline{SS2}$/AN23			
				RD3	I/O	ST	Digital I/O.
				P2C	O	CMOS	Enhanced CCP2 PWM output.
				$\overline{SS2}$	I	TTL	SPI slave select input (MSSP).
				AN23	I	Analog	Analog input 23.
27	2	2	2	RD4/P2D/SDO2/AN24			
				RD4	I/O	ST	Digital I/O.
				P2D	O	CMOS	Enhanced CCP2 PWM output.
				SDO2	O	—	SPI data out (MSSP).
				AN24	I	Analog	Analog input 24.
28	3	3	3	RD5/P1B/AN25			
				RD5	I/O	ST	Digital I/O.
				P1B	O	CMOS	Enhanced CCP1 PWM output.
				AN25	I	Analog	Analog input 25.
29	4	4	4	RD6/P1C/TX2/CK2/AN26			
				RD6	I/O	ST	Digital I/O.
				P1C	O	CMOS	Enhanced CCP1 PWM output.
				TX2	O	—	EUSART asynchronous transmit.
				CK2	I/O	ST	EUSART synchronous clock (see related RXx/DTx).
				AN26	I	Analog	Analog input 26.
30	5	5	5	RD7/P1D/RX2/DT2/AN27			
				RD7	I/O	ST	Digital I/O.
				P1D	O	CMOS	Enhanced CCP1 PWM output.
				RX2	I	ST	EUSART asynchronous receive.
				DT2	I/O	ST	EUSART synchronous data (see related TXx/CKx).
				AN27	I	Analog	Analog input 27.
8	25	25	23	RE0/P3A/CCP3/AN5			
				RE0	I/O	ST	Digital I/O.
				P3A(2)	O	CMOS	Enhanced CCP3 PWM output.
				CCP3(2)	I/O	ST	Capture 3 input/Compare 3 output/PWM 3 output.
				AN5	I	Analog	Analog input 5.
9	26	26	24	RE1/P3B/AN6			
				RE1	I/O	ST	Digital I/O.
				P3B	O	CMOS	Enhanced CCP3 PWM output.
				AN6	I	Analog	Analog input 6.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power.

Note 1: Default pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

2: Alternate pin assignment for P2B, T3CKI, CCP3/P3A and CCP2/P2A when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are clear.

9.0 INTERRUPTS

The PIC18(L)F2X/4XK22 devices have multiple interrupt sources and an interrupt priority feature that allows most interrupt sources to be assigned a high or low priority level (INT0 does not have a priority bit, it is always a high priority). The high priority interrupt vector is at 0008h and the low priority interrupt vector is at 0018h. A high priority interrupt event will interrupt a low priority interrupt that may be in progress.

There are 19 registers used to control interrupt operation.

These registers are:

- INTCON, INTCON2, INTCON3
- PIR1, PIR2, PIR3, PIR4, PIR5
- PIE1, PIE2, PIE3, PIE4, PIE5
- IPR1, IPR2, IPR3, IPR4, IPR5
- RCON

It is recommended that the Microchip header files supplied with MPLAB® IDE be used for the symbolic bit names in these registers. This allows the assembler/ compiler to automatically take care of the placement of these bits within the specified register.

In general, interrupt sources have three bits to control their operation. They are:

- **Flag bit** to indicate that an interrupt event occurred
- **Enable bit** that allows program execution to branch to the interrupt vector address when the flag bit is set
- **Priority bit** to select high priority or low priority

9.1 Mid-Range Compatibility

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC® microcontroller mid-range devices. In Compatibility mode, the interrupt priority bits of the IPRx registers have no effect. The PEIE/GIEL bit of the INTCON register is the global interrupt enable for the peripherals. The PEIE/GIEL bit disables only the peripheral interrupt sources and enables the peripheral interrupt sources when the GIE/GIEH bit is also set. The GIE/GIEH bit of the INTCON register is the global interrupt enable which enables all non-peripheral interrupt sources and disables all interrupt sources, including the peripherals. All interrupts branch to address 0008h in Compatibility mode.

9.2 Interrupt Priority

The interrupt priority feature is enabled by setting the IPEN bit of the RCON register. When interrupt priority is enabled the GIE/GIEH and PEIE/GIEL global interrupt enable bits of Compatibility mode are replaced by the GIEH high priority, and GIEL low priority, global interrupt enables. When set, the GIEH bit of the INTCON register enables all interrupts that have their associated IPRx register or INTCONx register priority bit set (high priority). When clear, the GIEH bit disables all interrupt sources including those selected as low priority. When clear, the GIEL bit of the INTCON register disables only the interrupts that have their associated priority bit cleared (low priority). When set, the GIEL bit enables the low priority sources when the GIEH bit is also set.

When the interrupt flag, enable bit and appropriate Global Interrupt Enable (GIE) bit are all set, the interrupt will vector immediately to address 0008h for high priority, or 0018h for low priority, depending on level of the interrupting source's priority bit. Individual interrupts can be disabled through their corresponding interrupt enable bits.

9.3 Interrupt Response

When an interrupt is responded to, the Global Interrupt Enable bit is cleared to disable further interrupts. The GIE/GIEH bit is the Global Interrupt Enable when the IPEN bit is cleared. When the IPEN bit is set, enabling interrupt priority levels, the GIEH bit is the high priority global interrupt enable and the GIEL bit is the low priority Global Interrupt Enable. High priority interrupt sources can interrupt a low priority interrupt. Low priority interrupts are not processed while high priority interrupts are in progress.

The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (0008h or 0018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits in the INTCONx and PIRx registers. The interrupt flag bits must be cleared by software before re-enabling interrupts to avoid repeating the same interrupt.

The "return from interrupt" instruction, `RETFIE`, exits the interrupt routine and sets the GIE/GIEH bit (GIEH or GIEL if priority levels are used), which re-enables interrupts.

For external interrupt events, such as the INT pins or the PORTB interrupt-on-change, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one-cycle or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding enable bits or the Global Interrupt Enable bit.

10.5 PORTD Registers

Note: PORTD is only available on 40-pin and 44-pin devices.

PORTD is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISD. Setting a TRISD bit (= 1) will make the corresponding PORTD pin an input (i.e., disable the output driver). Clearing a TRISD bit (= 0) will make the corresponding PORTD pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin).

The Data Latch register (LATD) is also memory mapped. Read-modify-write operations on the LATD register read and write the latched output value for PORTD.

All pins on PORTD are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

All of the PORTD pins are multiplexed with analog and digital peripheral modules. See Table 10-11.

Note: On a Power-on Reset, these pins are configured as analog inputs.

EXAMPLE 10-4: INITIALIZING PORTD

```
MOVLB   0xF     ; Set BSR for banked SFRs
CLRF    PORTD   ; Initialize PORTD by
                ; clearing output
                ; data latches
CLRF    LATD    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISD   ; Set RD<3:0> as inputs
                ; RD<5:4> as outputs
                ; RD<7:6> as inputs
MOVLW   30h     ; Value used to
                ; enable digital inputs
MOVWF   ANSELD  ; RD<3:0> dig input enable
                ; RC<7:6> dig input enable
```

10.5.1 PORTD OUTPUT PRIORITY

Each PORTD pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the higher priority. Table 10-4 lists the PORTD pin functions from the highest to the lowest priority.

Analog input functions, such as ADC, comparator and SR latch inputs, are not shown in the priority lists.

These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown below.

TABLE 10-11: PORTD I/O SUMMARY

Pin Name	Function	TRIS Setting	ANSEL setting	Pin Type	Buffer Type	Description
RD0/SCK2/SCL2/AN20	RD0	0	0	O	DIG	LATD<0> data output; not affected by analog input.
		1	0	I	ST	PORTD<0> data input; disabled when analog input enabled.
	SCK2	0	0	O	DIG	MSSP2 SPI Clock output.
		1	0	I	ST	MSSP2 SPI Clock input.
	SCL2	0	0	O	DIG	MSSP2 I^2C Clock output.
		1	0	I	I^2C	MSSP2 I^2C Clock input.
	AN20	1	1	I	AN	Analog input 20.
RD1/CCP4/SDI2/SDA2/AN21	RD1	0	0	O	DIG	LATD<1> data output; not affected by analog input.
		1	0	I	ST	PORTD<1> data input; disabled when analog input enabled.
	CCP4	0	0	O	DIG	Compare 4 output/PWM 4 output.
		1	0	I	ST	Capture 4 input.
	SDI2	1	0	I	ST	MSSP2 SPI data input.
	SDA2	0	0	O	DIG	MSSP2 I^2C data output.
		1	0	I	I^2C	MSSP2 I^2C data input.
	AN21	1	1	I	AN	Analog input 21.
RD2/P2B/AN22	RD2	0	0	O	DIG	LATD<2> data output; not affected by analog input.
		1	0	I	ST	PORTD<2> data input; disabled when analog input enabled.
	P2B(1)	0	0	O	DIG	Enhanced CCP2 PWM output 2.
	AN22	1	1	I	AN	Analog input 22.
RD3/P2C/$\overline{SS2}$/AN23	RD3	0	0	O	DIG	LATD<3> data output; not affected by analog input.
		1	0	I	ST	PORTD<3> data input; disabled when analog input enabled.
	P2C	0	0	O	DIG	Enhanced CCP2 PWM output 4.
	$\overline{SS2}$	1	0	I	TTL	MSSP2 SPI slave select input.
	AN23	1	1	I	AN	Analog input 23.
RD4/P2D/SDO2/AN24	RD4	0	0	O	DIG	LATD<4> data output; not affected by analog input.
		1	0	I	ST	PORTD<4> data input; disabled when analog input enabled.
	P2D	0	0	O	DIG	Enhanced CCP2 PWM output 3.
	SDO2	0	0	O	DIG	MSSP2 SPI data output.
	AN24	1	1	I	AN	Analog input 24.
RD5/P1B/AN25	RD5	0	0	O	DIG	LATD<5> data output; not affected by analog input.
		1	0	I	ST	PORTD<5> data input; disabled when analog input enabled.
	P1B	0	0	O	DIG	Enhanced CCP1 PWM output 2.
	AN25	1	1	I	AN	Analog input 25.

Legend: AN = Analog input or output; TTL = TTL compatible input; HV = High Voltage; OD = Open Drain; XTAL = Crystal; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C.

Note 1: Default pin assignment for P2B, T3CKI, CCP3 and CCP2 when Configuration bits PB2MX, T3CMX, CCP3MX and CCP2MX are set.

12.8 Timer1/3/5 Interrupt

The Timer1/3/5 register pair (TMRxH:TMRxL) increments to FFFFh and rolls over to 0000h. When Timer1/3/5 rolls over, the Timer1/3/5 interrupt flag bit of the PIR1/2/5 register is set. To enable the interrupt on rollover, you must set these bits:

- TMRxON bit of the TxCON register
- TMRxIE bits of the PIE1, PIE2 or PIE5 registers
- PEIE/GIEL bit of the INTCON register
- GIE/GIEH bit of the INTCON register

The interrupt is cleared by clearing the TMRxIF bit in the Interrupt Service Routine.

For more information on selecting high or low priority status for the Timer1/3/5 Overflow Interrupt, see **Section 9.0 "Interrupts"**.

Note:	The TMRxH:TMRxL register pair and the TMRxIF bit should be cleared before enabling interrupts.

12.9 Timer1/3/5 Operation During Sleep

Timer1/3/5 can only operate during Sleep when set up in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMRxON bit of the TxCON register must be set
- TMRxIE bit of the PIE1/2/5 register must be set
- PEIE/GIEL bit of the INTCON register must be set
- $\overline{\text{TxSYNC}}$ bit of the TxCON register must be set
- TMRxCS bits of the TxCON register must be configured
- TxSOSCEN bit of the TxCON register must be configured

The device will wake-up on an overflow and execute the next instruction. If the GIE/GIEH bit of the INTCON register is set, the device will call the Interrupt Service Routine.

The secondary oscillator will continue to operate in Sleep regardless of the $\overline{\text{TxSYNC}}$ bit setting.

12.10 ECCP/CCP Capture/Compare Time Base

The CCP modules use the TMRxH:TMRxL register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMRxH:TMRxL register pair is copied into the CCPRxH:CCPRxL register pair on a configured event.

In Compare mode, an event is triggered when the value CCPRxH:CCPRxL register pair matches the value in the TMRxH:TMRxL register pair. This event can be a Special Event Trigger.

For more information, see **Section 14.0 "Capture/Compare/PWM Modules"**.

12.11 ECCP/CCP Special Event Trigger

When any of the CCP's are configured to trigger a special event, the trigger will clear the TMRxH:TMRxL register pair. This special event does not cause a Timer1/3/5 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPRxH:CCPRxL register pair becomes the period register for Timer1/3/5.

Timer1/3/5 should be synchronized and FOSC/4 should be selected as the clock source in order to utilize the Special Event Trigger. Asynchronous operation of Timer1/3/5 can cause a Special Event Trigger to be missed.

In the event that a write to TMRxH or TMRxL coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see **Section 17.2.8 "Special Event Trigger"**.

FIGURE 15-15: I^2C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)

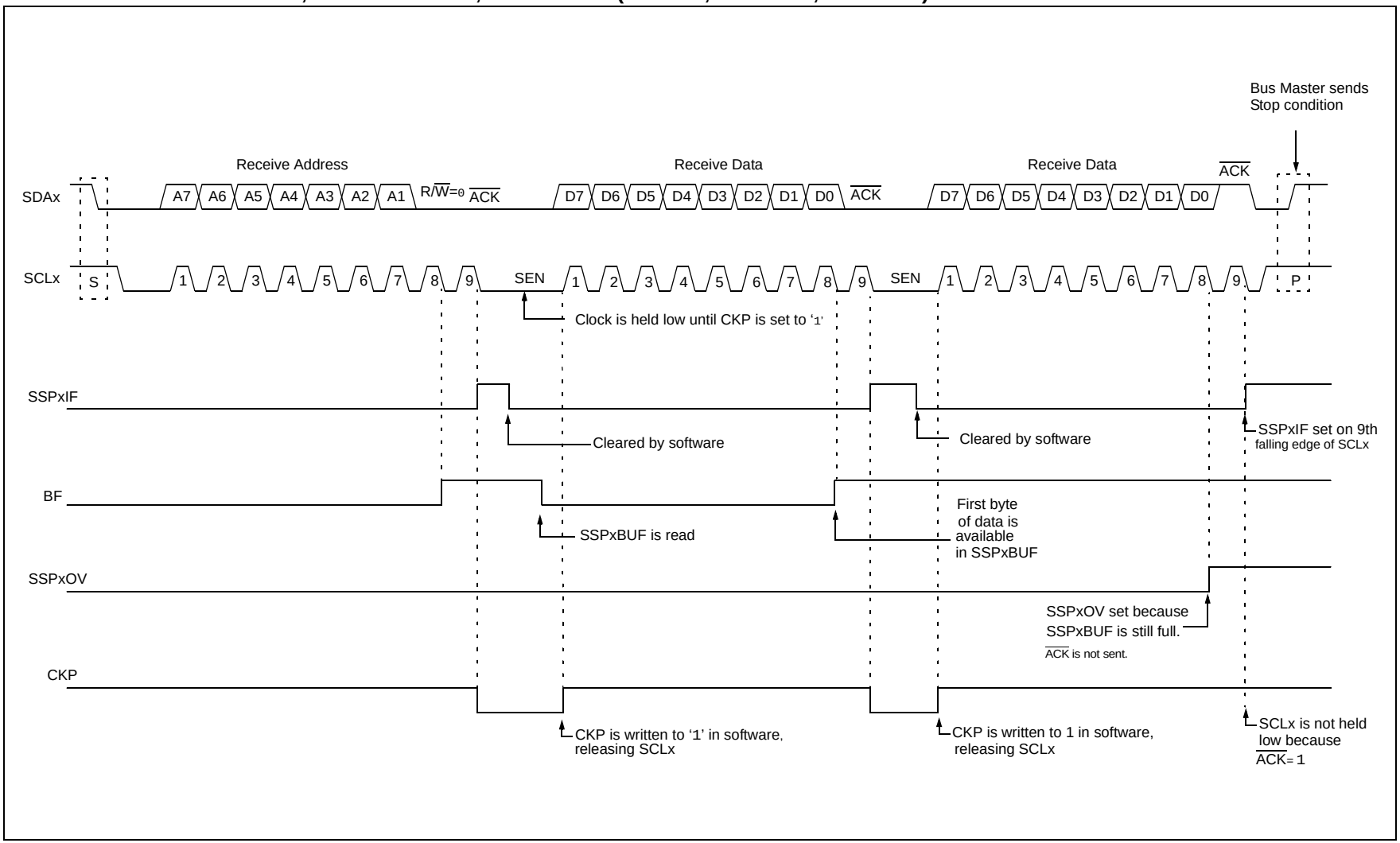


FIGURE 15-17: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)

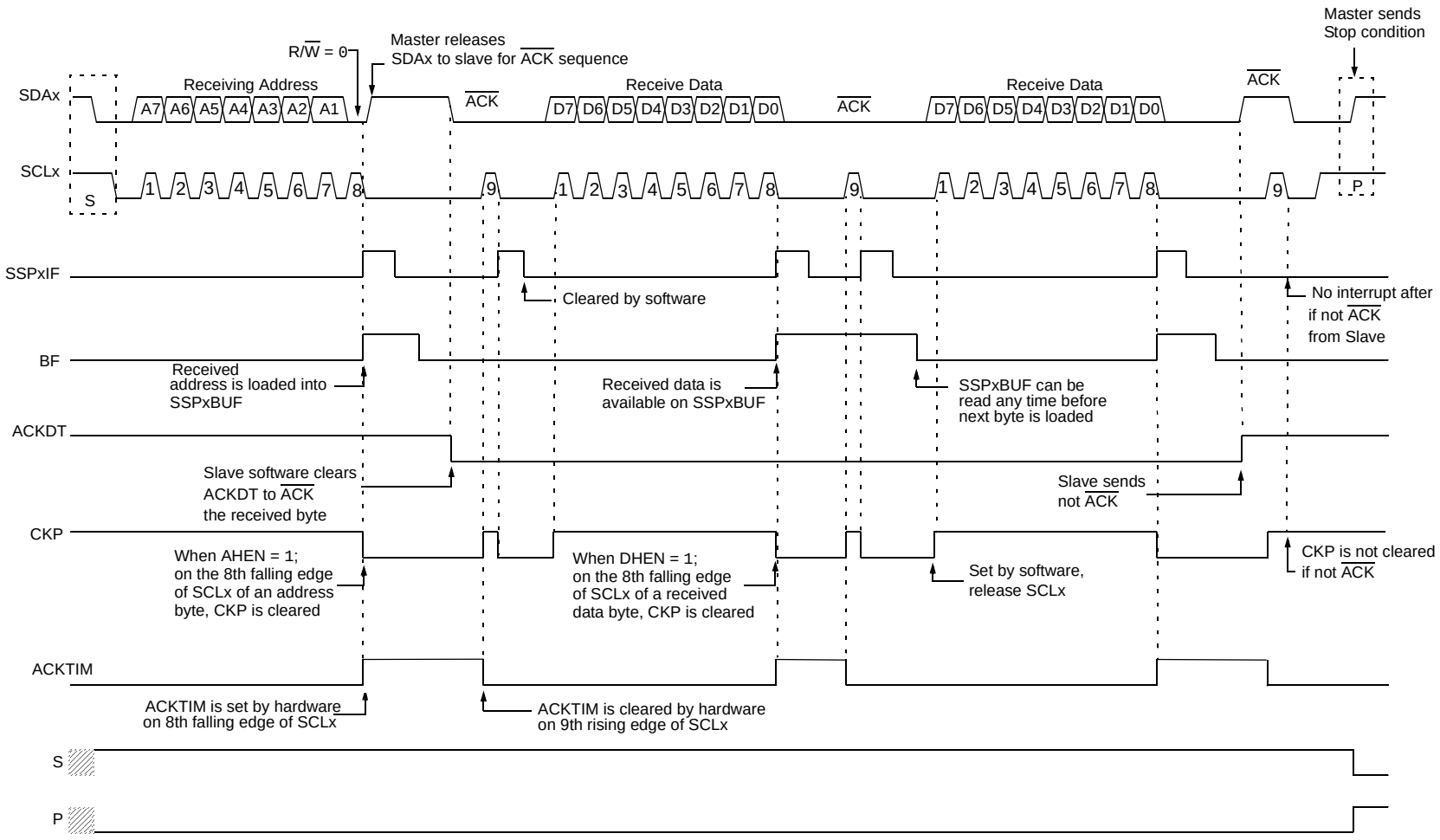


FIGURE 15-34: BUS COLLISION DURING START CONDITION (SCLx = 0)

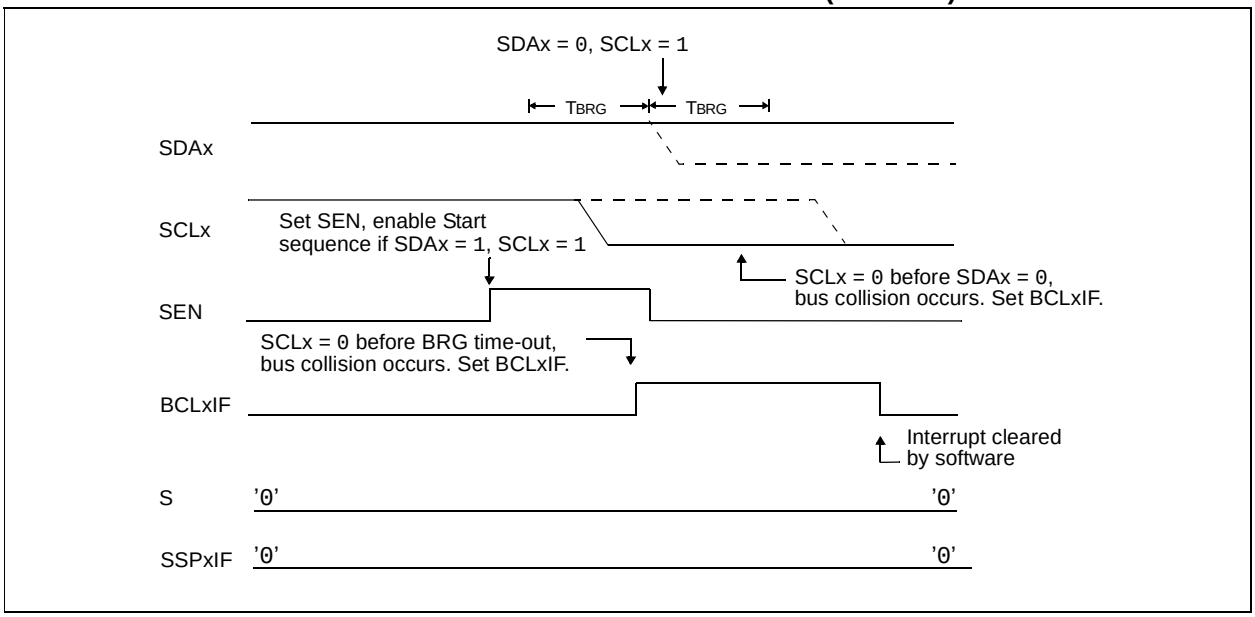
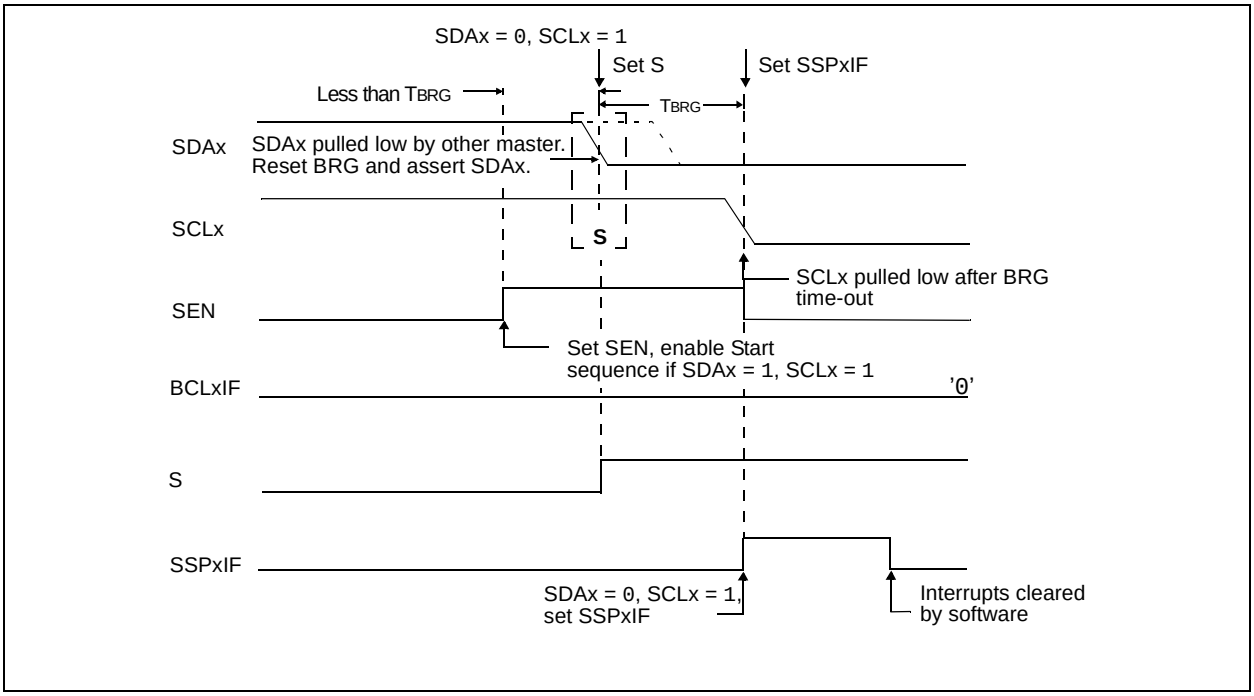


FIGURE 15-35: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION



18.8 Additional Comparator Features

There are four additional comparator features:

- Simultaneous read of comparator outputs
- Internal reference selection
- Hysteresis selection
- Output Synchronization

18.8.1 SIMULTANEOUS COMPARATOR OUTPUT READ

The MC1OUT and MC2OUT bits of the CM2CON1 register are mirror copies of both comparator outputs. The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note 1:	Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

18.8.2 INTERNAL REFERENCE SELECTION

There are two internal voltage references available to the non-inverting input of each comparator. One of these is the Fixed Voltage Reference (FVR) and the other is the variable Digital-to-Analog Converter (DAC). The CxRSEL bit of the CM2CON1 register determines which of these references is routed to the Comparator Voltage reference output (CxVREF). Further routing to the comparator is accomplished by the CxR bit of the CMxCON0 register. See **Section 21.0 “Fixed Voltage Reference (FVR)”** and Figure 18-2 for more detail.

18.8.3 COMPARATOR HYSTERESIS

Each Comparator has a selectable hysteresis feature. The hysteresis can be enabled by setting the CxHYS bit of the CM2CON1 register. See **Section 27.0 “Electrical Specifications”** for more details.

18.8.4 SYNCHRONIZING COMPARATOR OUTPUT TO TIMER1

The Comparator Cx output can be synchronized with Timer1 by setting the CxSYNC bit of the CM2CON1 register. When enabled, the Cx output is latched on the falling edge of the Timer1 source clock. To prevent a race condition when gating Timer1 clock with the comparator output, Timer1 increments on the rising edge of its clock source, and the falling edge latches the comparator output. See the Comparator Block Diagram (Figure 18-2) and the Timer1 Block Diagram (Figure 12-1) for more information.

Note 1:	The comparator synchronized output should not be used to gate the external Timer1 clock when the Timer1 synchronizer is enabled.
2:	The Timer1 prescale should be set to 1:1 when synchronizing the comparator output as unexpected results may occur with other prescale values.

REGISTER 24-11: CONFIG7H: CONFIGURATION REGISTER 7 HIGH

U-0	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
—	EBTRB	—	—	—	—	—	—
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’
-n = Value when device is unprogrammed	C = Clearable only bit

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **EBTRB:** Boot Block Table Read Protection bit
1 = Boot Block not protected from table reads executed in other blocks
0 = Boot Block protected from table reads executed in other blocks

bit 5-0 **Unimplemented:** Read as ‘0’

REGISTER 24-12: DEVID1: DEVICE ID REGISTER 1

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’
-n = Value when device is unprogrammed	C = Clearable only bit

bit 7-5 **DEV<2:0>:** Device ID bits
These bits, together with DEV<10:3> in DEVID2, determine the device ID.
See Table 24-2 for complete Device ID list.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits indicate the device revision.

REGISTER 24-13: DEVID2: DEVICE ID REGISTER 2

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’
-n = Value when device is unprogrammed	C = Clearable only bit

bit 7-0 **DEV<10:3>:** Device ID bits
These bits, together with DEV<2:0> in DEVID1, determine the device ID.
See Table 24-2 for complete Device ID list.

BZ **Branch if Zero**

Syntax: BZ n

Operands: -128 ≤ n ≤ 127

Operation: if ZERO bit is '1'
(PC) + 2 + 2n → PC

Status Affected: None

Encoding:

1110	0000	nnnn	nnnn

Description: If the ZERO bit is '1', then the program will branch.
The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is then a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:
If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	Write to PC
No operation	No operation	No operation	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BZ Jump

Before Instruction
PC = address (HERE)
After Instruction
If ZERO = 1;
PC = address (Jump)
If ZERO = 0;
PC = address (HERE + 2)

CALL **Subroutine Call**

Syntax: CALL k {,s}

Operands: 0 ≤ k ≤ 1048575
s ∈ [0,1]

Operation: (PC) + 4 → TOS,
k → PC<20:1>,
if s = 1
(W) → WS,
(Status) → STATUSS,
(BSR) → BSRS

Status Affected: None

Encoding:

1st word (k<7:0>)	1110	110s	$k_7$kkk	kkkk$_0$
2nd word(k<19:8>)	1111	k_{19}kkk	kkkk	kkkk$_8$

Description: Subroutine call of entire 2-Mbyte memory range. First, return address (PC + 4) is pushed onto the return stack. If 's' = 1, the W, STATUS and BSR registers are also pushed into their respective shadow registers, WS, STATUSS and BSRS. If 's' = 0, no update occurs (default). Then, the 20-bit value 'k' is loaded into PC<20:1>. CALL is a 2-cycle instruction.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'<7:0>,	PUSH PC to stack	Read literal 'k'<19:8>, Write to PC
No operation	No operation	No operation	No operation

Example: HERE CALL THERE, 1

Before Instruction
PC = address (HERE)
After Instruction
PC = address (THERE)
TOS = address (HERE + 4)
WS = W
BSRS = BSR
STATUSS = Status

27.2 DC Characteristics: Power-Down Current, PIC18(L)F2X/4XK22

PIC18LF2X/4XK22		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C						
PIC18F2X/4XK22		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C						
Param No.	**Device Characteristics**	**Typ +25°C**	**Typ +60°C**	**Max +85°C**	**Max +125°C**	**Units**	**Conditions**	
							VDD	**Notes**
Power-down Base Current (IPD)(1)								
D006	Sleep mode	0.01	0.04	2	10	µA	1.8V	WDT, BOR, FVR and SOSC disabled, all Peripherals inactive
		0.01	0.06	2	10	µA	3.0V	
		12	13	25	35	µA	2.3V	
		13	14	30	40	µA	3.0V	
		13	14	35	50	µA	5.0V	
Power-down Module Differential Current (delta IPD)								
D007	Watchdog Timer	0.3	0.3	2.5	2.5	µA	1.8V	
		0.5	0.5	2.5	2.5	µA	3.0V	
		0.35	0.35	5.0	5.0	µA	2.3V	
		0.5	0.5	5.0	5.0	µA	3.0V	
		0.5	0.5	5.0	5.0	µA	5.0V	
D008	Brown-out Reset(2)	8	8.5	15	16	µA	2.0V	
		9	9.5	15	16	µA	3.0V	
		3.4	3.4	15	16	µA	2.3V	
		3.8	3.8	15	16	µA	3.0V	
		5.2	5.2	15	16	µA	5.0V	
D010	High/Low Voltage Detect(2)	6.5	6.7	15	15	µA	2.0V	
		7	7.5	15	15	µA	3.0V	
		2.1	2.1	15	15	µA	2.3V	
		2.4	2.4	15	15	µA	3.0V	
		3.2	3.2	15	15	µA	5.0V	
D011	Secondary Oscillator	0.5	1	3	10	µA	1.8V	32 kHz on SOSC
		0.6	1.1	4	10	µA	3.0V	
		0.5	1	3	10	µA	2.3V	
		0.6	1.1	4	10	µA	3.0V	
		0.6	1.1	5	10	µA	5.0V	

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: On PIC18LF2X/4XK22 the BOR, HLVD and FVR enable internal band gap reference. With more than one of these modules enabled, the current consumption will be less than the sum of the specifications. On PIC18F2X/4XK22, the internal band gap reference is always enabled and its current consumption is included in the Power-down Base Current (IPD).

3: A/D converter differential currents apply only in Run mode. In Sleep or Idle mode both the ADC and the FRC turn off as soon as conversion (if any) is complete.

27.6 DC Characteristics: Primary Idle Supply Current, PIC18(L)F2X/4XK22

PIC18LF2X/4XK22		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
PIC18F2X/4XK22		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	**Device Characteristics**	**Typ**	**Max**	**Units**	**Conditions**		
D100	Supply Current (IDD)[1],[2]	0.030	0.050	mA	-40°C to +125°C	VDD = 1.8V	Fosc = 1 MHz (**PRI_IDLE** mode, ECM source)
D101		0.045	0.065	mA	-40°C to +125°C	VDD = 3.0V	
D102		0.06	0.12	mA	-40°C to +125°C	VDD = 2.3V	Fosc = 1 MHz (**PRI_IDLE** mode, ECM source)
D103		0.08	0.15	mA	-40°C to +125°C	VDD = 3.0V	
D104		0.13	0.20	mA	-40°C to +125°C	VDD = 5.0V	
D105		0.45	0.8	mA	-40°C to +125°C	VDD = 1.8V	Fosc = 20 MHz (**PRI_IDLE** mode, ECH source)
D106		0.70	1.0	mA	-40°C to +125°C	VDD = 3.0V	
D107		0.55	0.8	mA	-40°C to +125°C	VDD = 2.3V	Fosc = 20 MHz (**PRI_IDLE** mode, ECH source)
D108		0.75	1.0	mA	-40°C to +125°C	VDD = 3.0V	
D109		0.90	1.2	mA	-40°C to +125°C	VDD = 5.0V	
D110		2.25	3.0	mA	-40°C to +125°C	VDD = 3.0V	Fosc = 64 MHz (**PRI_IDLE** mode, ECH source)
D111		2.25	3.0	mA	-40°C to +125°C	VDD = 3.0V	Fosc = 64 MHz (**PRI_IDLE** mode, ECH source)
D112		2.60	3.5	mA	-40°C to +125°C	VDD = 5.0V	
D113		0.35	0.6	mA	-40°C to +125°C	VDD = 1.8V	Fosc = 4 MHz 16 MHz Internal (**PRI_IDLE** mode, ECM + PLL source)
D114		0.55	0.8	mA	-40°C to +125°C	VDD = 3.0V	
D115		0.45	0.6	mA	-40°C to +125°C	VDD = 2.3V	Fosc = 4 MHz 16 MHz Internal (**PRI_IDLE** mode, ECM + PLL source)
D116		0.60	0.9	mA	-40°C to +125°C	VDD = 3.0V	
D117		0.70	1.0	mA	-40°C to +125°C	VDD = 5.0V	
D118		2.2	3.0	mA	-40°C to +125°C	VDD = 3.0V	Fosc = 16 MHz 64 MHz Internal (**PRI_IDLE** mode, ECH + PLL source)
D119		2.2	3.0	mA	-40°C to +125°C	VDD = 3.0V	Fosc = 16 MHz 64 MHz Internal (**PRI_IDLE** mode, ECH + PLL source)
D120		2.5	3.5	mA	-40°C to +125°C	VDD = 5.0V	

Note 1: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

Test condition: All Peripheral Module Control bits in PMD0, PMD1 and PMD2 set to '1'.

2: The test conditions for all IDD measurements in active operation mode are:

All I/O pins set as outputs driven to Vss;
MCLR = VDD;
OSC1 = external square wave, from rail-to-rail (PRI_RUN and PRI_IDLE only).

FIGURE 27-13: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)

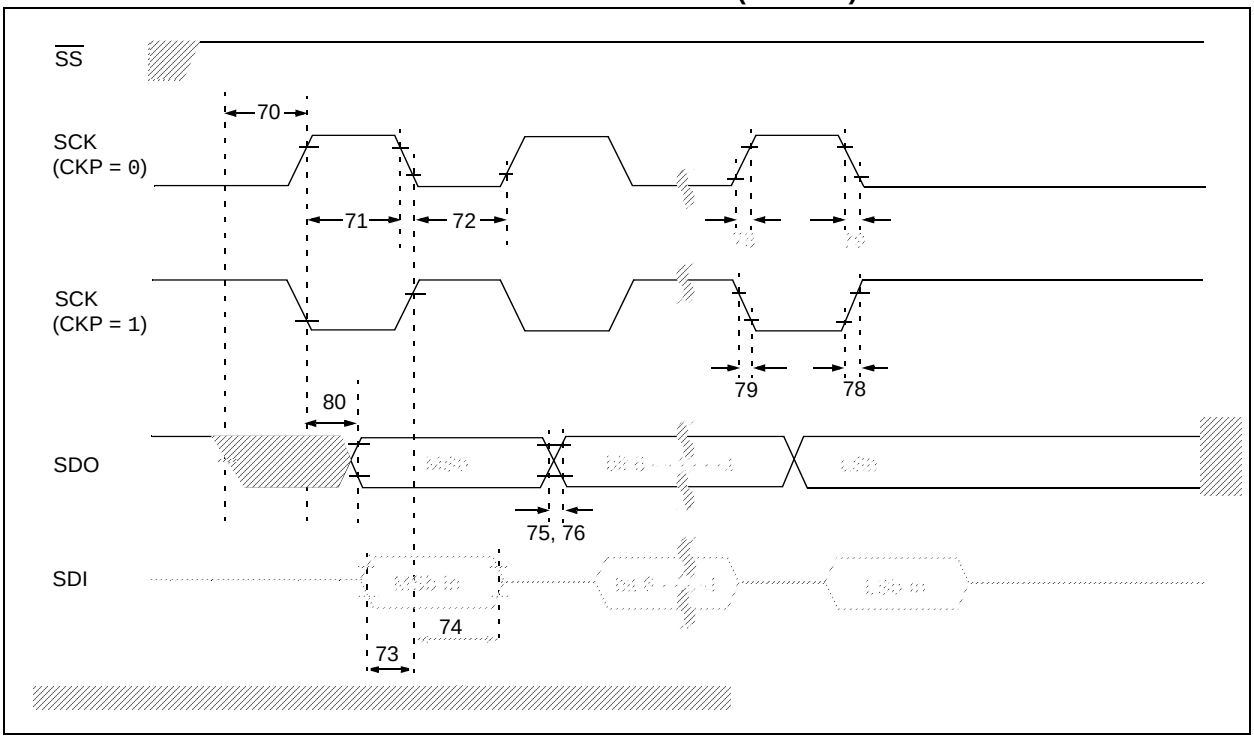
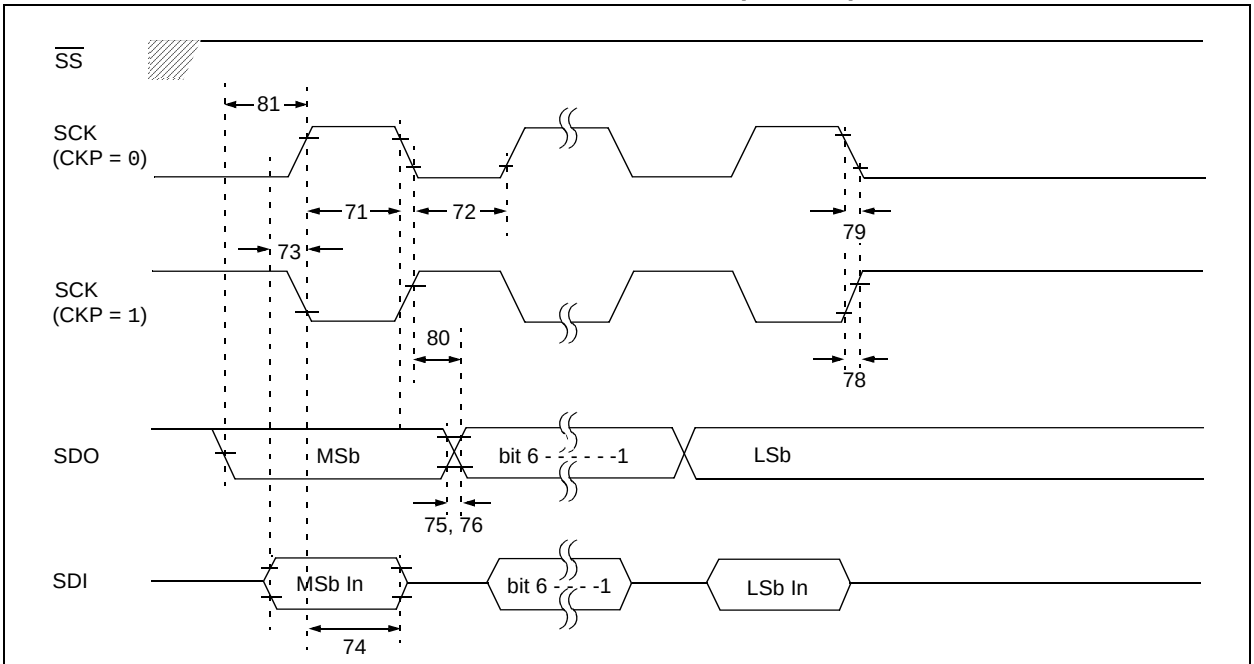


FIGURE 27-14: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)

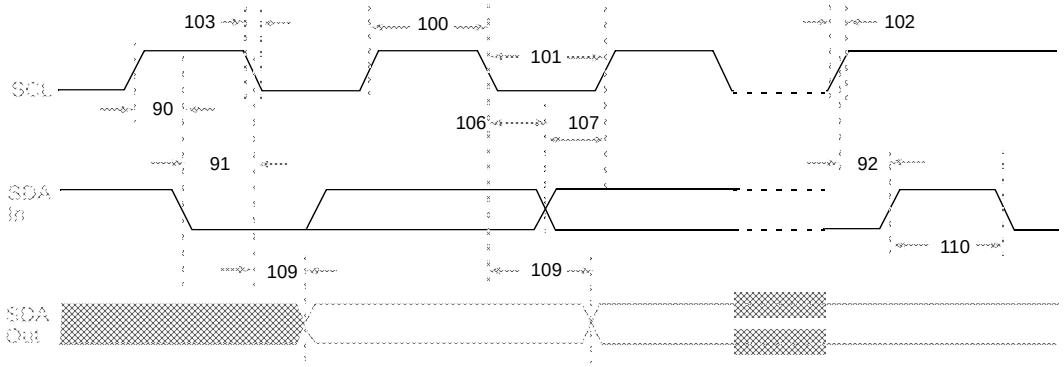


Note: Refer to Figure 27-6 for load conditions.

TABLE 27-15: I²C BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—		
91	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—		
92	TSU:STO	Stop Condition Setup Time	100 kHz mode	4700	—	ns	
			400 kHz mode	600	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—		

FIGURE 27-18: I²C BUS DATA TIMING



Note: Refer to Figure 27-6 for load conditions.

FIGURE 28-13: PIC18LF2X/4XK22 DELTA IPD COMPARATOR HIGH-POWER MODE

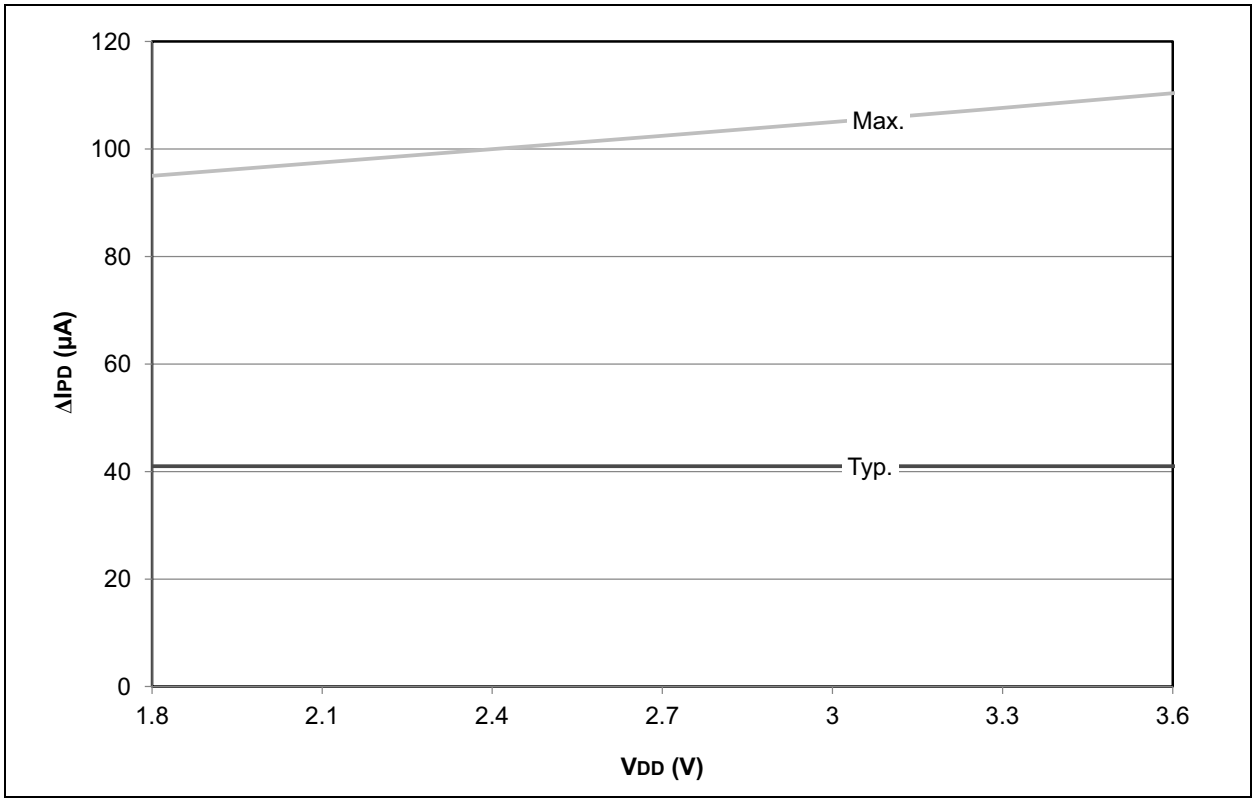


FIGURE 28-14: PIC18F2X/4XK22 DELTA IPD COMPARATOR HIGH-POWER MODE

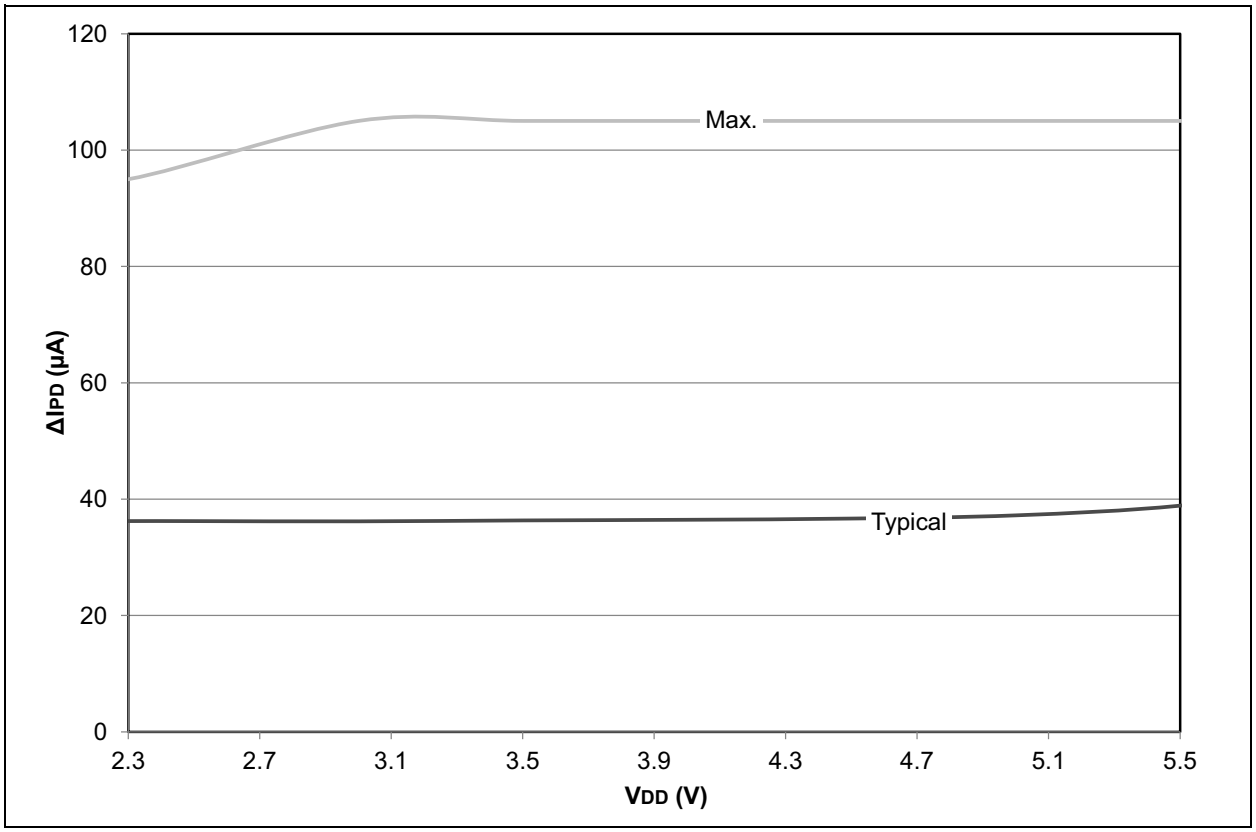
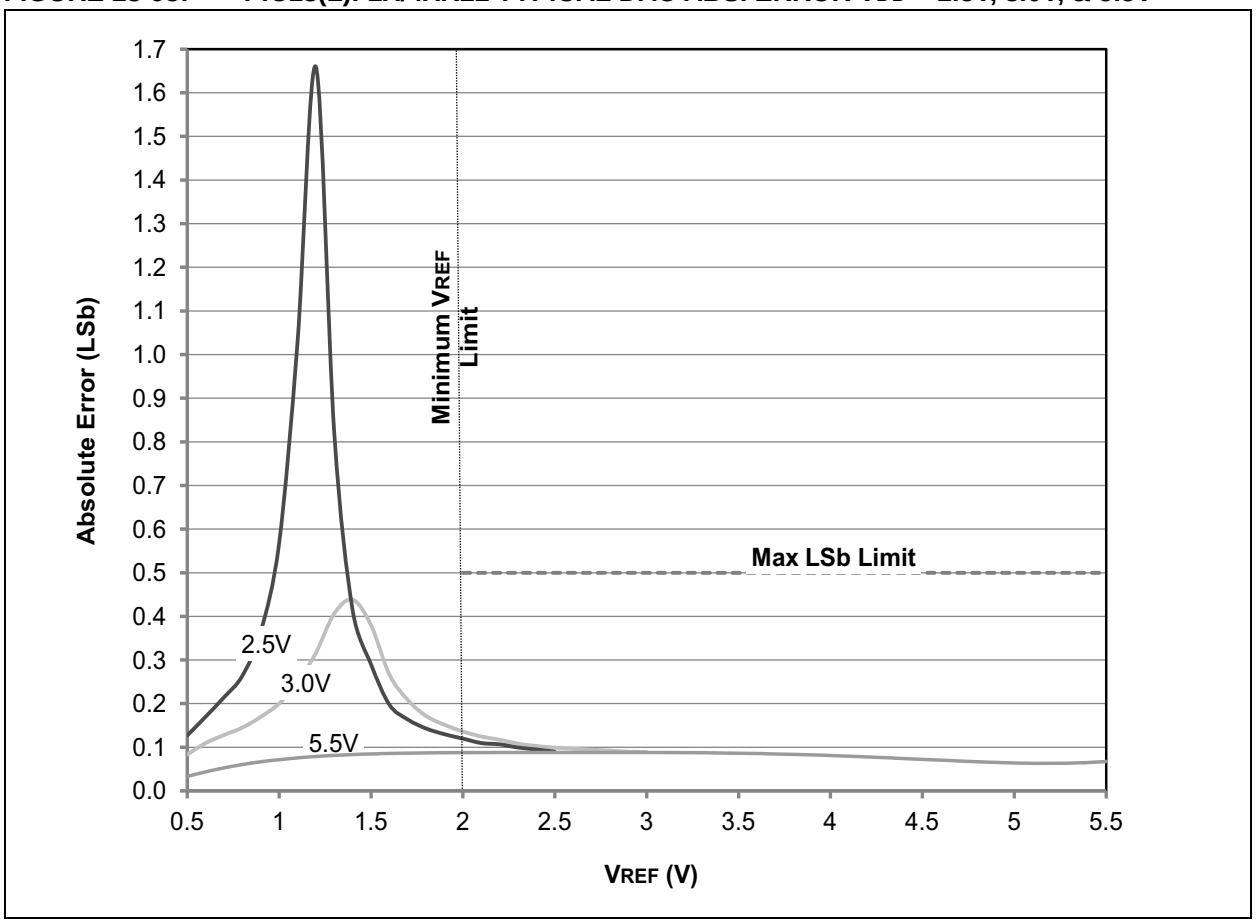
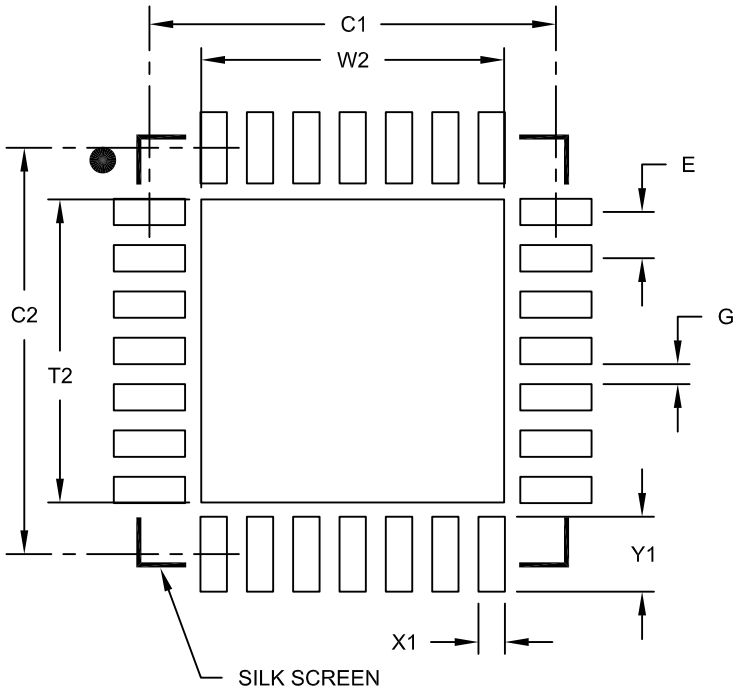


FIGURE 28-93: PIC18(L)F2X/4XK22 TYPICAL DAC ABS. ERROR V_{DD} = 2.5V, 3.0V, & 5.5V



28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features[1]	PIC18F23K22 PIC18LF23K22	PIC18F24K22 PIC18LF24K22	PIC18F25K22 PIC18LF25K22	PIC18F26K22 PIC18LF26K22	PIC18F43K22 PIC18LF43K22	PIC18F44K22 PIC18LF44K22	PIC18F45K22 PIC18LF45K22	PIC18F46K22 PIC18LF46K22
Program Memory (Bytes)	8192	16384	32768	65536	8192	16384	32768	65536
SRAM (Bytes)	512	768	1536	3896	512	768	1536	3896
EEPROM (Bytes)	256	256	256	1024	256	256	256	1024
Interrupt Sources	26	26	33	33	26	26	33	33
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules (CCP)	2	2	2	2	2	2	2	2
Enhanced CCP Modules (ECCP) Full Bridge	1	1	1	1	2	2	2	2
ECCP Module Half Bridge	2	2	2	2	1	1	1	1
10-bit Analog-to-Digital Module	17 input channels	17 input channels	17 input channels	17 input channels	28 input channels	28 input channels	28 input channels	28 input channels
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN 28-pin UQFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN	40-pin PDIP 40-pin UQFN 44-pin TQFP 44-pin QFN

Note 1: PIC18FXXK22: operating voltage, 2.3V-5.5V.

PIC18LFXXK22: operating voltage, 1.8V-3.6V.