Renesas Electronics America Inc - UPD78F9418AGK-9EU-A Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	78K0S
Core Size	8-Bit
Speed	5MHz
Connectivity	3-Wire SIO, UART/USART
Peripherals	LCD, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f9418agk-9eu-a

(2) Non-port pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P24/TI0
INTP1				P25/TI1
INTP2				P26/TO5
INTP3				P27/CPT5
KR0 to KR5	Input	Key return signal detection	Input	P40 to P45
SI	Input	Serial interface serial data input	Input	P22/RxD
SO	Output	Serial interface serial data output	Input	P21/TxD
$\overline{SCK}$	I/O	Serial interface serial clock input/output	Input	P20/ASCK
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK}$
RxD	Input	Serial data input for asynchronous serial interface	Input	P22/SI
TxD	Output	Serial data output for asynchronous serial interface	Input	P21/SO
TI0	Input	External count clock input to 8-bit timer (TM00)	Input	P24/INTP0
TI1	Input	External count clock input to 8-bit timer (TM01)	Input	P25/INTP1
TO2	Output	8-bit timer (TM02) output	Input	P23/CMPTOUT0
TO5	Output	16-bit timer (TM50) output	Input	P26/INTP2
CPT5	Input	Capture edge input	Input	P27/INTP3
CMPTOUT0	Output	Comparator output	Input	P23/TO2
CMPIN0	Input	Comparator input	Input	P60/ANI0
CMPREF0	Input	Comparator reference voltage input	Input	P61/ANI1
ANI0	Input	A/D converter analog input	Input	P60/CMPIN0
ANI1				P61/CMPREF0
ANI2 to ANI6				P62 to P66
AV_{REF}	–	A/D converter reference voltage	–	–
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
S0 to S15	Output	LCD controller/driver segment signal output	Output	–
S16 to S19			Input	P93 to P90
S20 to S27				P87 to P80
COM0 to COM3	Output	LCD controller/driver common signal output	Output	–
V_{LC0} to V_{LC2}	–	LCD driving voltage	–	–
BIAS	–	Supply voltage for LCD driving	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
RESET	Input	System reset input	Input	–

3.3.2 Immediate addressing

[Function]

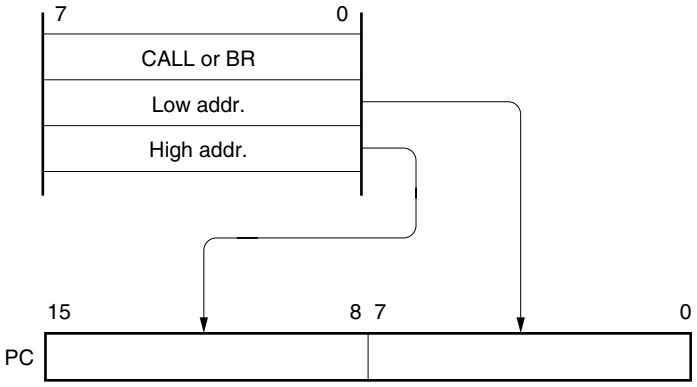
Immediate data in the instruction word is transferred to the program counter (PC) and branched.

This function is carried out when the CALL !addr16 or BR !addr16 instruction is executed.

The CALL !addr16 and BR !addr16 instructions can be branched to any location in the memory space.

[Illustration]

In case of CALL !addr16 and BR !addr16 instructions



3.4.4 Register addressing

[Function]

In the register addressing mode, general-purpose registers are accessed as operands. The general-purpose register to be accessed is specified by the register specification code or functional name in the instruction code. Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the instruction code.

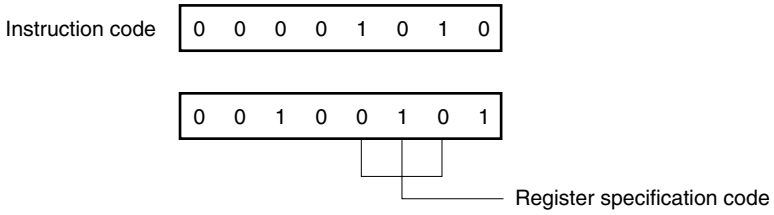
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

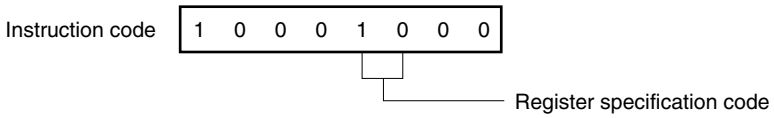
r and rp can be described using absolute names (R0 to R7 and RP0 to RP3) as well as functional names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; When selecting the C register for r



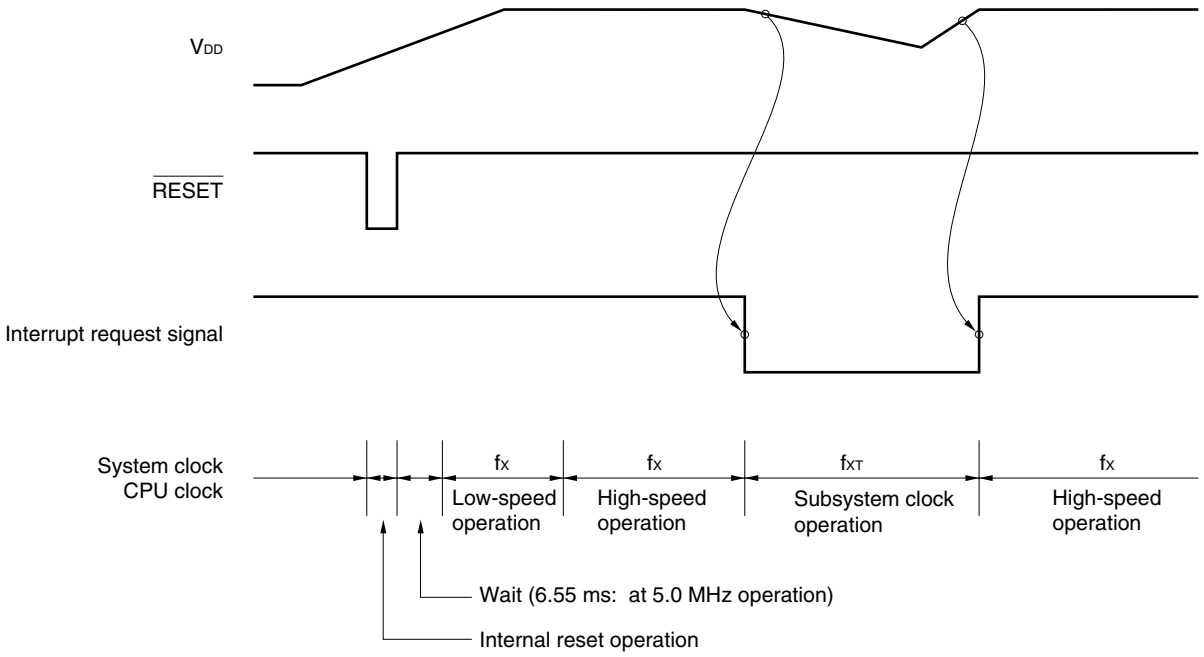
INCW DE; When selecting the DE register pair for rp



5.6.2 Switching between system clock and CPU clock

The following figure illustrates how the CPU clock and system clock are switched.

Figure 5-8. Switching Between System Clock and CPU Clock



<1> The CPU is reset when the $\overline{\text{RESET}}$ pin is made low on power application. Reset is released when the $\overline{\text{RESET}}$ pin is later made high, and the main system clock starts oscillating. At this time, the oscillation stabilization time (2^{15}/fx) is automatically secured.
After that, the CPU starts instruction execution at the low speed of the main system clock (1.6 μs at 5.0 MHz operation).

<2> After the time required for the V_{DD} voltage to rise to the level at which the CPU can operate at the high speed has elapsed, bit 1 (PCC1) of the processor clock control register (PCC) and bit 4 (CSS0) of the subclock control register (CSS) are rewritten so that the high-speed operation can be selected.

<3> A drop of the V_{DD} voltage is detected by an interrupt request signal. The clock is switched to the subsystem clock (at this moment, the subsystem clock must be in the stable oscillation status).

<4> Recovery of the V_{DD} voltage is detected by an interrupt request signal. Bit 7 (MCC) of PCC is set to 0, and the main system clock starts oscillating. After the time required for the oscillation to stabilize has elapsed, PCC1 and CSS0 are rewritten so that high-speed operation can be selected again.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

(2) Port mode register 2 (PM2)

This register sets input/output of port 2 in 1-bit units.

To use the P26/INTP2/TO5 pin for timer output, set PM26 and the output latch of P26 to 0.

PM2 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets PM2 to FFH.

Figure 6-3. Format of Port Mode Register 2

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W

PM26	P26 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

<Countermeasure B> When rewriting using 16-bit access

<1> Disable interrupts (TMMK50 = 1) and the inversion control of timer output (TOC50 = 0).

<2> Rewrite CR50 (16 bits).

<3> Wait for one cycle or more of the count clock.

<4> Clear the interrupt request flag (TMIF50).

<5> Enable timer interrupts/timer output inversion.

<Program example B> (count clock = 32/fx, CPU clock = fx)

```
TM50_VCT   SET1 TMMK50      ;  Disable timer interrupts
           CLR1 TMC50.3     ;  Disable timer output inversion
           MOVW AX,#xxyyH   ;  Set the rewrite value of CR50
           MOVW CR50,AX     ;  Rewrite CR50
           NOP
           NOP
            :               ;  16 NOP instructions (wait for 32/fx)Note
           NOP
           NOP
           CLR1 TMIF50      ;  Clear interrupt request flag
           CLR1 TMMK50      ;  Enable timer interrupts
           SET1 TMC50.3     ;  Enable timer output inversion
```

Note Clear the interrupt request flag (TMIF50) after waiting for one cycle or more of the count clock from the instruction rewriting CR50 (MOVW CR50, AX).

7.4.3 Operation as square-wave output (timer 02 only)

The 8-bit timer can generate a square-wave output of any frequency at intervals specified by the count value preset to 8-bit compare register 02 (CR02).

To operate 8-bit timer 02 as a square-wave output, make the settings in the following order.

<1> Set P23 to output mode (PM23 = 0), and set the output latch of P23 to 0
<2> Disable 8-bit timer counter 02 (TM02) operation (TCE02 (bit 0 of 8-bit timer mode control register 02 (TMC02)) = 1)
<3> Set the count clock of 8-bit timer 02 (see **Table 7-9**), and enable TO2 to output (TOE02 (bit 0 of TMC02) = 1)
<4> Set the count value to CR02
<5> Enable TM02 operation (TCE02 = 1)

When the count value of 8-bit timer counter 02 (TM02) matches the value set in CR02, the TO2/P23/CMPTOUT0 pin output is inverted. Through application of this mechanism, square waves of any frequency can be output. As soon as a match occurs, the TM02 value is cleared to 00H, then counting continues count and an interrupt request signal (INTTM02) is generated.

Setting bit 7 of TMC02 (TCE02) to 0 clears the square-wave output to 0.

Table 7-9 lists the square-wave output range, and Figure 7-11 shows the timing of square-wave output.

Caution When the setting of the count clock using TMC02 and the setting of the TM02 to operation-enable using an 8-bit memory manipulation instruction are performed at the same time, an error of one clock or more may occur in the first cycle after the timer is started. Because of this, when the 8-bit timer operates as a square-wave output, be sure to make the settings in the order described above.

Table 7-9. Square-Wave Output Range of 8-Bit Timer 02

TCL021	TCL020	Minimum Pulse Width	Maximum Pulse Width	Resolution
0	0	$2^3/f_X$ (1.6 μs)	$2^{11}/f_X$ (409.6 μs)	$2^3/f_X$ (1.6 μs)
0	1	$2^7/f_X$ (25.6 μs)	$2^{15}/f_X$ (6.55 ms)	$2^7/f_X$ (25.6 μs)
1	0	$1/f_{XT}$ (30.5 μs)	$2^8/f_{XT}$ (7.81 ms)	$1/f_{XT}$ (30.5 μs)
1	1	Setting prohibited		

Remarks 1. f_X: Main system clock oscillation frequency
2. f_{XT}: Subsystem clock oscillation frequency
3. The parenthesized values apply to operation at f_X = 5.0 MHz or f_{XT} = 32.768 kHz.

9.4 Operation of Watchdog Timer

9.4.1 Operation as watchdog timer

The watchdog timer detects an inadvertent program loop when bit 4 (WDTM4) of the watchdog timer mode register (WDTM) is set to 1.

The count clock (program loop detection time interval) of the watchdog timer can be selected by bits 0 to 2 (TCL20 to TCL22) of timer clock selection register 2 (TCL2). By setting bit 7 (RUN) of WDTM to 1, the watchdog timer is started. Set RUN to 1 within the set program loop detection time interval after the watchdog timer has been started. By setting RUN to 1, the watchdog timer can be cleared and start counting. If RUN is not set to 1, and the program loop detection time is exceeded, the system is reset or a non-maskable interrupt is generated by the value of bit 3 (WDTM3) of WDTM.

The watchdog timer continues operation in the HALT mode, but stops in the STOP mode. Therefore, set RUN to 1 before entering the STOP mode to clear the watchdog timer, and then execute the STOP instruction.

Cautions 1. The actual program loop detection time may be up to 0.8% shorter than the set time.

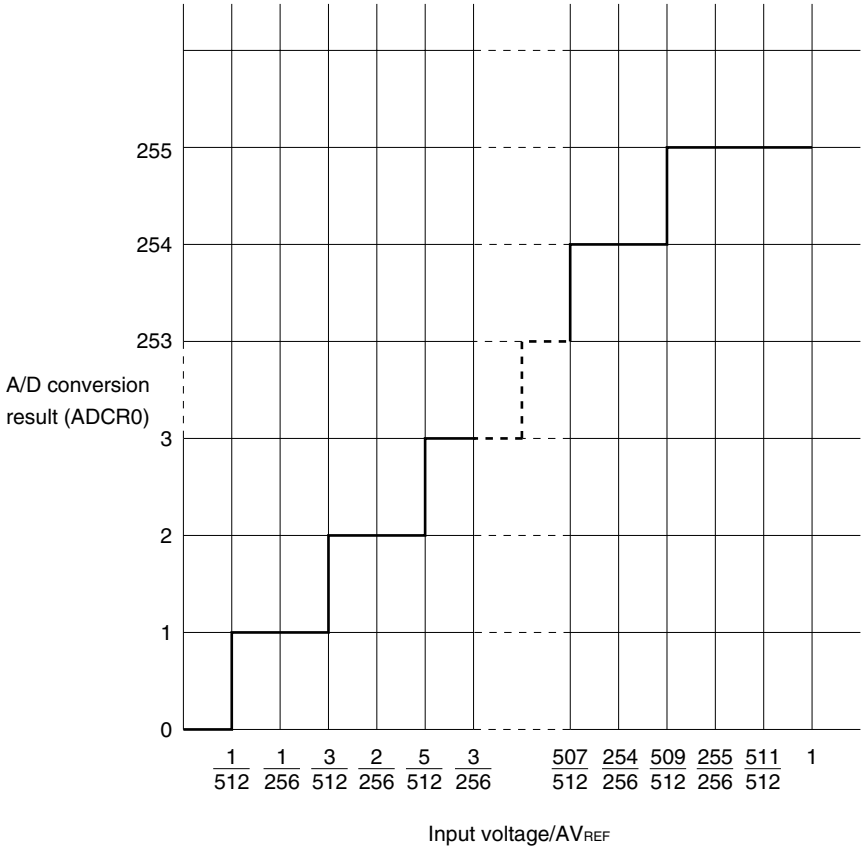
2. When the subsystem clock is selected as the CPU clock, the watchdog timer stops counting.

Table 9-4. Program Loop Detection Time of Watchdog Timer

TCL22	TCL21	TCL20	Program Loop Detection Time	Operation at f_X = 5.0 MHz
0	0	0	$2^{11} \times 1/f_X$	410 μs
0	1	0	$2^{13} \times 1/f_X$	1.64 ms
1	0	0	$2^{15} \times 1/f_X$	6.55 ms
1	1	0	$2^{17} \times 1/f_X$	26.2 ms

f_X: Main system clock oscillation frequency

Figure 10-5. Relationship Between Analog Input Voltage and A/D Conversion Result



(b) Asynchronous serial interface mode register 00 (ASIM00)

ASIM00 is set using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets ASIM00 to 00H.

Symbol	<7>	<6>	5	4	3	2	1	0	Address	After reset	R/W
ASIM00	TXE00	RXE00	PS001	PS000	CL00	SL00	0	0	FF70H	00H	R/W

TXE00	Transmit operation control
0	Transmit operation stopped
1	Transmit operation enabled

RXE00	Receive operation control
0	Receive operation stopped
1	Receive operation enabled

Caution Bits 0 and 1 must be fixed to 0.

(c) Asynchronous serial interface status register 00 (ASIS00)

ASIS00 is read using a 1-bit or 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets ASIS00 to 00H.

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
ASIS00	0	0	0	0	0	PE00	FE00	OVE00	FF71H	00H	R

PE00	Parity error flag
0	Parity error did not occur
1	Parity error occurred (when the transmit parity and receive parity did not match)

FE00	Framing error flag
0	Framing error did not occur
1	Framing error occurred (when stop bit was not detected)Note 1

OVE00	Overrun error flag
0	Overrun error did not occur
1	Overrun error occurredNote 2 (when the next receive operation was completed before the data was read from receive buffer register 00)

Notes 1. Even when the stop bit length is set to 2 bits by setting bit 2 (SL00) of asynchronous serial interface mode register 00 (ASIM00), only one stop bit will be detected during reception.

2. Be sure to read receive buffer register 00 (RXB00) when an overrun error occurs. If not, every time the data is received an overrun error occurs.

(b) Parity types and operation

The parity bit is used to detect a bit error in the communication data. Normally, the same kind of parity bit is used on the transmitting side and the receiving side. With even parity and odd parity, a “1” bit (odd number) error can be detected. With 0 parity and no parity, an error cannot be detected.

(i) Even parity

- **At transmission**

  The transmission operation is controlled so that the number of bits with a value of 1 in the transmit data including the parity bit may be even. The parity bit value should be as follows.

  The number of bits with a value of 1 is an odd number in transmit data: 1
  The number of bits with a value of 1 is an even number in transmit data: 0

- **At reception**

  The number of bits with a value of 1 in the receive data including the parity bit is counted, and if the number is odd, a parity error occurs.

(ii) Odd parity

- **At transmission**

  Conversely to even parity, the transmission operation is controlled so that the number of bits with a value of 1 in the transmit data including the parity bit may be odd. The parity bit value should be as follows.

  The number of bits with a value of 1 is an odd number in transmit data: 0
  The number of bits with a value of 1 is an even number in transmit data: 1

- **At reception**

  The number of bits with a value of 1 in the receive data including the parity bit is counted, and if the number is even, a parity error occurs.

(iii) 0 Parity

When transmitting, the parity bit is set to 0 irrespective of the transmit data.

At reception, a parity bit check is not performed. Therefore, a parity error does not occur, irrespective of whether the parity bit is set to 0 or 1.

(iv) No parity

A parity bit is not added to the transmit data. At reception, data is received assuming that there is no parity bit. Since there is no parity bit, a parity error does not occur.

(3) Output waveforms of common and segment signals

The voltages listed in Table 14-5 are output as common and segment signals.

When both common and segment signals are at the select voltage, a display on-voltage of $\pm V_{LCD}$ is obtained.

The other combinations of the signals correspond to the display off-voltage.

Table 14-5. LCD Drive Voltage

(a) Static display mode

Segment Signal / Common Signal	Select Signal Level	Deselect Signal Level
	V_{SS0}/V_{LC0}	V_{LC0}/V_{SS0}
V_{LC0}/V_{SS0}	$-V_{LCD}/+V_{LCD}$	0 V/0 V

(b) 1/2 bias method

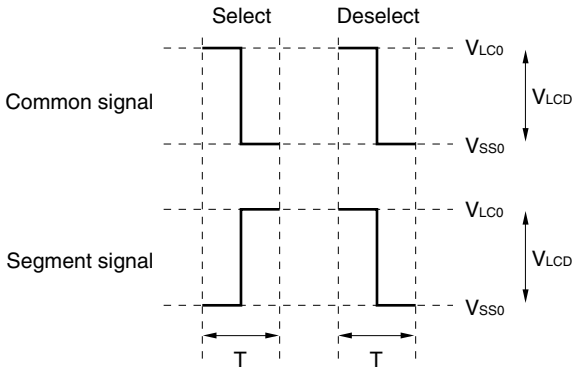
Segment Signal / Common Signal		Select Signal Level	Deselect Signal Level
		V_{SS0}/V_{LC0}	V_{LC0}/V_{SS0}
Select signal level	V_{LC0}/V_{SS0}	$-V_{LCD}/+V_{LCD}$	0 V/0 V
Deselect signal level	$V_{LC1} = V_{LC2}$	$-\frac{1}{2}V_{LCD}/+\frac{1}{2}V_{LCD}$	$+\frac{1}{2}V_{LCD}/-\frac{1}{2}V_{LCD}$

(c) 1/3 bias method

Segment Signal / Common Signal		Select Signal Level	Deselect Signal Level
		V_{SS0}/V_{LC0}	V_{LC1}/V_{LC2}
Select signal level	V_{LC0}/V_{SS0}	$-V_{LCD}/+V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$
Deselect signal level	V_{LC2}/V_{LC1}	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$	$-\frac{1}{3}V_{LCD}/+\frac{1}{3}V_{LCD}$

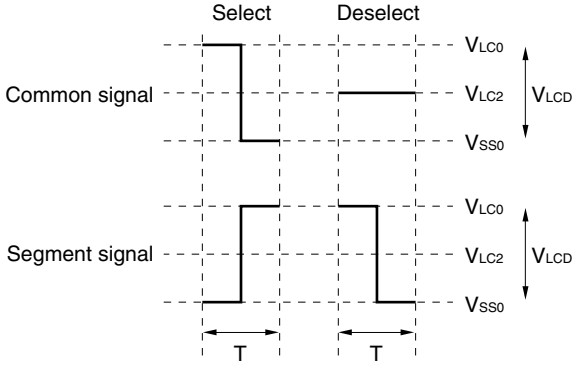
Figure 14-7. Voltages and Phases of Common and Segment Signals

(a) Static display mode



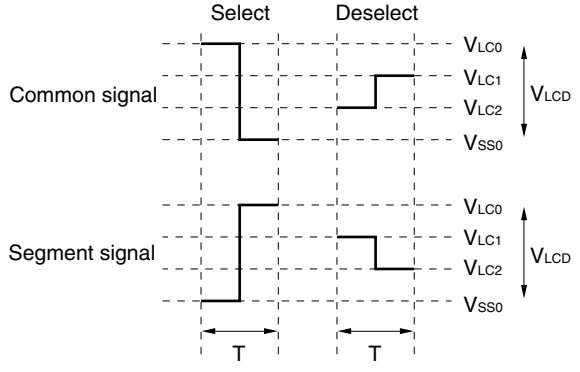
T: One LCD clock period

(b) 1/2 bias method



T: One LCD clock period

(c) 1/3 bias method



T: One LCD clock period

15.3 Registers Controlling Interrupt Function

The following five registers are used to control the interrupt functions.

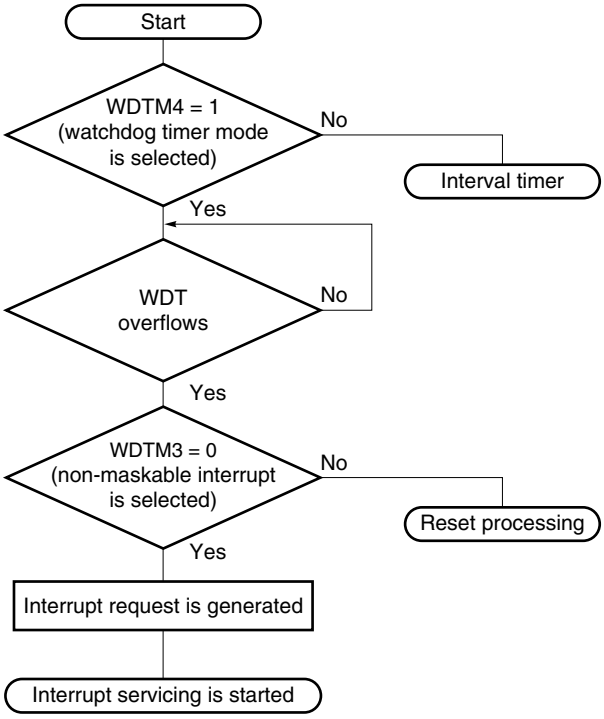
- Interrupt request flag registers 0, 1 (IF0 and IF1)
- Interrupt mask flag registers 0, 1 (MK0 and MK1)
- External interrupt mode registers 0, 1 (INTM0 and INTM1)
- Program status word (PSW)
- Key return mode register 00 (KRM00)

Table 15-2 lists the interrupt request flag and interrupt mask flag names corresponding to interrupt requests.

Table 15-2. Flags Corresponding to Interrupt Request Signal Name

Interrupt Request Signal Name	Interrupt Request Flag	Interrupt Mask Flag
INTWDT	TMIF4	TMMK4
INTP0	PIF0	PMK0
INTP1	PIF1	PMK1
INTP2	PIF2	PMK2
INTP3	PIF3	PMK3
INTSR00/INTCSI00	SRIF00	SRMK00
INTST00	STIF00	STMK00
INTWT	WTIF	WTMK
INTWTI	WTIIF	WTIMK
INTTM00	TMIF00	TMMK00
INTTM01	TMIF01	TMMK01
INTTM02	TMIF02	TMMK02
INTTM50	TMIF50	TMMK50
INTKR00	KRIF00	KRMK00
INTAD0	ADIF0	ADMK0
INTCMP0	CMPIF0	CMPMK0

Figure 15-9. Flowchart of Non-Maskable Interrupt Request Acknowledgment



WDTM: Watchdog timer mode register
WDT: Watchdog timer

Figure 15-10. Timing of Non-Maskable Interrupt Request Acknowledgment

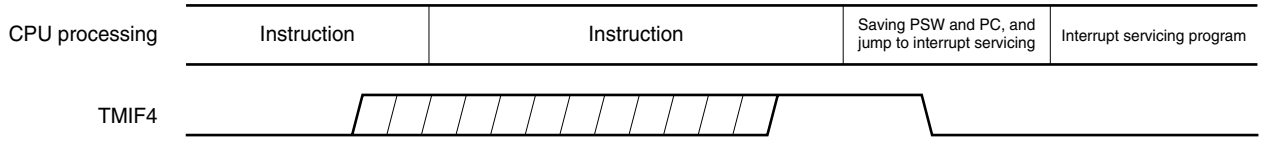
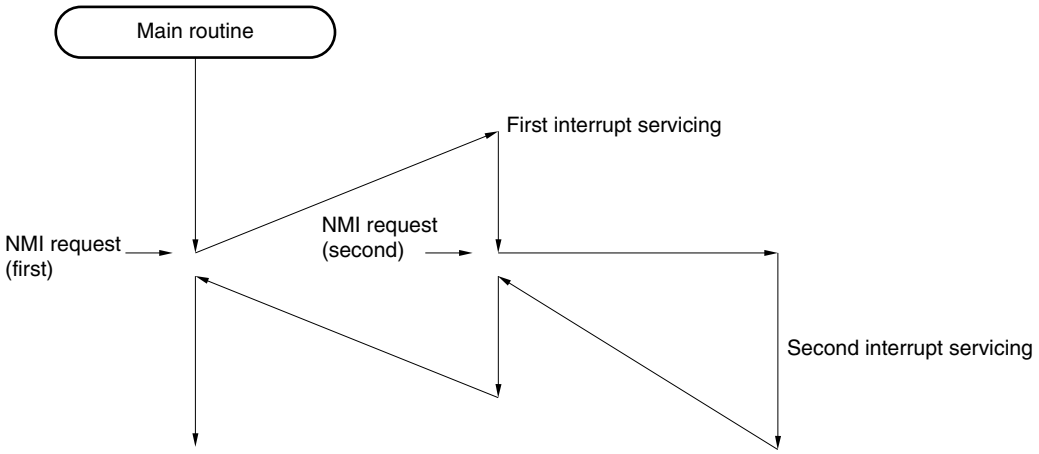


Figure 15-11. Non-Maskable Interrupt Request Acknowledgment



★ 18.1 Flash Memory Characteristics

Flash memory programming is performed by connecting a dedicated flash programmer (Flashpro III (part no. FL-PR3, PG-FP3)/Flashpro IV (part no. FL-PR4, PG-FP4)) to the target system with the μPD78F9418A mounted on the target system (on-board). A flash memory program adapter (FA adapter), which is a target board used exclusively for programming, is also provided.

Remark FL-PR3, FL-PR4, and the program adapter are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL +81-45-475-4191).

Programming using flash memory has the following advantages.

- Software can be modified after the microcontroller is solder-mounted on the target system.
- Distinguishing software facilities small-quantity, varied model production
- Easy data adjustment when starting mass production

18.1.1 Programming environment

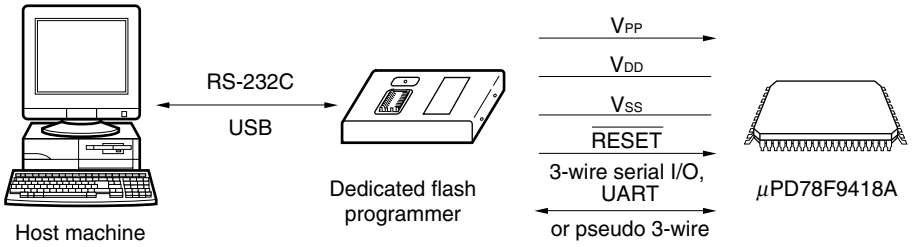
The following shows the environment required for μPD78F9418A flash memory programming.

When Flashpro III (part no. FL-PR3, PG-FP3) or Flashpro IV (part no. FL-PR4, PG-FP4) is used as a dedicated flash programmer, a host machine is required to control the dedicated flash programmer. Communication between the host machine and flash programmer is performed via RS-232C/USB (Rev. 1.1).

For details, refer to the manuals for Flashpro III/Flashpro IV.

Remark USB is supported by Flashpro IV only.

Figure 18-1. Environment for Writing Program to Flash Memory



Mnemonic	Operands	Bytes	Clocks	Operation	Flag
					Z AC CY
CALL	!addr16	3	6	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, $PC \leftarrow$ addr16, $SP \leftarrow SP-2$	
CALLT	[addr5]	1	8	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_H \leftarrow$ (00000000, addr5 + 1), $PC_L \leftarrow$ (00000000, addr5), $SP \leftarrow SP-2$	
RET		1	6	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $SP \leftarrow SP+2$	
RETI		1	8	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $PSW \leftarrow (SP+2)$, $SP \leftarrow SP+3$, NMIS $\leftarrow 0$	R R R
PUSH	PSW	1	2	$(SP-1) \leftarrow PSW$, $SP \leftarrow SP-1$	
	rp	1	4	$(SP-1) \leftarrow rp_H$, $(SP-2) \leftarrow rp_L$, $SP \leftarrow SP-2$	
POP	PSW	1	4	$PSW \leftarrow (SP)$, $SP \leftarrow SP+1$	R R R
	rp	1	6	$rp_H \leftarrow (SP+1)$, $rp_L \leftarrow (SP)$, $SP \leftarrow SP+2$	
MOVW	SP, AX	2	8	$SP \leftarrow AX$	
	AX, SP	2	6	$AX \leftarrow SP$	
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	$PC \leftarrow PC+2+$ jdisp8	
	AX	1	6	$PC_H \leftarrow A$, $PC_L \leftarrow X$	
BC	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if CY = 1	
BNC	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if CY = 0	
BZ	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if Z = 1	
BNZ	$saddr16	2	6	$PC \leftarrow PC+2+$ jdisp8 if Z = 0	
BT	saddr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if (saddr.bit) = 1	
	sfr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if sfr.bit = 1	
	A.bit, $addr16	3	8	$PC \leftarrow PC+3+$ jdisp8 if A.bit = 1	
	PSW.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if PSW.bit = 1	
BF	saddr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if (saddr.bit) = 0	
	sfr.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if sfr.bit = 0	
	A.bit, $addr16	3	8	$PC \leftarrow PC+3+$ jdisp8 if A.bit = 0	
	PSW.bit, $addr16	4	10	$PC \leftarrow PC+4+$ jdisp8 if PSW.bit = 0	
DBNZ	B, $addr16	2	6	$B \leftarrow B-1$, then $PC \leftarrow PC+2+$ jdisp8 if $B \neq 0$	
	C, $addr16	2	6	$C \leftarrow C-1$, then $PC \leftarrow PC+2+$ jdisp8 if $C \neq 0$	
	saddr, $addr16	3	8	$(saddr) \leftarrow (saddr)-1$, then $PC \leftarrow PC+3+$ jdisp8 if $(saddr) \neq 0$	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable interrupt)	
DI		3	6	IE ← 0 (Disable interrupt)	
HALT		1	2	Set HALT mode	
STOP		1	2	Set STOP mode	

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R_1	V_{IN} = 0 V, pins other than P50 to P53		50	100	200	kΩ
Mask option pull-up resistor[Note 1]	R_2	V_{IN} = 0 V, P50 to P53		15	30	60	kΩ
Supply current (mask ROM version)	I_{DD1}[Note 2]	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 5]		2.0	4.0	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.6	1.2	mA
			V_{DD} = 2.0 V ±10%[Note 6]		0.3	0.6	mA
	I_{DD2}[Note 2]	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 5]		1.1	2.2	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.4	0.8	mA
			V_{DD} = 2.0 V ±10%[Note 6]		0.2	0.4	mA
	I_{DD3}[Note 2]	32.768 kHz crystal oscillation operating mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		30	90	μA
			V_{DD} = 3.0 V ±10%		9	50	μA
			V_{DD} = 2.0 V ±10%		4	25	μA
	I_{DD4}[Note 2]	32.768 kHz crystal oscillation HALT mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	25	μA
			V_{DD} = 2.0 V ±10%		2.5	12.5	μA
	I_{DD5}[Note 2]	32.768 kHz crystal oscillation STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			T_A = 25°C		0.05	3.0	μA
			V_{DD} = 2.0 V ±10%		0.05	3.0	μA
	I_{DD6}[Note 3]	5.0 MHz crystal oscillation A/D operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%		2.6	6.0	mA
			V_{DD} = 3.0 V ±10%		1.2	3.6	mA
			V_{DD} = 2.0 V ±10%		0.9	2.7	mA

Notes 1. Mask ROM version only

2. The current flowing to AV_{REF} (A/D operation ON (ADCS0 = 1)), AV_{DD} current, and the port current (including the current flowing through the on-chip pull-up resistors) is not included.

3. The current flowing to AV_{REF} (A/D operation ON (ADCS0 = 1)) and the port current (including the current flowing through the on-chip pull-up resistors) is not included. For the current flowing to AV_{REF}, refer to the parameter of "Resistance between AV_{REF} and AV_{SS}" in the **8-Bit A/D Converter Characteristics** and **10-Bit A/D Converter Characteristics**.

4. When the main system clock is stopped

5. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

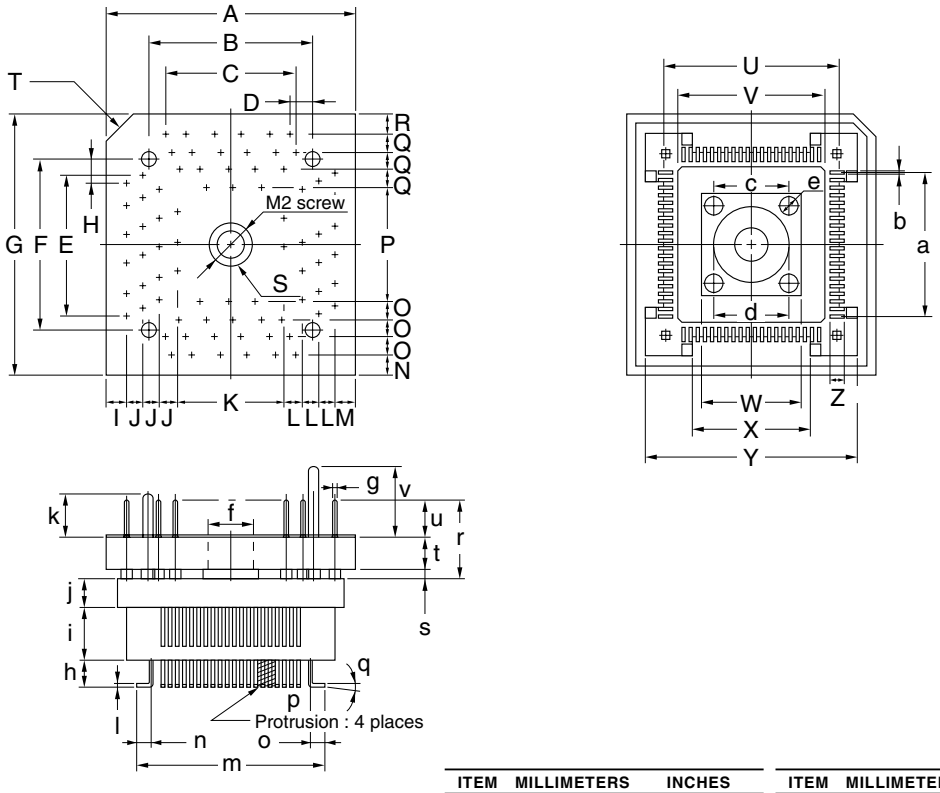
6. Low-speed mode operation (when PCC is set to 02H)

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

A.7.2 Package drawing of conversion adapter (TGK-080SDW)

Figure A-4. Package Drawing of TGK-080SDW (for Reference)

TGK-080SDW (TQPACK080SD + TQSOCKET080SDW) Package dimension (unit: mm)



ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	11.77	0.463
C	0.5x19=9.5	0.020x0.748=0.374
D	0.5	0.020
E	0.5x19=9.5	0.020x0.748=0.374
F	11.77	0.463
G	18.0	0.709
H	0.5	0.020
I	1.58	0.062
J	1.2	0.047
K	7.64	0.301
L	1.2	0.047
M	1.58	0.062
N	1.58	0.062
O	1.2	0.047
P	7.64	0.301
Q	1.2	0.047
R	1.58	0.062
S	ϕ3.55	ϕ0.140
T	C 2.0	C 0.079
U	12.31	0.485
V	10.17	0.400
W	6.8	0.268
X	8.24	0.324
Y	14.8	0.583
Z	1.4±0.2	0.055±0.008

ITEM	MILLIMETERS	INCHES
a	0.5x19=9.5±0.10	0.020x0.748=0.374±0.004
b	0.25	0.010
c	ϕ5.3	ϕ0.209
d	ϕ5.3	ϕ0.209
e	ϕ1.3	ϕ0.051
f	ϕ3.55	ϕ0.140
g	ϕ0.3	ϕ0.012
h	1.85±0.2	0.073±0.008
i	3.5	0.138
j	2.0	0.079
k	3.0	0.118
l	0.25	0.010
m	14.0	0.551
n	1.4±0.2	0.055±0.008
o	1.4±0.2	0.055±0.008
p	h=1.8 ϕ1.3	h=0.071 ϕ0.051
q	0~5°	0.000~0.197°
r	5.9	0.232
s	0.8	0.031
t	2.4	0.094
u	2.7	0.106
v	3.9	0.154

TGK-080SDW-G1E

note: Product by TOKYO ELETECH CORPORATION.