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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349czuajdb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.



Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV _{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV _{DD} = 1.8 V
TSEC/10/100 signals	40	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, JTAG, USB	40	OV _{DD} = 3.3 V
GPIO signals	40	OV _{DD} = 3.3 V, LV _{DD} = 2.5/3.3 V

Table 3. Output Drive Capability

2.2 **Power Sequencing**

This section details the power sequencing considerations for the MPC8349EA.

2.2.1 Power-Up Sequencing

MPC8349EA does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

DDR and DDR2 SDRAM

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	_	mA	_

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to equal 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.

 V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

Table 13 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	—
Output leakage current	I _{OZ}	-9.9	-9.9	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	—	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	—	mA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

DDR and DDR2 SDRAM

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) \pm 5%.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
- 4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual for the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).



Figure 6. Timing Diagram for t_{DDKHMH}

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	_	4.0	ns
RX_CLK clock fall time (80%-20%)	t _{MRXF}	1.0	_	4.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

Figure 12 provides the AC test load for TSEC.



Figure 12. TSEC AC Test Load

Figure 13 shows the MII receive AC timing diagram.



Figure 13. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

Table 31. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
Data to clock output skew (at transmitter)	t _{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t _{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t _{RGTH} /t _{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t _{RGTH} /t _{RGT}	40	50	60	%
Rise time (20%–80%)	t _{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t _{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).

2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.

5. Duty cycle reference is $LV_{DD}/2$.

Local Bus



Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)

JTAG

Figure 30 provides the boundary-scan timing diagram.











Table 45. PCI AC Timing Specifications at 66 MHz ¹	(continued)
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Parameter	Symbol ²	Min	Мах	Unit	Notes
PORESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	6

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.}
- 3. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.
- 6. The setup and hold time is with respect to the rising edge of PORESET.

Table 46 provides the PCI AC timing specifications at 33 MHz.

Table 46. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	^t PCKHOV	—	11	ns	2
Output hold from clock	t _{PCKHOX}	2		ns	2
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	-	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	-	ns	2, 4
REQ64 to PORESET setup time	t _{PCRVRH}	5	_	clocks	5
PORESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	5

Notes:

2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.

3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4. Input timings are measured at the pin.

5. The setup and hold time is with respect to the rising edge of PORESET.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

Figure 34 provides the AC test load for PCI.



Figure 34. PCI AC Test Load

Figure 35 shows the PCI input AC timing diagram.



Figure 35. PCI Input AC Timing Diagram

Figure 36 shows the PCI output AC timing diagram.



14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the MPC8349EA timer pins, including TIN, TOUT, TGATE, and RTC_CLK.

Table 47. Timer DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	_	_	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V

Table 47. Timer DC Electrical C	Characteristics (continued)
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Parameter	Symbol	Condition	Min	Мах	Unit
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8349EA GPIO.

Table 49. GPIO DC Electrical Characteristics

PArameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	_	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

Table 50	. GPIO	Input AC	Timing	Specifications ¹
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Parameter	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the external interrupt pins.

Table 51. IPIC DC	Electrical Characteristics ¹
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Parameter	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	—	—	±5	μA	—
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	2

Notes:

1. This table applies for pins \overline{IRQ} [0:7], \overline{IRQ} _OUT, and \overline{MCP} _OUT.

2. IRQ_OUT and MCP_OUT are open-drain pins; thus VOH is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 52 provides the IPIC input and output AC timing specifications.

Table 52. IPIC Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.

 IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

Package and Pin Listings

18.2 Mechanical Dimensions for the MPC8349EA TBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8349EA, 672-TBGA package.



Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8349EA TBGA

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV _{DD}	_
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV _{DD2}	_
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV _{DD}	_
	DUART			
UART_SOUT[1:2]/MSRCID[0:1]/ LSRCID[0:1]	AK27, AN29	0	OV _{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/ LSRCID[2:3]	AL28, AM29	I/O	OV _{DD}	—
UART_CTS[1]/MSRCID4/LSRCID4	AP30	I/O	OV _{DD}	—
UART_CTS[2]/MDVAL/ LDVAL	AN30	I/O	OV _{DD}	—
UART_RTS[1:2]	AP31, AM30	0	OV _{DD}	—
	I ² C interface			
IIC1_SDA	AK29	I/O	OV _{DD}	2
IIC1_SCL	AP32	I/O	OV _{DD}	2
IIC2_SDA	AN31	I/O	OV _{DD}	2
IIC2_SCL	AM31	I/O	OV _{DD}	2
	SPI			
SPIMOSI/LCS[6]	AN32	I/O	OV _{DD}	—
SPIMISO/LCS[7]	AP33	I/O	OV _{DD}	—
SPICLK	AK30	I/O	OV _{DD}	—
SPISEL	AL31	I	OV _{DD}	—
	Clocks			
PCI_CLK_OUT[0:2]	AN9, AP9, AM10,	0	OV _{DD}	—
PCI_CLK_OUT[3]/LCS[6]	AN10	0	OV _{DD}	—
PCI_CLK_OUT[4]/LCS[7]	AJ11	0	OV _{DD}	—
PCI_CLK_OUT[5:7]	AP10, AL11, AM11	0	OV _{DD}	—
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV _{DD}	—
PCI_SYNC_OUT	AP11	0	OV _{DD}	3
RTC/PIT_CLOCK	AM32	I	OV _{DD}	—
CLKIN	AM9	I	OV _{DD}	—
	JTAG			
ТСК	E20	I	OV _{DD}	
TDI	F20	I	OV _{DD}	4

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	_		_
GV _{DD}	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}	_
LV _{DD1}	C9, D11	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV _{DD1}	_
LV _{DD2}	C6, D9	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD2}	_
V _{DD}	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V _{DD}	_
OV _{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	_
MVREF1	МЗ	I	DDR reference voltage	_

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Clocking

Table 57 provides the operating frequencies for the MPC8349EA TBGA under recommended operating conditions (see Table 2).

Characteristic ¹	400 MHz	533 MHz	667 MHz	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266	100–333	100–333	MHz
DDR1 memory bus frequency (MCK) ²	100–133	100–133	100–166.67	MHz
DDR2 memory bus frequency (MCK) ³	100–133	100–133	100–200	MHz
Local bus frequency (LCLK <i>n</i>) ⁴	16.67–133	16.67–133	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66	25–66	25–66	MHz
Security core maximum internal operating frequency	133	133	166	MHz
USB_DR, USB_MPH maximum internal operating frequency	133	133	166	MHz

Table 57. Operating Frequencies for TBGA

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM] and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the security core and USB modules does not exceed the respective values listed in this table.

² The DDR data rate is 2x the DDR memory bus frequency.

³ The DDR data rate is 2x the DDR memory bus frequency.

⁴ The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 22.1, "Part Numbers Fully Addressed by This Document," for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6

Table 58. System PLL Multiplication Factors

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
Low	0110	6:1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		1
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2:1				133
High	0011	3:1			100	200
High	0100	4 : 1			133	266
High	0101	5:1			166	333
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				

Table 59. CSB Frequency Options for Host Mode (continued)

¹ CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 60. CSB Frequency Options for Agent Mode

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333

RCWL[COREPLL]						
0–1	2–5	6	- core_cik : csb_cik Ratio	VCO Divider		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)		
00	0001	0	1:1	2		
01	0001	0	1:1	4		
10	0001	0	1:1	8		
11	0001	0	1:1	8		
00	0001	1	1.5:1	2		
01	0001	1	1.5:1	4		
10	0001	1	1.5:1	8		
11	0001	1	1.5:1	8		
00	0010	0	2:1	2		
01	0010	0	2:1	4		
10	0010	0	2:1	8		
11	0010	0	2:1	8		
00	0010	1	2.5:1	2		
01	0010	1	2.5:1	4		
10	0010	1	2.5:1	8		
11	0010	1	2.5:1	8		
00	0011	0	3:1	2		
01	0011	0	3:1	4		
10	0011	0	3:1	8		
11	0011	0	3:1	8		

Table 61. e300 Core PLL Configuration

¹ Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

Table 63. Package Thermal Characteristics for TBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_J = junction temperature (°C)

 T_A = ambient temperature for the package (°C)

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

Thermal

Heat sink vendors include the following list:	
Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers [™] P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102
Interface material vendors include the following:	
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997	800-248-2481
Internet: www.dowcorning.com Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674

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