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#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349eczuajdb

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Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.



Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

## 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV <sub>DD</sub> = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV <sub>DD</sub> = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV <sub>DD</sub> = 1.8 V
TSEC/10/100 signals	40	LV <sub>DD</sub> = 2.5/3.3 V
DUART, system control, I <sup>2</sup> C, JTAG, USB	40	OV <sub>DD</sub> = 3.3 V
GPIO signals	40	OV <sub>DD</sub> = 3.3 V, LV <sub>DD</sub> = 2.5/3.3 V

Table 3. Output Drive Capability

# 2.2 **Power Sequencing**

This section details the power sequencing considerations for the MPC8349EA.

## 2.2.1 Power-Up Sequencing

MPC8349EA does not require the core supply voltage ( $V_{DD}$  and  $AV_{DD}$ ) and I/O supply voltages ( $GV_{DD}$ ,  $LV_{DD}$ , and  $OV_{DD}$ ) to be applied in any particular order. During the power ramp up, before the power

- <sup>2</sup> Typical power is based on a voltage of  $V_{DD}$  = 1.2 V, a junction temperature of  $T_J$  = 105°C, and a Dhrystone benchmark application.
- <sup>3</sup> Thermal solutions may need to design to a value higher than typical power based on the end application, T<sub>A</sub> target, and I/O power.
- <sup>4</sup> Maximum power is based on a voltage of  $V_{DD}$  = 1.2 V, worst case process, a junction temperature of  $T_J$  = 105°C, and an artificial smoke test.
- <sup>5</sup> Typical power is based on a voltage of  $V_{DD}$  = 1.3 V, a junction temperature of  $T_J$  = 105°C, and a Dhrystone benchmark application.
- <sup>6</sup> Maximum power is based on a voltage of  $V_{DD}$  = 1.3 V, worst case process, a junction temperature of  $T_J$  = 105°C, and an artificial smoke test.

### Table 5 shows the estimated typical I/O power dissipation for MPC8349EA.

Interface	Parameter	GV <sub>DD</sub> (1.8 V)	GV <sub>DD</sub> (2.5 V)	OV <sub>DD</sub> (3.3 V)	LV <sub>DD</sub> (3.3 V)	LV <sub>DD</sub> (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 32 bits	0.31	0.42				W	—
65% utilization 2.5 V	200 MHz, 64 bits	0.42	0.55				W	—
Rs = 20 Ω Bt = 50 Ω	266 MHz, 32 bits	0.35	0.5				W	—
2 pair of clocks	266 MHz, 64 bits	0.47	0.66				W	—
	300 MHz, 32 bits	0.37	0.54	_	_	_	W	—
	300 MHz, 64 bits	0.50	0.7	_	_	_	W	—
	333 MHz, 32 bits	0.39	0.58	_	_	_	W	—
	333 MHz, 64 bits	0.53	0.76	_	_	_	W	—
	400 MHz, 32 bits	0.44						—
	400 MHz, 64 bits	0.59	_	_		_	_	—
PCI I/O	33 MHz, 64 bits	_	_	0.08	_	_	W	—
10ad = 30 pF	66 MHz, 64 bits	_	_	0.14	_	_	W	—
	33 MHz, 32 bits	_	_	0.04	_	_	W	Multiply by 2 if using
	66 MHz, 32 bits	_	_	0.07	_	_	W	2 ports.
Local bus I/O	133 MHz, 32 bits	_	_	0.27	_	_	W	—
10ad = 25 pF	83 MHz, 32 bits	_	_	0.17	_	_	W	—
	66 MHz, 32 bits	_	_	0.14	_	_	W	—
	50 MHz, 32 bits	_	_	0.11	_	_	W	—
TSEC I/O	MII	_	_	_	0.01	_	W	Multiply by number of
load = 25 pF	GMII or TBI	_	_		0.06	_	W	interfaces used.
	RGMII or RTBI	_	_			0.04	W	
USB	12 MHz	_	_	0.01	_	_	W	Multiply by 2 if using
	480 MHz	_	_	0.2	_	_	W	2 ports.
Other I/O	—			0.01			W	—

## Table 5. MPC8349EA Typical I/O Power Dissipation

#### DDR and DDR2 SDRAM

## Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

### Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with  $GV_{DD}$  of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t <sub>CISKEW</sub>			ps	1, 2
400 MHz		-600	600		3
333 MHz		-750	750		—
266 MHz		-750	750		—
200 MHz		-750	750		—

Notes:

1. t<sub>CISKEW</sub> represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t<sub>DISKEW</sub>. This can be determined by the equation: t<sub>DISKEW</sub> = ± (T/4 – abs (t<sub>CISKEW</sub>)); where T is the clock period and abs (t<sub>CISKEW</sub>) is the absolute value of t<sub>CISKEW</sub>.
- 3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t<sub>DISKEW</sub> timing parameter.



Figure 5. DDR Input Timing Diagram

# 6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

### Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with  $\text{GV}_{\text{DD}}$  of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
ADDR/CMD/MODT output setup with respect to MCK	t <sub>DDKHAS</sub>			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
ADDR/CMD/MODT output hold with respect to MCK	t <sub>DDKHAX</sub>			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output setup with respect to MCK	t <sub>DDKHCS</sub>			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output hold with respect to MCK	t <sub>DDKHCX</sub>			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	_		
MCK to MDQS Skew	t <sub>DDKHMH</sub>	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t <sub>DDKHDS,</sub> t <sub>DDKLDS</sub>			ps	5
400 MHz		700	—		
333 MHz		775	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	t <sub>DDKHDX,</sub> t <sub>DDKLDX</sub>			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t <sub>DDKHMP</sub>	$-0.5\times t_{\text{MCK}}-0.6$	$-0.5\times t_{MCK}+0.6$	ns	6

# 8.1.1 **TSEC DC Electrical Characteristics**

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV <sub>DD</sub> <sup>2</sup>	—		2.97	3.63	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA	$LV_{DD} = Min$	2.40	LV <sub>DD</sub> + 0.3	V
Output low voltage	V <sub>OL</sub>	$I_{OL} = 4.0 \text{ mA}$ $LV_{DD} = Min$		GND	0.50	V
Input high voltage	V <sub>IH</sub>	—	_	2.0	LV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	_	-0.3	0.90	V
Input high current	I <sub>IH</sub>	$V_{IN}^{1} = LV_{DD}$		_	40	μA
Input low current	Ι <sub>ΙL</sub>	V <sub>IN</sub> <sup>1</sup> =	GND	-600	_	μÂ

## Table 23. GMII/TBI and MII DC Electrical Characteristics

Notes:

1. The symbol  $V_{IN}$ , in this case, represents the LV<sub>IN</sub> symbol referenced in Table 1 and Table 2.

2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the OV<sub>DD</sub> supply.

## Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV <sub>DD</sub>	—		2.37	2.63	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	$LV_{DD} = Min$	2.00	LV <sub>DD</sub> + 0.3	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.0 mA LV <sub>DD</sub> = Min		GND – 0.3	0.40	V
Input high voltage	V <sub>IH</sub>	—	— LV <sub>DD</sub> = Min		LV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	$LV_{DD} = Min$	-0.3	0.70	V
Input high current	I <sub>IH</sub>	$V_{IN}^{1} = LV_{DD}$		—	10	μA
Input low current	۱ <sub>IL</sub>	V <sub>IN</sub> <sup>1</sup> =	V <sub>IN</sub> <sup>1</sup> = GND		—	μA

#### Note:

1. The symbol  $V_{IN}$ , in this case, represents the LV<sub>IN</sub> symbol referenced in Table 1 and Table 2.

# 8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

# 8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### Table 26. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V  $\pm$  10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
RX_CLK clock rise (20%–80%)	t <sub>GRXR</sub>		_	1.0	ns
RX_CLK clock fall time (80%-20%)	t <sub>GRXF</sub>	_		1.0	ns

### Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>GRDVKH</sub> symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>RX</sub> clock reference (K) going to the high state (H) or setup time. Also, t<sub>GRDXKL</sub> symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>GRX</sub> clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t<sub>GRX</sub> represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

Figure 10 shows the GMII receive AC timing diagram.



## 8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

## 8.2.2.1 MII Transmit AC Timing Specifications

Table 27 provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Tim	ing Specifications
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At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t <sub>MTX</sub>	—	400	—	ns
TX_CLK clock period 100 Mbps	t <sub>MTX</sub>	—	40	—	ns
TX_CLK duty cycle	t <sub>MTXH</sub> /t <sub>MTX</sub>	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t <sub>MTKHDX</sub>	1	5	15	ns

### Table 30. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V  $\pm$  10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t <sub>TRDVKH</sub> 2	2.5	—	_	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t <sub>тRDXKH</sub> <sup>2</sup>	1.5	—	_	ns
RX_CLK clock rise time (20%–80%)	t <sub>TRXR</sub>	0.7	—	2.4	ns
RX_CLK clock fall time (80%-20%)	t <sub>TRXF</sub>	0.7	_	2.4	ns

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TRDVKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>TRDXKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t<sub>TRX</sub> represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
</sub>

2. Setup and hold time of even numbered RCG are measured from the riding edge of PMA\_RX\_CLK1. Setup and hold times of odd-numbered RCG are measured from the riding edge of PMA\_RX\_CLK0.

## Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram

# 10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8349EA.

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	7.5	_	ns	2
Input setup to local bus clock (except LUPWAIT)	t <sub>LBIVKH1</sub>	1.5	_	ns	3, 4
LUPWAIT input setup to local bus clock	t <sub>LBIVKH2</sub>	2.2	_	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t <sub>LBIXKH1</sub>	1.0	_	ns	3, 4
LUPWAIT Input hold from local bus clock	t <sub>LBIXKH2</sub>	1.0	_	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t <sub>LBOTOT1</sub>	1.5	_	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t <sub>LBOTOT2</sub>	3	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t <sub>LBOTOT3</sub>	2.5	_	ns	7
Local bus clock to LALE rise	t <sub>LBKHLR</sub>	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	—	4.5	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	1	_	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	1	_	ns	3
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ</sub>	_	3.8	ns	8

Table 38. Local Bus Genera	I Timing Parameters-	-DLL On
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#### Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one (1). Also, t<sub>LBKH0X</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub></sub>

- 2. All timings are in reference to the rising edge of LSYNC\_IN.
- 3. All signals are measured from  $OV_{DD}/2$  of the rising edge of LSYNC\_IN to  $0.4 \times OV_{DD}$  of the signal in question for 3.3 V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t<sub>LBOTOT1</sub> should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
- 6. t<sub>LBOTOT2</sub> should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
- 7. t<sub>LBOTOT3</sub> should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
- 8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.





Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)



Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

## Table 41. JTAG AC Timing Specifications (Independent of CLKIN)<sup>1</sup> (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t <sub>JTKLDZ</sub> t <sub>JTKLOZ</sub>	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50  $\Omega$  load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>JTDVKH</sub> symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>JTDXKH</sub> symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t<sub>TCLK</sub>.

5. Non-JTAG signal output timing with respect to t<sub>TCLK</sub>.

6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8349EA.



Figure 27. AC Test Load for the JTAG Interface

Figure 28 provides the JTAG clock input timing diagram.



Figure 28. JTAG Clock Input Timing Diagram

Figure 29 provides the  $\overline{\text{TRST}}$  timing diagram.



# 13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8349EA.

# **13.1 PCI DC Electrical Characteristics**

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8349EA.

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	$V_{OUT} \ge V_{OH}$ (min) or	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	$V_{OUT} \le V_{OL}$ (max)	-0.3	0.8	V
Input current	I <sub>IN</sub>	$V_{IN}^{1} = 0 V \text{ or } V_{IN} = OV_{DD}$	_	±5	μA
High-level output voltage	V <sub>OH</sub>	OV <sub>DD</sub> = min, I <sub>OH</sub> = -100 μA	OV <sub>DD</sub> – 0.2	_	V
Low-level output voltage	V <sub>OL</sub>	OV <sub>DD</sub> = min, I <sub>OL</sub> = 100 μA	_	0.2	V

**Table 44. PCI DC Electrical Characteristics** 

Note:

1. The symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1.

# 13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8349EA. Note that the PCI\_CLK or PCI\_SYNC\_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing	Specifications at 66 MHz <sup>1</sup>
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Parameter	Symbol <sup>2</sup>	Min	Мах	Unit	Notes
Clock to output valid	<sup>t</sup> PCKHOV	—	6.0	ns	3
Output hold from clock	t <sub>PCKHOX</sub>	1		ns	3
Clock to output high impedance	t <sub>PCKHOZ</sub>	—	14	ns	3, 4
Input setup to clock	t <sub>PCIVKH</sub>	3.0	_	ns	3, 5
Input hold from clock	t <sub>PCIXKH</sub>	0	_	ns	3, 5
REQ64 to PORESET setup time	t <sub>PCRVRH</sub>	5	—	clocks	6

Figure 37 provides the AC test load for the SPI.



Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 38 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.



Figure 39 shows the SPI timings in master mode (internal clock).



Figure 39. SPI AC Timing in Master Mode (Internal Clock) Diagram

# **18 Package and Pin Listings**

This section details package parameters, pin assignments, and dimensions. The MPC8349EA is available in a tape ball grid array (TBGA). See Section 18.1, "Package Parameters for the MPC8349EA TBGA" and Section 18.2, "Mechanical Dimensions for the MPC8349EA TBGA.

# 18.3 Pinout Listings

Table 55 provides the pin-out listing for the MPC8349EA, 672 TBGA package.

## Table 55. MPC8349EA (TBGA) Pinout Listing

Signal Package Pin Number		Pin Type	Power Supply	Notes
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)			
PCI1_INTA/IRQ_OUT	B34	0	OV <sub>DD</sub>	2
PCI1_RESET_OUT	C33	0	OV <sub>DD</sub>	_
PCI1_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV <sub>DD</sub>	—
PCI1_C/BE[3:0]	J30, M31, P33, T34	I/O	OV <sub>DD</sub>	
PCI1_PAR	P32	I/O	OV <sub>DD</sub>	_
PCI1_FRAME	M32	I/O	OV <sub>DD</sub>	5
PCI1_TRDY	N29	I/O	OV <sub>DD</sub>	5
PCI1_IRDY	M34	I/O	OV <sub>DD</sub>	5
PCI1_STOP	N31	I/O	OV <sub>DD</sub>	5
PCI1_DEVSEL	VSEL N30		OV <sub>DD</sub>	5
PCI1_IDSEL	J31	I	OV <sub>DD</sub>	_
PCI1_SERR	N34	I/O	OV <sub>DD</sub>	5
PCI1_PERR	N33	I/O	OV <sub>DD</sub>	5
PCI1_REQ[0]	D32	I/O	OV <sub>DD</sub>	_
PCI1_REQ[1]/CPCI1_HS_ES	D34	I	OV <sub>DD</sub>	_
PCI1_REQ[2:4]	E34, F32, G29	I	OV <sub>DD</sub>	_
PCI1_GNT0	C34	I/O	OV <sub>DD</sub>	_
PCI1_GNT1/CPCI1_HS_LED	D33	0	OV <sub>DD</sub>	_
PCI1_GNT2/CPCI1_HS_ENUM	E33	0	OV <sub>DD</sub>	_
PCI1_GNT[3:4]	F31, F33	0	OV <sub>DD</sub>	_
PCI2_RESET_OUT/GPIO2[0]	W32	I/O	OV <sub>DD</sub>	_
PCI2_AD[31:0]/PCI1[63:32]	AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30	I/O	OV <sub>DD</sub>	
PCI2_C/BE[3:0]/PCI1_C/BE[7:4]	AC32, AE32, AH31, AL32	I/O	OV <sub>DD</sub>	—
PCI2_PAR/PCI1_PAR64	AG34	I/O	OV <sub>DD</sub>	_

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	_	_	_
GV <sub>DD</sub>	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV <sub>DD</sub>	_
LV <sub>DD1</sub>	C9, D11	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV <sub>DD1</sub>	_
LV <sub>DD2</sub>	C6, D9	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV <sub>DD2</sub>	_
V <sub>DD</sub>	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V <sub>DD</sub>	_
OV <sub>DD</sub>	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV <sub>DD</sub>	_
MVREF1	МЗ	I	DDR reference voltage	_

### Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

RCWL[SPMF]	System PLL Multiplication Factor
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

Table 58. System	n PLL Multi	plication	Factors	(continued)	)
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As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG\_CLKIN\_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI\_CLK) and the internal coherent system bus clock (*csb\_clk*). Table 59 and Table 60 show the expected frequency values for the CSB frequency for select *csb\_clk* to CLKIN/PCI\_SYNC\_IN ratios.

			In	put Clock Fre	quency (MHz	) <sup>2</sup>
CFG_CLKIN_DIV at Reset <sup>1</sup>	SPMF	<i>csb_clk</i> : Input Clock Ratio <sup>2</sup>	16.67	25	33.33	66.67
				<i>csb_clk</i> Frequency (MHz		
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333

Table 59. CSB Frequency Options for Host Mode

### Table 63. Package Thermal Characteristics for TBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	$\Psi_{JT}$	1	°C/W	6

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

# 20.2 Thermal Management Information

For the following sections,  $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$  where  $P_{I/O}$  is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

## 20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T<sub>J</sub>, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)

 $T_A$  = ambient temperature for the package (°C)

 $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity  $T_J - T_A$ ) are possible.

## 20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

#### Thermal

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

 $T_J = T_A + (R_{\theta JA} \times P_D)$ 

where:

 $T_J$  = junction temperature (°C)

 $T_A$  = ambient temperature for the package (°C)

 $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

## 20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter ( $\Psi_{JT}$ ) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)

 $T_T$  = thermocouple temperature on top of package (°C)

 $\Psi_{JT}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

 $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$  = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$  = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$  is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 64 shows heat sink thermal resistance for TBGA of the MPC8349EA.

Host Sink Assuming Thermal Grosse	Air Flow	35  imes 35  mm TBGA
neat Sink Assuming merinal drease		Thermal Resistance
AAVID $30 \times 30 \times 9.4$ mm pin fin	Natural convection	10
AAVID $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.5
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	5.6
AAVID 31 $\times$ 35 $\times$ 23 mm pin fin	Natural convection	8.4
AAVID 31 $\times$ 35 $\times$ 23 mm pin fin	1 m/s	4.7
AAVID 31 $\times$ 35 $\times$ 23 mm pin fin	2 m/s	4
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	5.7
Wakefield, $53 \times 53 \times 25$ mm pin fin	1 m/s	3.5
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	2.7
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	6.7
MEI, 75 $\times$ 85 $\times$ 12 no adjacent board, extrusion	1 m/s	4.1
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	2 m/s	2.8
MEI, $75 \times 85 \times 12$ mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Table 64. Heat Sink and Thermal Resistance of MPC8349EA (TBGA)

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

#### System Design Information

2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, "Core PLL Configuration."

# 21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ( $AV_{DD}1$ ,  $AV_{DD}2$ , respectively). The  $AV_{DD}$  level should always equal to  $V_{DD}$ , and preferably these voltages are derived directly from  $V_{DD}$  through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four  $AV_{DD}$  pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific  $AV_{DD}$  pin being supplied. It should be possible to route directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.



Figure 42. PLL Power Supply Filter Circuit

# 21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8349EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8349EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  pin of the device. These capacitors should receive their power from separate  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1  $\mu$ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330  $\mu$ F (AVX TPS tantalum or Sanyo OSCON).

# 21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to  $OV_{DD}$ ,  $GV_{DD}$ , or  $LV_{DD}$  as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external  $V_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ ,  $OV_{DD}$ , and GND pins of the MPC8349EA.

# 21.5 Output Buffer DC Impedance

The MPC8349EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for  $I^2C$ ).

To measure  $Z_0$  for the single-ended drivers, an external resistor is connected from the chip pad to  $OV_{DD}$  or GND. Then the value of each resistor is varied until the pad voltage is  $OV_{DD}/2$  (see Figure 43). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and  $R_P$  is trimmed until the voltage at the pad equals  $OV_{DD}/2$ .  $R_P$  then becomes the resistance of the pull-up devices.  $R_P$  and  $R_N$  are designed to be close to each other in value. Then,  $Z_0 = (R_P + R_N) \div 2$ .



Figure 43. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{source} \times I_{source}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{term}$ . The measured voltage is