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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349evvajdb

- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- or 64-bit data interface, up to 400 MHz data rate
  - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
  - DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
  - Full error checking and correction (ECC) support
  - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep-mode support for SDRAM self refresh
  - Auto refresh
  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- Dual PCI interfaces
  - Designed to comply with *PCI Specification Revision 2.3*
  - Data bus width options:
    - Dual 32-bit data PCI interfaces operating at up to 66 MHz
    - Single 64-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities on both interfaces
  - PCI agent mode on PCI1 interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8349EA.

Table 6. CLKIN DC Timing Specifications

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	0.5 V ≤V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±50	μA

4.2 AC Electrical Characteristics

The primary clock source for the MPC8349EA can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 50 KHz modulation rate regardless of input frequency.

Table 26. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the GMII receive AC timing diagram.

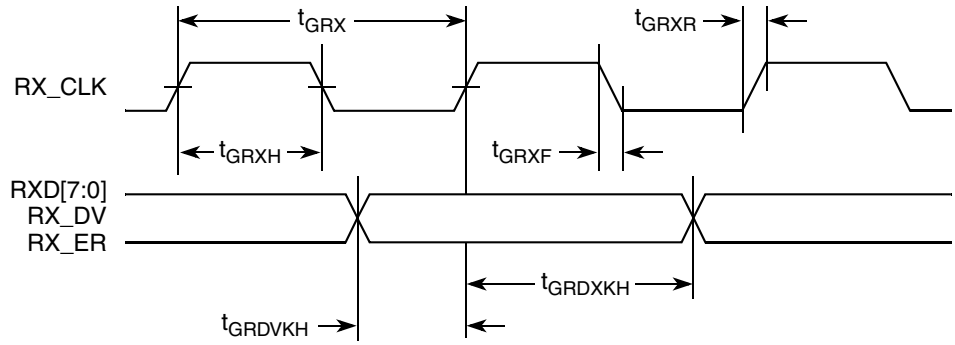

Figure 10. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 27 provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load for TSEC.

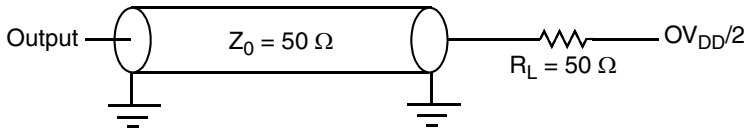

Figure 12. TSEC AC Test Load

Figure 13 shows the MII receive AC timing diagram.

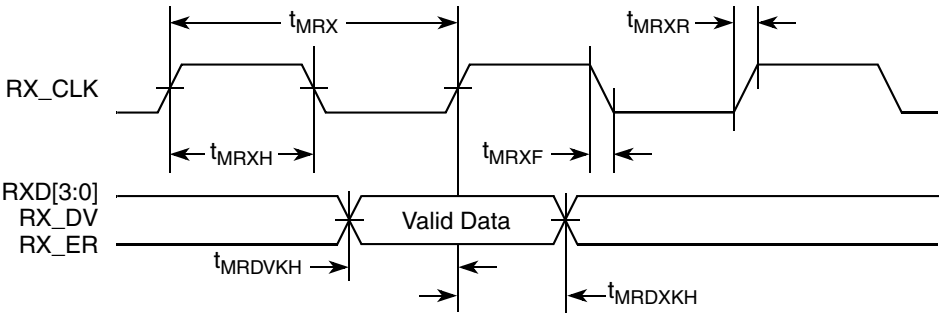

Figure 13. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

Figure 16 shows the RBMII and RTBI AC timing and multiplexing diagrams.

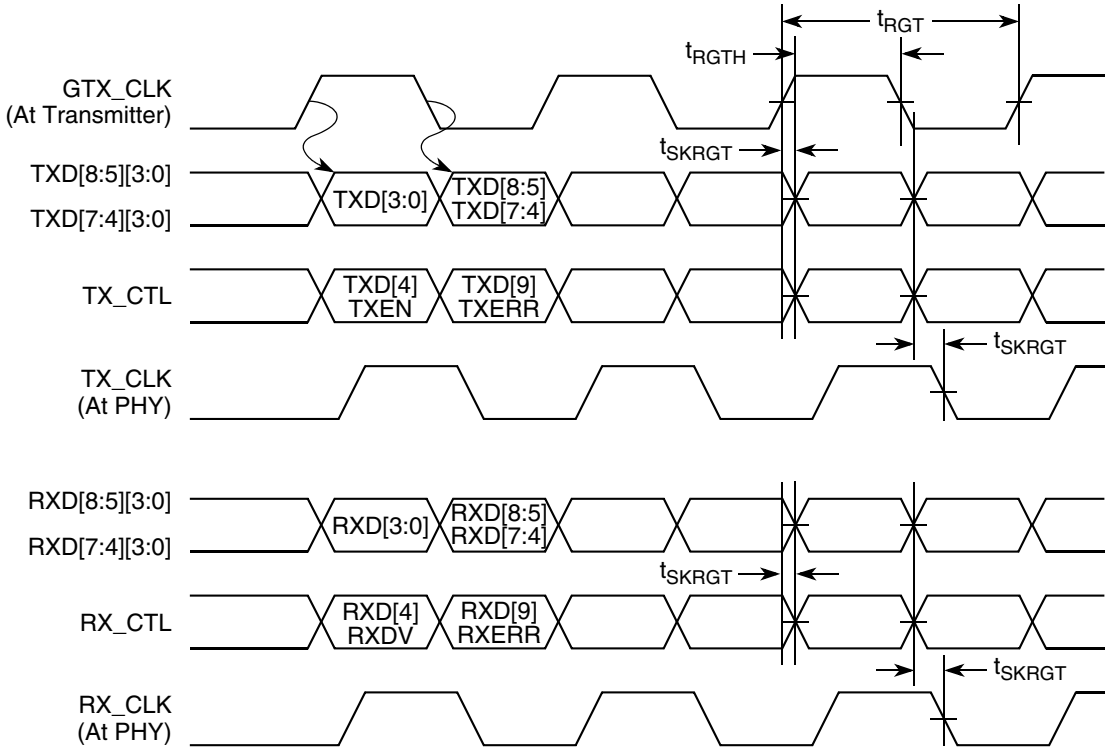

Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 32 and Table 33.

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	—	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V

Table 34. MII Management AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 17 shows the MII management AC timing diagram.

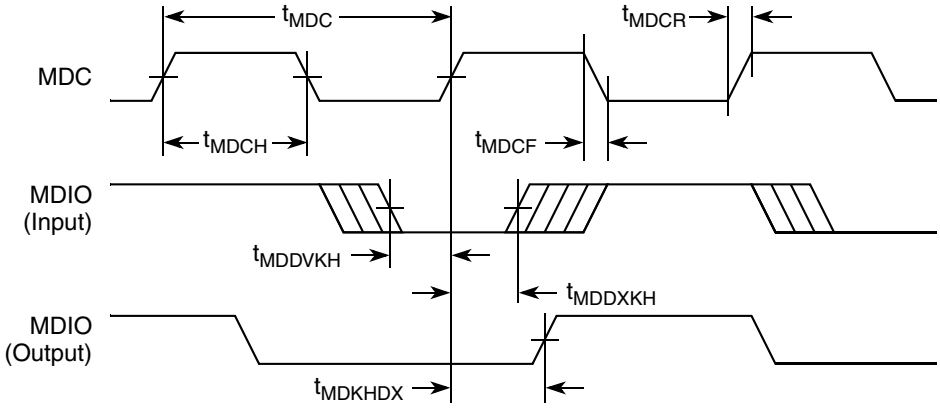

Figure 17. MII Management Interface Timing Diagram

Figure 30 provides the boundary-scan timing diagram.

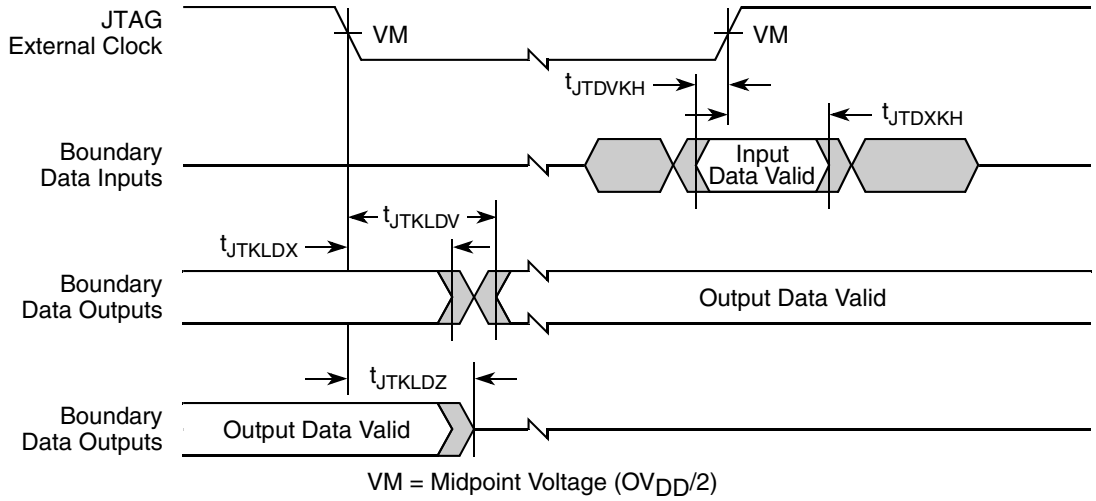

Figure 30. Boundary-Scan Timing Diagram

Figure 31 provides the test access port timing diagram.

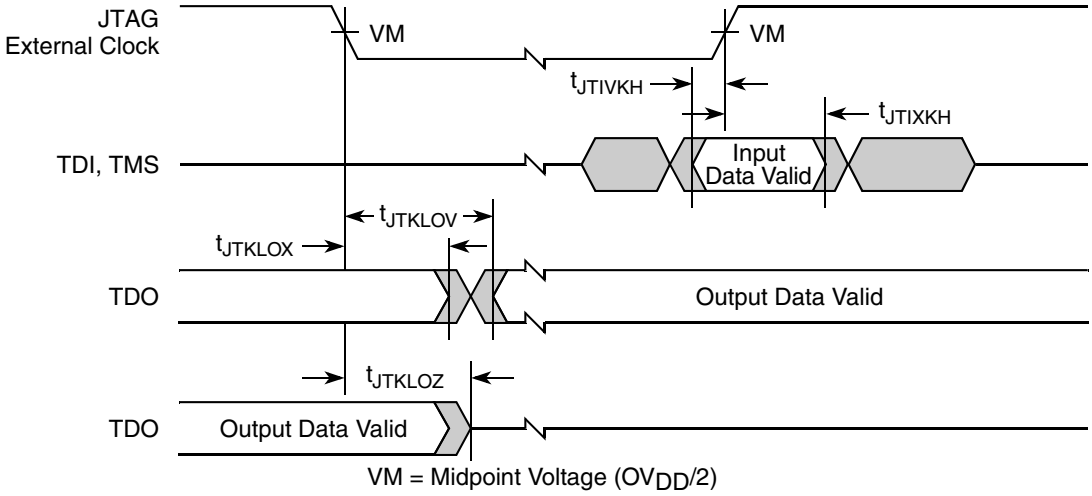

Figure 31. Test Access Port Timing Diagram

Figure 34 provides the AC test load for PCI.

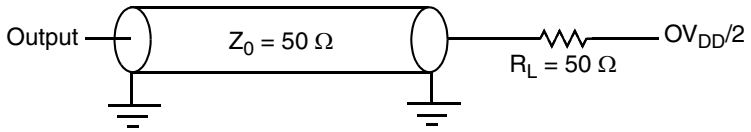

Figure 34. PCI AC Test Load

Figure 35 shows the PCI input AC timing diagram.

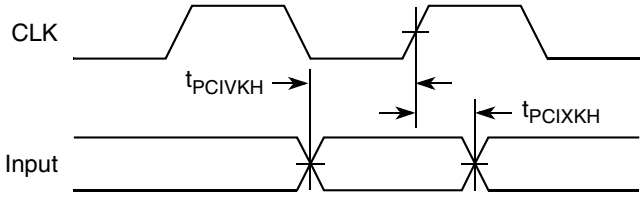

Figure 35. PCI Input AC Timing Diagram

Figure 36 shows the PCI output AC timing diagram.

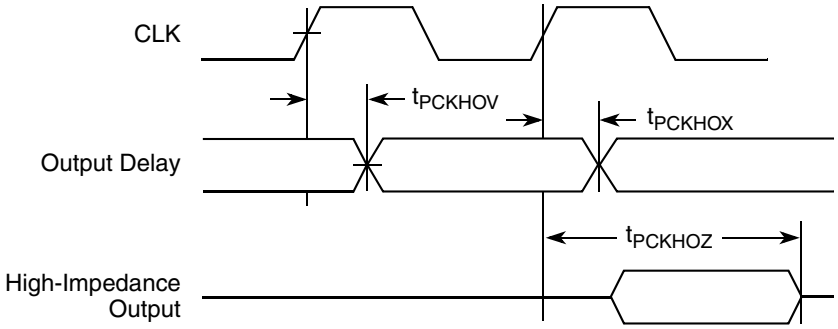

Figure 36. PCI Output AC Timing Diagram

14 Timers

This section describes the DC and AC electrical specifications for the timers.

14.1 Timer DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the MPC8349EA timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 47. Timer DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V

15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

Table 50. GPIO Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the external interrupt pins.

Table 51. IPIC DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	—	—	±5	μA	—
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	2

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, and $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 52 provides the IPIC input and output AC timing specifications.

Table 52. IPIC Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PICWID}	20	ns

Notes:
1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}	—	6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}	—	8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2	—	ns
SPI inputs—Master mode (internal clock input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MBA[2]	H4	O	GV_{DD}	—
MDIC0	AB1	I/O	—	9
MDIC1	AA1	I/O	—	9
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV_{DD}	—
LDP[0]/$\overline{\text{CKSTOP\_OUT}}$	AM21	I/O	OV_{DD}	—
LDP[1]/$\overline{\text{CKSTOP\_IN}}$	AP22	I/O	OV_{DD}	—
LDP[2]/$\overline{\text{LCS}}$[4]	AN22	I/O	OV_{DD}	—
LDP[3]/$\overline{\text{LCS}}$[5]	AM22	I/O	OV_{DD}	—
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV_{DD}	—
$\overline{\text{LCS}}$[0:3]	AN24, AL23, AP25, AN25	O	OV_{DD}	—
$\overline{\text{LWE}}$[0:3]/LSDDQM[0:3]/$\overline{\text{LBS}}$[0:3]	AK23, AP26, AL24, AM25	O	OV_{DD}	—
LBCTL	AN26	O	OV_{DD}	—
LALE	AK24	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV_{DD}	—
LGPL1/$\overline{\text{LSDWE}}$/cfg_reset_source1	AL25	I/O	OV_{DD}	—
LGPL2/$\overline{\text{LSDRAS}}$/$\overline{\text{LOE}}$	AJ24	O	OV_{DD}	—
LGPL3/$\overline{\text{LSDCAS}}$/cfg_reset_source2	AN27	I/O	OV_{DD}	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	AP28	I/O	OV_{DD}	12
LGPL5/cfg_clkin_div	AL26	I/O	OV_{DD}	—
LCKE	AM27	O	OV_{DD}	—
LCLK[0:2]	AN28, AK26, AP29	O	OV_{DD}	—
LSYNC_OUT	AM12	O	OV_{DD}	—
LSYNC_IN	AJ10	I	OV_{DD}	—
General Purpose I/O Timers				
GPIO1[0]/$\overline{\text{DMA\_DREQ0}}$/GTM1_TIN1/ GTM2_TIN2	F24	I/O	OV_{DD}	—
GPIO1[1]/$\overline{\text{DMA\_DACK0}}$/ $\overline{\text{GTM1\_TGATE1}}$/$\overline{\text{GTM2\_TGATE2}}$	E24	I/O	OV_{DD}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO1[2]/DMA_DDONE0/ GTM1_TOUT1	B25	I/O	OV_{DD}	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	D24	**I/O**	OV_{DD}	—
GPIO1[4]/DMA_DACK1/ GTM1_TGATE2/GTM2_TGATE1	A25	**I/O**	OV_{DD}	—
GPIO1[5]/DMA_DDONE1/ GTM1_TOUT2/GTM2_TOUT1	B24	**I/O**	OV_{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	A24	**I/O**	OV_{DD}	—
GPIO1[7]/DMA_DACK2/ GTM1_TGATE3/GTM2_TGATE4	D23	**I/O**	OV_{DD}	—
GPIO1[8]/DMA_DDONE2/ GTM1_TOUT3	B23	**I/O**	OV_{DD}	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	A23	**I/O**	OV_{DD}	—
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	F22	**I/O**	OV_{DD}	—
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	E22	**I/O**	OV_{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/ DR_D0_ENABLEN	A26	I/O	OV_{DD}	—
MPH1_D1_SER_TXD/ DR_D1_SER_TXD	B26	I/O	OV_{DD}	—
MPH1_D2_VMO_SE0/ DR_D2_VMO_SE0	D25	I/O	OV_{DD}	—
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV_{DD}	—
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV_{DD}	—
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV_{DD}	—
MPH1_D6_SER_RCV/ DR_D6_SER_RCV	D26	I/O	OV_{DD}	—
MPH1_D7_DRVVBUS/ DR_D7_DRVVBUS	E26	I/O	OV_{DD}	—
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV_{DD}	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV_{DD}	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	O	OV_{DD}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	B20	O	OV_{DD}	3
TMS	A20	I	OV_{DD}	4
$\overline{\text{TRST}}$	B19	I	OV_{DD}	4
Test				
TEST	D22	I	OV_{DD}	6
TEST_SEL	AL13	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	A18	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	C18	I	OV_{DD}	—
$\overline{\text{HRESET}}$	B18	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	D18	I/O	OV_{DD}	2
Thermal Management				
THERM0	K32	I	—	8
Power and Ground Signals				
$AV_{DD}1$	L31	Power for e300 PLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}1$	—
$AV_{DD}2$	AP12	Power for system PLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}2$	—
$AV_{DD}3$	AE1	Power for DDR DLL (1.2 V nominal, 1.3 V for 667 MHz)	—	—
$AV_{DD}4$	AJ13	Power for LBIU DLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}4$	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF2	AD2	I	DDR reference voltage	—

Notes:
1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be left not connected.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.
10. TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
11. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to LV_{DD1}.
12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

19 Clocking

Figure 41 shows the internal distribution of the clocks.

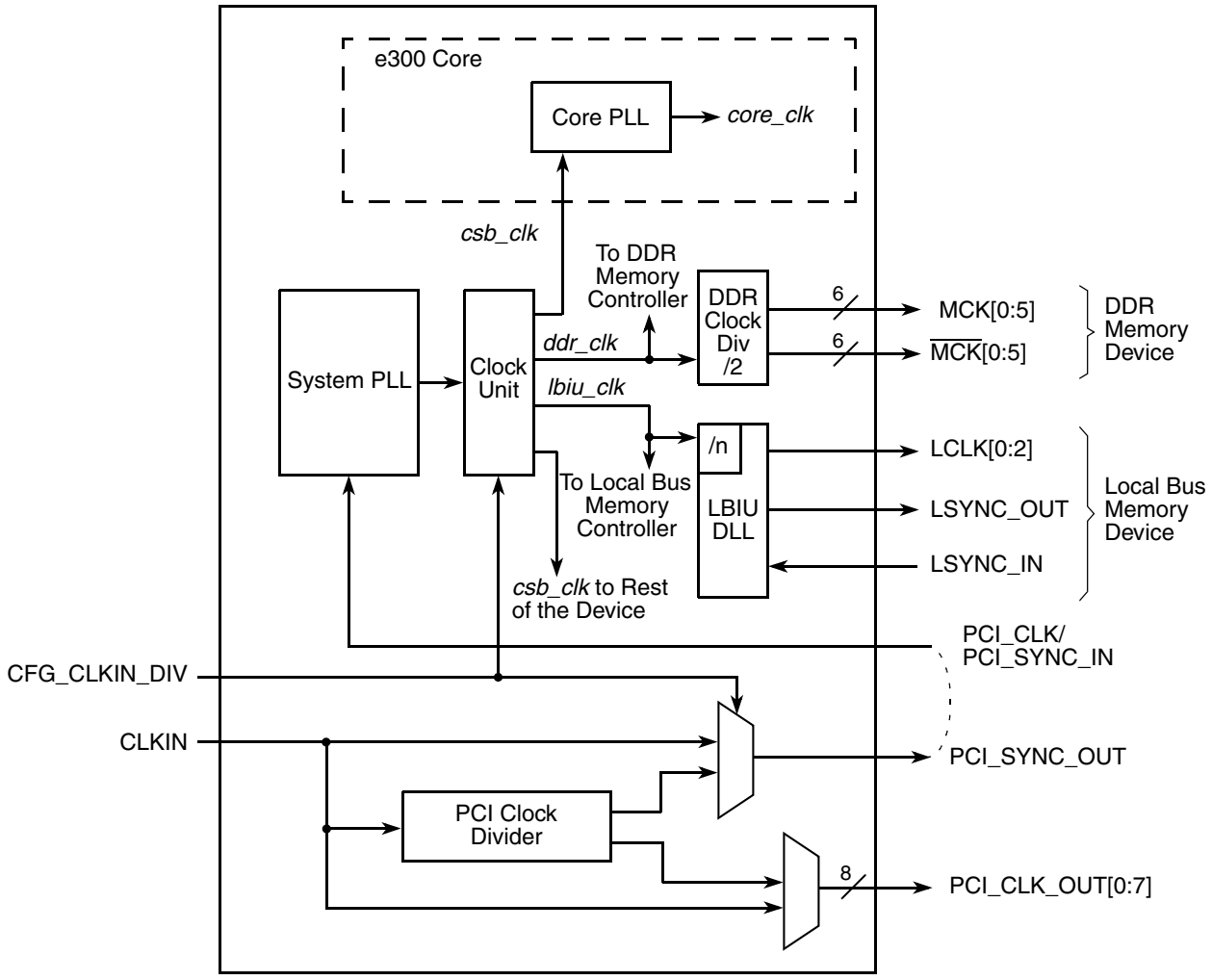

Figure 41. MPC8349EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8349EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8349EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

Table 60. CSB Frequency Options for Agent Mode (continued)

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

1 CFG_CLKIN_DIV doubles csb_clk if set high.
2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 61 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 61 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 64 shows heat sink thermal resistance for TBGA of the MPC8349EA.

Table 64. Heat Sink and Thermal Resistance of MPC8349EA (TBGA)

Heat Sink Assuming Thermal Grease	Air Flow	35 × 35 mm TBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.5
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.6
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.4
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.7
AAVID 31 × 35 × 23 mm pin fin	2 m/s	4
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.7
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.5
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	4.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.8
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-567-8082
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI) 408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics 800-522-2800
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering 603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Dow-Corning Electronic Materials
P.O. Box 994
Midland, MI 48686-0997
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, "Core PLL Configuration."

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The AV_{DD} level should always equal to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four AV_{DD} pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV_{DD} pin being supplied. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.

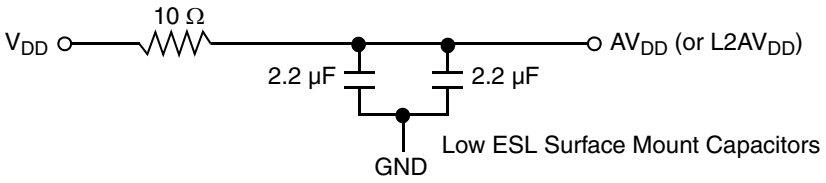

Figure 42. PLL Power Supply Filter Circuit

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8349EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8349EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

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