


**Understanding Embedded - Microprocessors**

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

**Applications of Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 533MHz |
| Co-Processors/DSP | Security; SEC |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 672-LBGA |
| Supplier Device Package | 672-LBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349evvajf |

**NOTE**

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

# 1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8349EA.

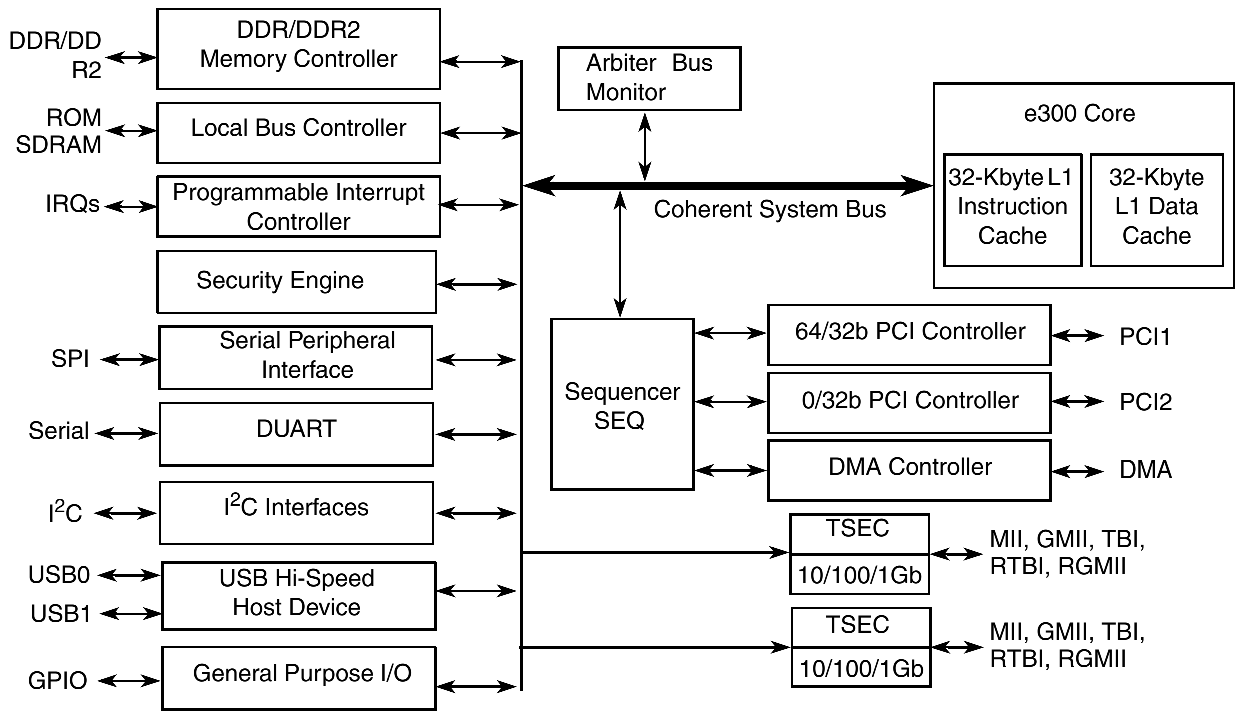


**Figure 1. MPC8349EA Block Diagram**

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  — High-performance, superscalar processor core
  — Floating-point, integer, load/store, system register, and branch processing units
  — 32-Kbyte instruction cache, 32-Kbyte data cache
  — Lockable portion of L1 cache
  — Dynamic power management
  — Software-compatible with the other Freescale processor families that implement Power Architecture technology

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Parameter | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core supply voltage | | $V_{DD}$ | –0.3 to 1.32 (1.36 max for 667-MHz core frequency) | V | — |
| PLL supply voltage | | $AV_{DD}$ | –0.3 to 1.32 (1.36 max for 667-MHz core frequency) | V | — |
| DDR and DDR2 DRAM I/O voltage | | $GV_{DD}$ | –0.3 to 2.75<br>–0.3 to 1.98 | V | — |
| Three-speed Ethernet I/O, MII management voltage | | $LV_{DD}$ | –0.3 to 3.63 | V | — |
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | — |
| Input voltage | DDR DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | DDR DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | Three-speed Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | 4, 5 |
| | Local bus, DUART, CLKIN, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3, 5 |
| | PCI | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 6 |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**

1 Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2 **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3 **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4 **Caution:** $LV_{IN}$ must not exceed $LV_{DD}$ by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5 (M,L,O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

6 OVIN on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

**Table 21. DUART DC Electrical Characteristics (continued)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

## 7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

**Table 22. DUART AC Timing Specifications**

| Parameter | Value | Unit | Notes |
|---|---|---|---|
| Minimum baud rate | 256 | baud | — |
| Maximum baud rate | > 1,000,000 | baud | 1 |
| Oversample rate | 16 | — | 2 |

**Notes:**
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

# 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

## 8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

**Table 27. MII Transmit AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK data clock rise (20%–80%) | $t_{MTXR}$ | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%–20%) | $t_{MTXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time $t_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of $t_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 shows the MII transmit AC timing diagram.

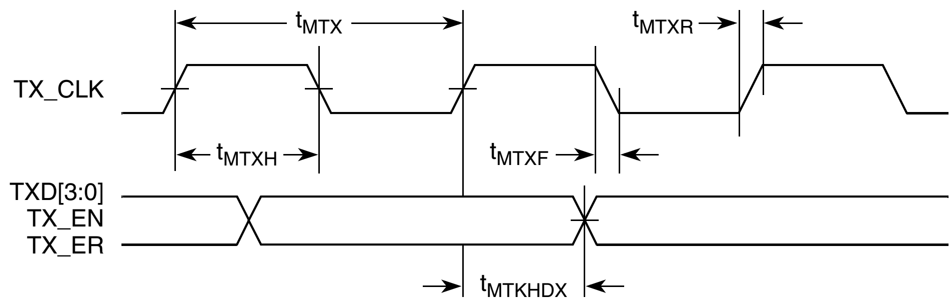


**Figure 11. MII Transmit AC Timing Diagram**

### 8.2.2.2 MII Receive AC Timing Specifications

Table 28 provides the MII receive AC timing specifications.

**Table 28. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |

Figure 18 and Figure 19 provide the AC test load and signals for the USB, respectively.

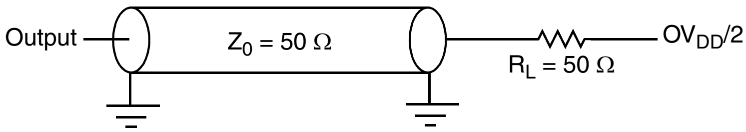


**Figure 18. USB AC Test Load**

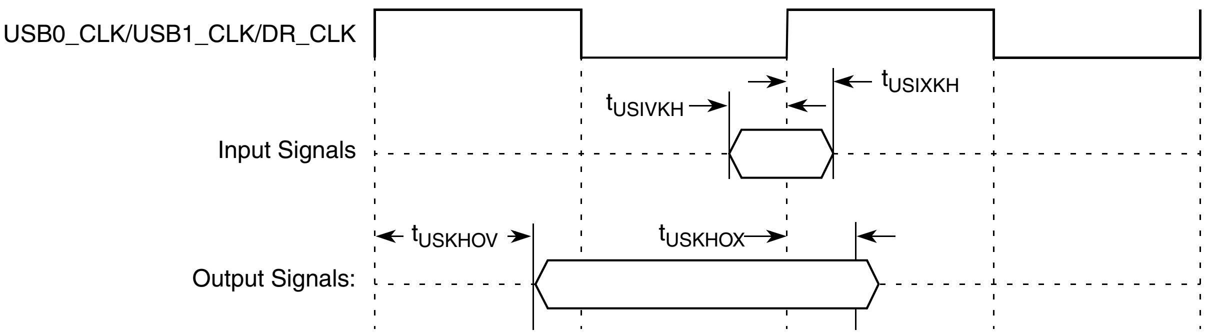


**Figure 19. USB Signals**

# 10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8349EA.

## 10.1 Local Bus DC Electrical Characteristics

Table 37 provides the DC electrical characteristics for the local bus interface.

**Table 37. Local Bus DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | ±5 | μA |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage, $I_{OL}$ = 100 μA | $V_{OL}$ | — | 0.2 | V |

## 10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8349EA.

**Table 38. Local Bus General Timing Parameters—DLL On**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 7.5 | — | ns | 2 |
| Input setup to local bus clock (except LUPWAIT) | $t_{LBIVKH1}$ | 1.5 | — | ns | 3, 4 |
| LUPWAIT input setup to local bus clock | $t_{LBIVKH2}$ | 2.2 | — | ns | 3, 4 |
| Input hold from local bus clock (except LUPWAIT) | $t_{LBIXKH1}$ | 1.0 | — | ns | 3, 4 |
| LUPWAIT Input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |
| Local bus clock to LALE rise | $t_{LBKHLR}$ | — | 4.5 | ns | — |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 4.5 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 4.5 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 4.5 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 1 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 1 | — | ns | 3 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ}$ | — | 3.8 | ns | 8 |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

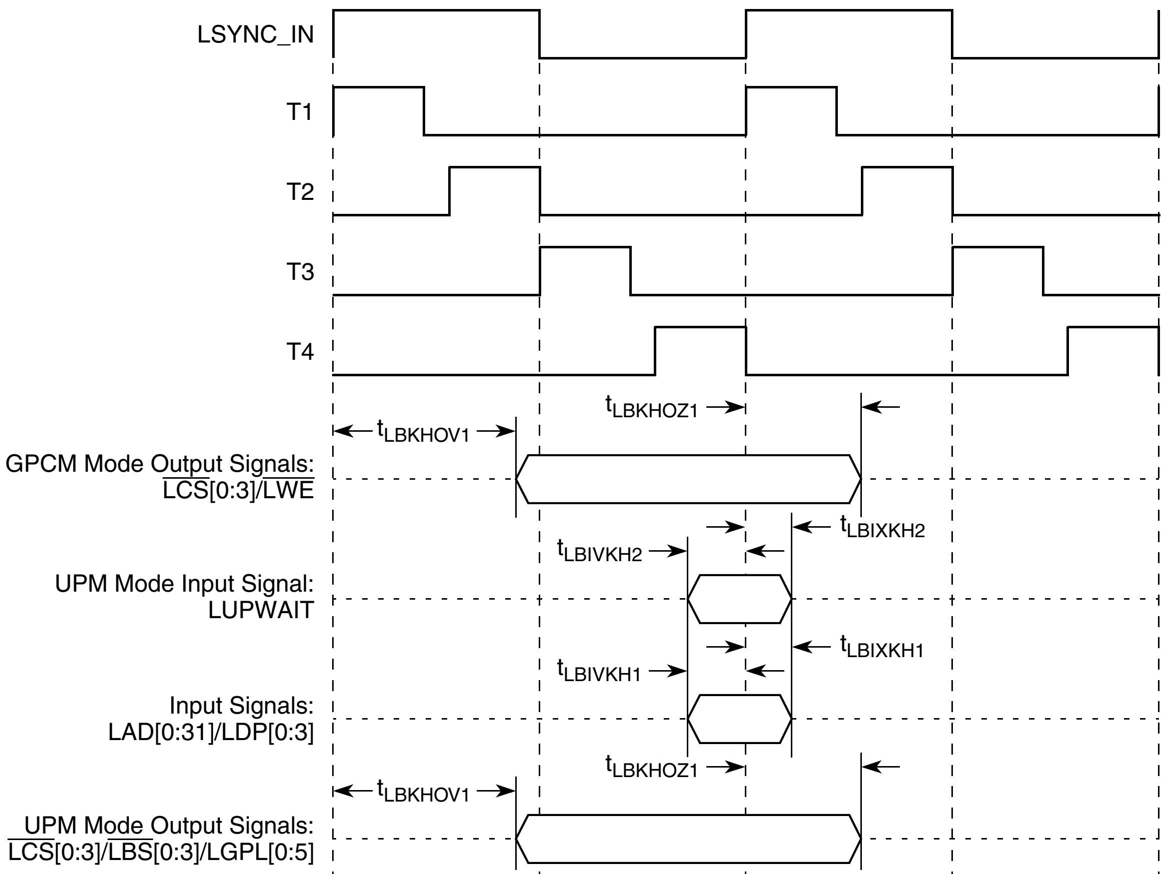


**Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)**

# 11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA.

## 11.1 JTAG DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA.

**Table 40. JTAG Interface DC Electrical Characteristics**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | $OV_{DD}$ – 0.3 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |

**Table 45. PCI AC Timing Specifications at 66 MHz[1] (continued)**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{PORESET}}$ to $\overline{\text{REQ64}}$ hold time | $t_{PCRHRX}$ | 0 | 50 | ns | 6 |

**Notes:**
1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The setup and hold time is with respect to the rising edge of $\overline{\text{PORESET}}$.

Table 46 provides the PCI AC timing specifications at 33 MHz.

**Table 46. PCI AC Timing Specifications at 33 MHz**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 11 | ns | 2 |
| Output hold from clock | $t_{PCKHOX}$ | 2 | — | ns | 2 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 2, 3 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 2, 4 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 2, 4 |
| $\overline{\text{REQ64}}$ to $\overline{\text{PORESET}}$ setup time | $t_{PCRVRH}$ | 5 | — | clocks | 5 |
| $\overline{\text{PORESET}}$ to $\overline{\text{REQ64}}$ hold time | $t_{PCRHRX}$ | 0 | 50 | ns | 5 |

**Notes:**
1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{PCIVKH}$ symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, $t_{SYS}$, reference (K) going to the high (H) state or setup time. Also, $t_{PCRHFV}$ symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The setup and hold time is with respect to the rising edge of $\overline{\text{PORESET}}$.

## 15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

**Table 50. GPIO Input AC Timing Specifications[1]**

| Parameter | Symbol[2] | Min | Unit |
|---|---|---|---|
| GPIO inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns |

**Notes:**

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least $t_{PIWID}$ ns to ensure proper operation.

# 16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

## 16.1 IPIC DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the external interrupt pins.

**Table 51. IPIC DC Electrical Characteristics[1]**

| Parameter | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V | — |
| Input current | $I_{IN}$ | — | — | ±5 | μA | — |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V | 2 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V | 2 |

**Notes:**

1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, and $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open-drain pins; thus $V_{OH}$ is not relevant for those pins.

## 16.2 IPIC AC Timing Specifications

Table 52 provides the IPIC input and output AC timing specifications.

**Table 52. IPIC Input AC Timing Specifications[1]**

| Parameter | Symbol[2] | Min | Unit |
|---|---|---|---|
| IPIC inputs—minimum pulse width | $t_{PICWID}$ | 20 | ns |

**Notes:**

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least $t_{PICWID}$ ns to ensure proper operation in edge triggered mode.

## 18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

| | |
|---|---|
| Package outline | 35 mm × 35 mm |
| Interconnects | 672 |
| Pitch | 1.00 mm |
| Module height (typical) | 1.46 mm |
| Solder balls | 62 Sn/36 Pb/2 Ag (ZU package)<br>96.5 Sn/3.5Ag (VV package) |
| Ball diameter (typical) | 0.64 mm |

## 18.3 Pinout Listings

Table 55 provides the pin-out listing for the MPC8349EA, 672 TBGA package.

**Table 55. MPC8349EA (TBGA) Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI1 and PCI2 (One 64-Bit or Two 32-Bit)** | | | | |
| PCI1_INTA/IRQ_OUT | B34 | O | $OV_{DD}$ | 2 |
| PCI1_RESET_OUT | C33 | O | $OV_{DD}$ | — |
| PCI1_AD[31:0] | G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34 | I/O | $OV_{DD}$ | — |
| PCI1_C/BE[3:0] | J30, M31, P33, T34 | I/O | $OV_{DD}$ | — |
| PCI1_PAR | P32 | I/O | $OV_{DD}$ | — |
| PCI1_FRAME | M32 | I/O | $OV_{DD}$ | 5 |
| PCI1_TRDY | N29 | I/O | $OV_{DD}$ | 5 |
| PCI1_IRDY | M34 | I/O | $OV_{DD}$ | 5 |
| PCI1_STOP | N31 | I/O | $OV_{DD}$ | 5 |
| PCI1_DEVSEL | N30 | I/O | $OV_{DD}$ | 5 |
| PCI1_IDSEL | J31 | I | $OV_{DD}$ | — |
| PCI1_SERR | N34 | I/O | $OV_{DD}$ | 5 |
| PCI1_PERR | N33 | I/O | $OV_{DD}$ | 5 |
| PCI1_REQ[0] | D32 | I/O | $OV_{DD}$ | — |
| PCI1_REQ[1]/CPCI1_HS_ES | D34 | I | $OV_{DD}$ | — |
| PCI1_REQ[2:4] | E34, F32, G29 | I | $OV_{DD}$ | — |
| PCI1_GNT0 | C34 | I/O | $OV_{DD}$ | — |
| PCI1_GNT1/CPCI1_HS_LED | D33 | O | $OV_{DD}$ | — |
| PCI1_GNT2/CPCI1_HS_ENUM | E33 | O | $OV_{DD}$ | — |
| PCI1_GNT[3:4] | F31, F33 | O | $OV_{DD}$ | — |
| PCI2_RESET_OUT/GPIO2[0] | W32 | I/O | $OV_{DD}$ | — |
| PCI2_AD[31:0]/PCI1[63:32] | AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30 | I/O | $OV_{DD}$ | — |
| PCI2_C/BE[3:0]/PCI1_C/BE[7:4] | AC32, AE32, AH31, AL32 | I/O | $OV_{DD}$ | — |
| PCI2_PAR/PCI1_PAR64 | AG34 | I/O | $OV_{DD}$ | — |

**Table 55. MPC8349EA (TBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| GPIO1[2]/DMA_DDONE0/ GTM1_TOUT1 | B25 | I/O | $OV_{DD}$ | — |
| GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1 | D24 | **I/O** | $OV_{DD}$ | — |
| GPIO1[4]/DMA_DACK1/ GTM1_TGATE2/GTM2_TGATE1 | A25 | **I/O** | $OV_{DD}$ | — |
| GPIO1[5]/DMA_DDONE1/ GTM1_TOUT2/GTM2_TOUT1 | B24 | **I/O** | $OV_{DD}$ | — |
| GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4 | A24 | **I/O** | $OV_{DD}$ | — |
| GPIO1[7]/DMA_DACK2/ GTM1_TGATE3/GTM2_TGATE4 | D23 | **I/O** | $OV_{DD}$ | — |
| GPIO1[8]/DMA_DDONE2/ GTM1_TOUT3 | B23 | **I/O** | $OV_{DD}$ | — |
| GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3 | A23 | **I/O** | $OV_{DD}$ | — |
| GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3 | F22 | **I/O** | $OV_{DD}$ | — |
| GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3 | E22 | **I/O** | $OV_{DD}$ | — |
| **USB Port 1** | | | | |
| MPH1_D0_ENABLEN/ DR_D0_ENABLEN | A26 | I/O | $OV_{DD}$ | — |
| MPH1_D1_SER_TXD/ DR_D1_SER_TXD | B26 | I/O | $OV_{DD}$ | — |
| MPH1_D2_VMO_SE0/ DR_D2_VMO_SE0 | D25 | I/O | $OV_{DD}$ | — |
| MPH1_D3_SPEED/DR_D3_SPEED | A27 | I/O | $OV_{DD}$ | — |
| MPH1_D4_DP/DR_D4_DP | B27 | I/O | $OV_{DD}$ | — |
| MPH1_D5_DM/DR_D5_DM | C27 | I/O | $OV_{DD}$ | — |
| MPH1_D6_SER_RCV/ DR_D6_SER_RCV | D26 | I/O | $OV_{DD}$ | — |
| MPH1_D7_DRVVBUS/ DR_D7_DRVVBUS | E26 | I/O | $OV_{DD}$ | — |
| MPH1_NXT/DR_SESS_VLD_NXT | D27 | I | $OV_{DD}$ | — |
| MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP | A28 | I/O | $OV_{DD}$ | — |
| MPH1_STP_SUSPEND/ DR_STP_SUSPEND | F26 | O | $OV_{DD}$ | — |

Table 57 provides the operating frequencies for the MPC8349EA TBGA under recommended operating conditions (see Table 2).

**Table 57. Operating Frequencies for TBGA**

| Characteristic[1] | 400 MHz | 533 MHz | 667 MHz | Unit |
|---|---|---|---|---|
| e300 core frequency (*core_clk*) | 266–400 | 266–533 | 266–667 | MHz |
| Coherent system bus frequency (*csb_clk*) | 100–266 | 100–333 | 100–333 | MHz |
| DDR1 memory bus frequency (MCK)[2] | 100–133 | 100–133 | 100–166.67 | MHz |
| DDR2 memory bus frequency (MCK)[3] | 100–133 | 100–133 | 100–200 | MHz |
| Local bus frequency (LCLK*n*)[4] | 16.67–133 | 16.67–133 | 16.67–133 | MHz |
| PCI input frequency (CLKIN or PCI_CLK) | 25–66 | 25–66 | 25–66 | MHz |
| Security core maximum internal operating frequency | 133 | 133 | 166 | MHz |
| USB_DR, USB_MPH maximum internal operating frequency | 133 | 133 | 166 | MHz |

1 The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM] and SCCR[USBMPHCM] must be programmed so that the maximum internal operating frequency of the security core and USB modules does not exceed the respective values listed in this table.
2 The DDR data rate is 2x the DDR memory bus frequency.
3 The DDR data rate is 2x the DDR memory bus frequency.
4 The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 22.1, “Part Numbers Fully Addressed by This Document,” for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

## 19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

**Table 58. System PLL Multiplication Factors**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0000 | × 16 |
| 0001 | Reserved |
| 0010 | × 2 |
| 0011 | × 3 |
| 0100 | × 4 |
| 0101 | × 5 |
| 0110 | × 6 |

**Table 60. CSB Frequency Options for Agent Mode (continued)**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |
| High | 0010 | 4 : 1 | | 100 | 133 | 266 |
| High | 0011 | 6 : 1 | 100 | 150 | 200 | |
| High | 0100 | 8 : 1 | 133 | 200 | 266 | |
| High | 0101 | 10 : 1 | 166 | 250 | 333 | |
| High | 0110 | 12 : 1 | 200 | 300 | | |
| High | 0111 | 14 : 1 | 233 | | | |
| High | 1000 | 16 : 1 | 266 | | | |

1 CFG_CLKIN_DIV doubles csb_clk if set high.
2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

## 19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 61 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 61 should be considered as reserved.

**NOTE**

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

**Table 61. e300 Core PLL Configuration**

| RCWL[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider[1] |
|---|---|---|---|---|
| 0–1 | 2–5 | 6 | | |
| nn | 0000 | n | PLL bypassed (PLL off, *csb_clk* clocks core directly) | PLL bypassed (PLL off, *csb_clk* clocks core directly) |
| 00 | 0001 | 0 | 1:1 | 2 |
| 01 | 0001 | 0 | 1:1 | 4 |
| 10 | 0001 | 0 | 1:1 | 8 |
| 11 | 0001 | 0 | 1:1 | 8 |
| 00 | 0001 | 1 | 1.5:1 | 2 |
| 01 | 0001 | 1 | 1.5:1 | 4 |
| 10 | 0001 | 1 | 1.5:1 | 8 |
| 11 | 0001 | 1 | 1.5:1 | 8 |
| 00 | 0010 | 0 | 2:1 | 2 |
| 01 | 0010 | 0 | 2:1 | 4 |
| 10 | 0010 | 0 | 2:1 | 8 |
| 11 | 0010 | 0 | 2:1 | 8 |
| 00 | 0010 | 1 | 2.5:1 | 2 |
| 01 | 0010 | 1 | 2.5:1 | 4 |
| 10 | 0010 | 1 | 2.5:1 | 8 |
| 11 | 0010 | 1 | 2.5:1 | 8 |
| 00 | 0011 | 0 | 3:1 | 2 |
| 01 | 0011 | 0 | 3:1 | 4 |
| 10 | 0011 | 0 | 3:1 | 8 |
| 11 | 0011 | 0 | 3:1 | 8 |

[1] Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

**Table 62. Suggested PLL Configurations (continued)**

| Ref No.[1] | RCWL | | 400 MHz Device | | | 533 MHz Device | | | 667 MHz Device | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | SPMF | CORE PLL | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) | Input Clock Freq (MHz)[2] | CSB Freq (MHz) | Core Freq (MHz) |
| **306** | **0011** | **0000110** | | — | | | — | | 66 | 200 | 600 |
| **405** | **0100** | **0000101** | | — | | | — | | 66 | 266 | 667 |
| **504** | **0101** | **0000100** | | — | | | — | | 66 | 333 | 667 |

[1] The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

[2] The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

# 20 Thermal

This section describes the thermal specifications of the MPC8349EA.

## 20.1 Thermal Characteristics

Table 63 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8349EA.

**Table 63. Package Thermal Characteristics for TBGA**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient natural convection on single-layer board (1s) | $R_{\theta JA}$ | 14 | °C/W | 1, 2 |
| Junction-to-ambient natural convection on four-layer board (2s2p) | $R_{\theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction-to-ambient (at 200 ft/min) on single-layer board (1s) | $R_{\theta JMA}$ | 11 | °C/W | 1, 3 |
| Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p) | $R_{\theta JMA}$ | 8 | °C/W | 1, 3 |
| Junction-to-ambient (at 2 m/s) on single-layer board (1s) | $R_{\theta JMA}$ | 9 | °C/W | 1, 3 |
| Junction-to-ambient (at 2 m/s) on four-layer board (2s2p) | $R_{\theta JMA}$ | 7 | °C/W | 1, 3 |
| Junction-to-board thermal | $R_{\theta JB}$ | 3.8 | °C/W | 4 |
| Junction-to-case thermal | $R_{\theta JC}$ | 1.7 | °C/W | 5 |

The Bergquist Company 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

## 20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

### 20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_C$ = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$P_D$ = power dissipation (W)

# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8349EA.

## 21.1 System Clocking

The MPC8349EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, "System PLL Configuration."

2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, “Core PLL Configuration.”

## 21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The $AV_{DD}$ level should always equal to $V_{DD}$, and preferably these voltages are derived directly from $V_{DD}$ through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four $AV_{DD}$ pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific $AV_{DD}$ pin being supplied. It should be possible to route directly from the capacitors to the $AV_{DD}$ pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.

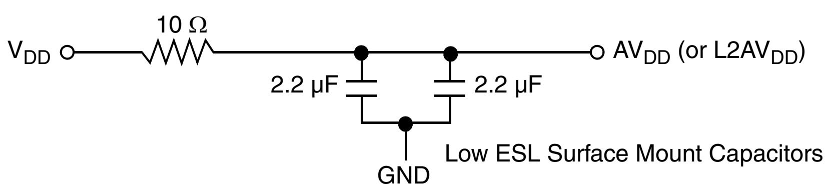


**Figure 42. PLL Power Supply Filter Circuit**

## 21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8349EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8349EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each $V_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ pin of the device. These capacitors should receive their power from separate $V_{DD}$, $OV_{DD}$, $GV_{DD}$, $LV_{DD}$, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the $V_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

**Table 68. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 3 | 11/2006 | • Updated note in introduction.<br>• In the features list in Section 1, “Overview,” updated DDR data rate to show 400 MHz for DDR2 for TBGA parts for silicon 3.x and 400 MHz for DDR2 for TBGA parts for silicon 3.x.<br>• In Section 23, “Ordering Information,” replicated note from document introduction. |
| 2 | 8/2006 | • Changed all references to revision 2.0 silicon to revision 3.0 silicon.<br>• Changed VIH minimum value in Table 40, “JTAG Interface DC Electrical Characteristics,” to $OV_{DD}$ – 0.3.<br>• In Table 44, “PCI DC Electrical Characteristics,” changed high-level input voltage values to min = 2 and max = $OV_{DD}$ + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8.<br>• Updated DDR2 I/O power values in Table 5, “MPC8347EA Typical I/O Power Dissipation.”<br>• In Table 66, “Suggested PLL Configurations,” deleted reference-number rows 902 and 703. |
| 1 | 4/2006 | • Removed Table 20, “Timing Parameters for DDR2-400.”<br>• Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, “DDR and DDR2 SDRAM Output AC Timing Specifications,” rows 2 and 3, and in Figure 2, “DDR SDRAM Output Timing Diagram.<br>• Changed Min and Max values for $V_{IH}$ and VIL in Table 40Table 44,“PCI DC Electrical Characteristics.”<br>• In Table 55, “MPC8349EA (TBGA) Pinout Listing,” and Table 52, “MPC8347EA (PBGA) Pinout Listing,” modified rows for MDICO and MDIC1 signals and added note ‘It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor.’<br>• Table 55, “MPC8349EA (TBGA) Pinout Listing,” in row AVDD3 changed power supply from “AVDD3” to ‘—.’ |
| 0 | 3/2006 | Initial public release |

***How to Reach Us:***

**Home Page:**
www.freescale.com

**Web Support:**
http://www.freescale.com/support

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

**For Literature Requests Only:**
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com



Document Number: MPC8349EAEC
Rev. 13
09/2011