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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349evvajfb

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8349EA.

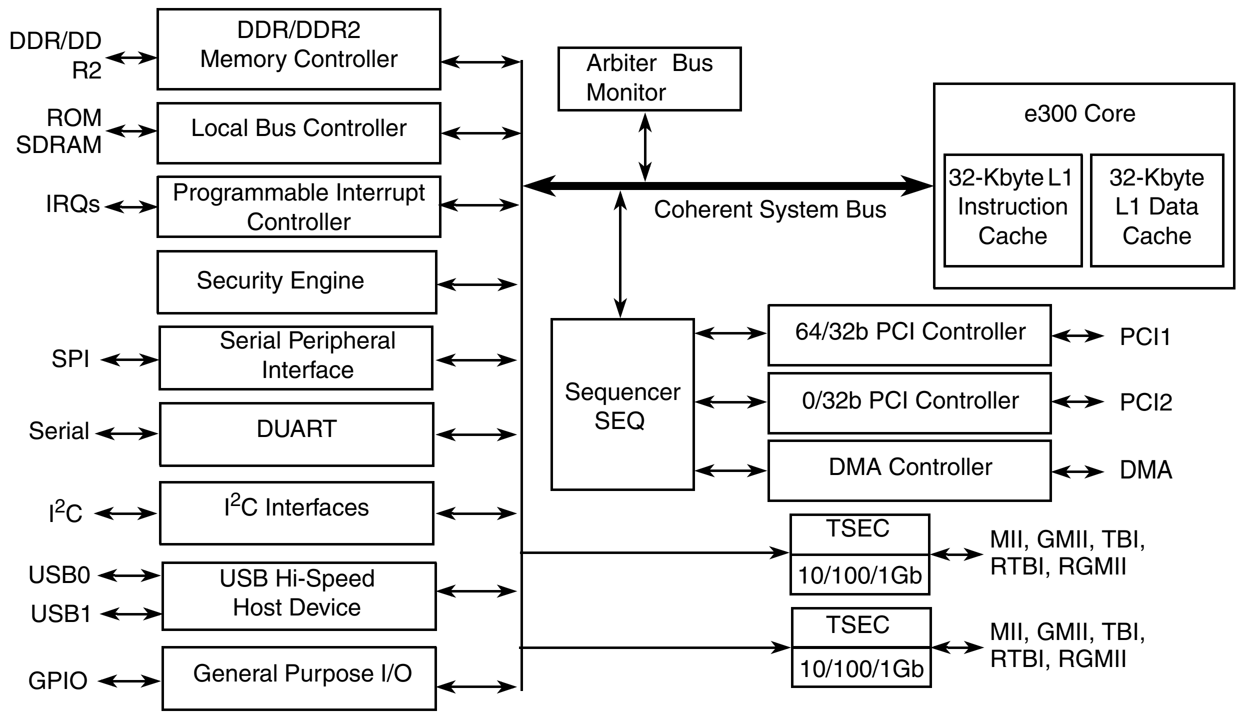

Figure 1. MPC8349EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - — High-performance, superscalar processor core
  - — Floating-point, integer, load/store, system register, and branch processing units
  - — 32-Kbyte instruction cache, 32-Kbyte data cache
  - — Lockable portion of L1 cache
  - — Dynamic power management
  - — Software-compatible with the other Freescale processor families that implement Power Architecture technology

- On-chip arbitration supporting five masters on PCI1, three masters on PCI2
- Accesses to all PCI address spaces
- Parity supported
- Selectable hardware-enforced coherency
- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI

- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
  - Public key execution unit (PKEU) :
    - RSA and Diffie-Hellman algorithms
    - Programmable field size up to 2048 bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511 bits
  - Data encryption standard (DES) execution unit (DEU)
    - DES and 3DES algorithms
    - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric-key cipher
    - Key lengths of 128, 192, and 256 bits
    - ECB, CBC, CCM, and counter (CTR) modes
  - XOR parity generation accelerator for RAID applications
  - ARC four execution unit (AFEU)
    - Stream cipher compatible with the RC4 algorithm
    - 40- to 128-bit programmable key
  - Message digest execution unit (MDEU)
    - SHA with 160-, 224-, or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Random number generator (RNG)
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Static and/or dynamic assignment of crypto-execution units through an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
  - USB on-the-go mode with both device and host functionality

- Complies with USB specification Rev. 2.0
- Can operate as a stand-alone USB device
  - One upstream facing port
  - Six programmable USB endpoints
- Can operate as a stand-alone USB host controller
  - USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
  - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)

• Universal serial bus (USB) multi-port host controller
- Can operate as a stand-alone USB host controller
  - USB root hub with one or two downstream-facing ports
  - Enhanced host controller interface (EHCI) compatible
  - Complies with *USB Specification Rev. 2.0*
- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Direct connection to a high-speed device without an external hub
- External PHY with serial and low-pin count (ULPI) interfaces

• Local bus controller (LBC)
- Multiplexed 32-bit address and data operating at up to 133 MHz
- Eight chip selects for eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
- Three protocol engines on a per chip select basis:
  - General-purpose chip select machine (GPCM)
  - Three user-programmable machines (UPMs)
  - Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)

• Programmable interrupt controller (PIC)
- Functional and programming compatibility with the MPC8260 interrupt controller
- Support for 8 external and 35 internal discrete interrupt sources
- Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
- Programmable highest priority request
- Four groups of interrupts with programmable priority
- External and internal interrupts directed to host processor
- Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
- Unique vector number for each interrupt source

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Parameter		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1 Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2 **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3 **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4 **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5 (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

6 OVIN on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.

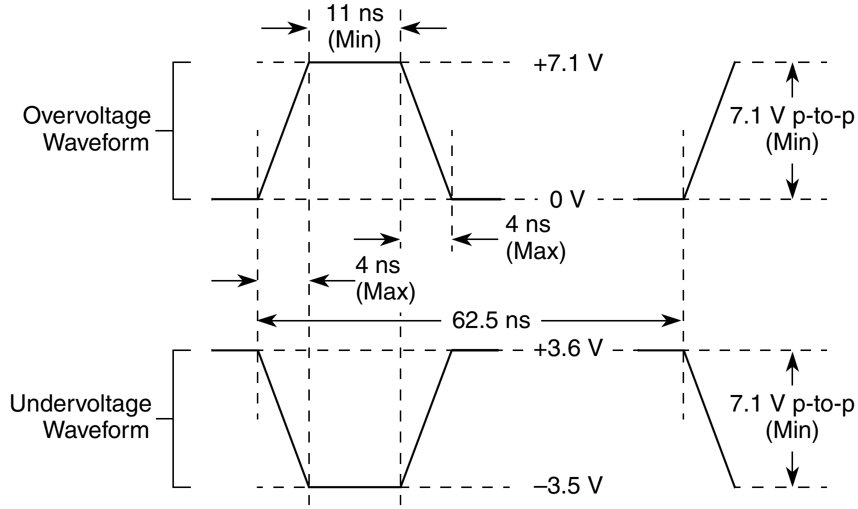

Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV_{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV_{DD} = 1.8 V
TSEC/10/100 signals	40	LV_{DD} = 2.5/3.3 V
DUART, system control, I^2C, JTAG, USB	40	OV_{DD} = 3.3 V
GPIO signals	40	OV_{DD} = 3.3 V, LV_{DD} = 2.5/3.3 V

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8349EA.

2.2.1 Power-Up Sequencing

MPC8349EA does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

Table 21. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, “Ethernet Management Interface Electrical Characteristics.”

8.2.3.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise (20%–80%)	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 shows the TBI transmit AC timing diagram.

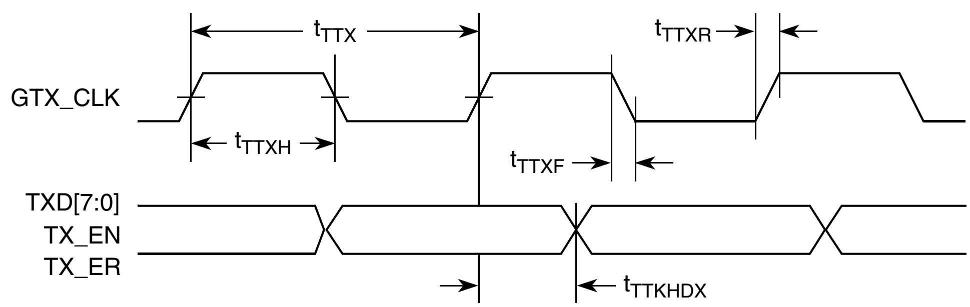

Figure 14. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%

Table 30. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t_{TRDVKH}[2]	2.5	—	—	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t_{TRDXKH}[2]	1.5	—	—	ns
RX_CLK clock rise time (20%–80%)	t_{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time (80%–20%)	t_{TRXF}	0.7	—	2.4	ns

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
2. Setup and hold time of even numbered RCG are measured from the riding edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the riding edge of PMA_RX_CLK0.

Figure 15 shows the TBI receive AC timing diagram.

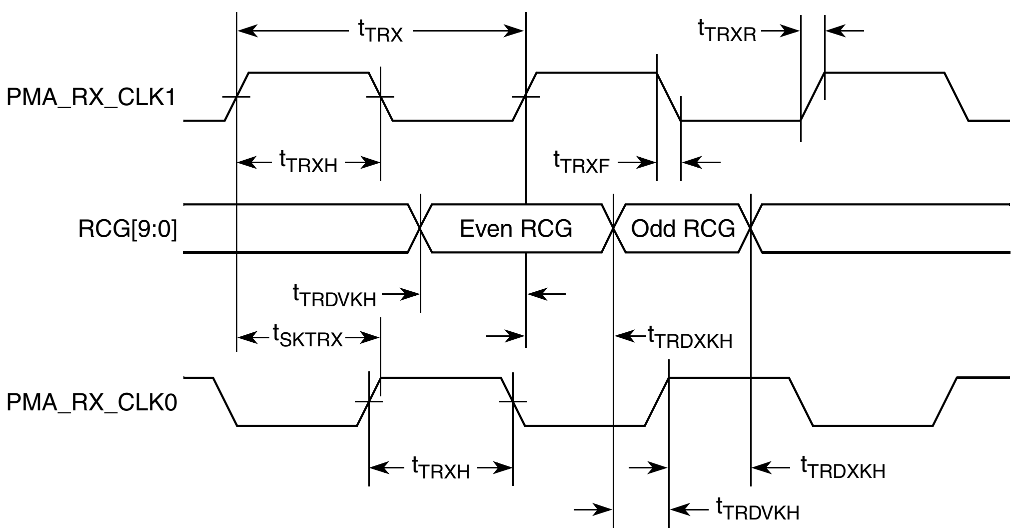

Figure 15. TBI Receive AC Timing Diagram

10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8349EA.

Table 38. Local Bus General Timing Parameters—DLL On

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 21 through Figure 26 show the local bus signals.

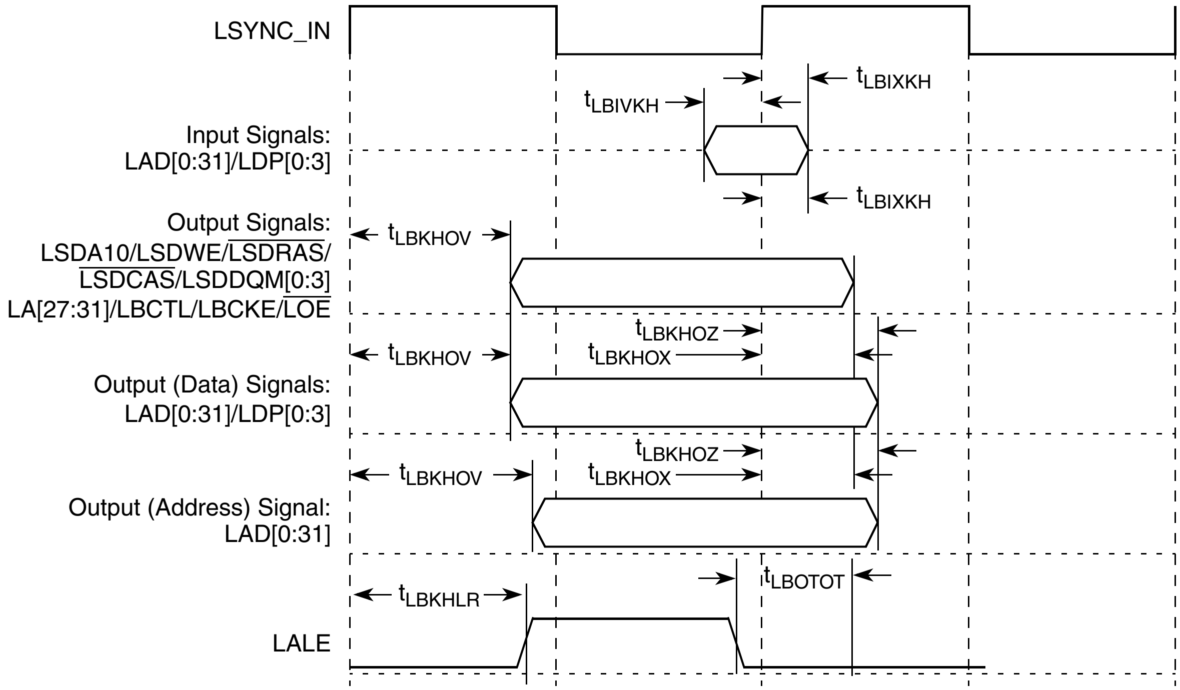

Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

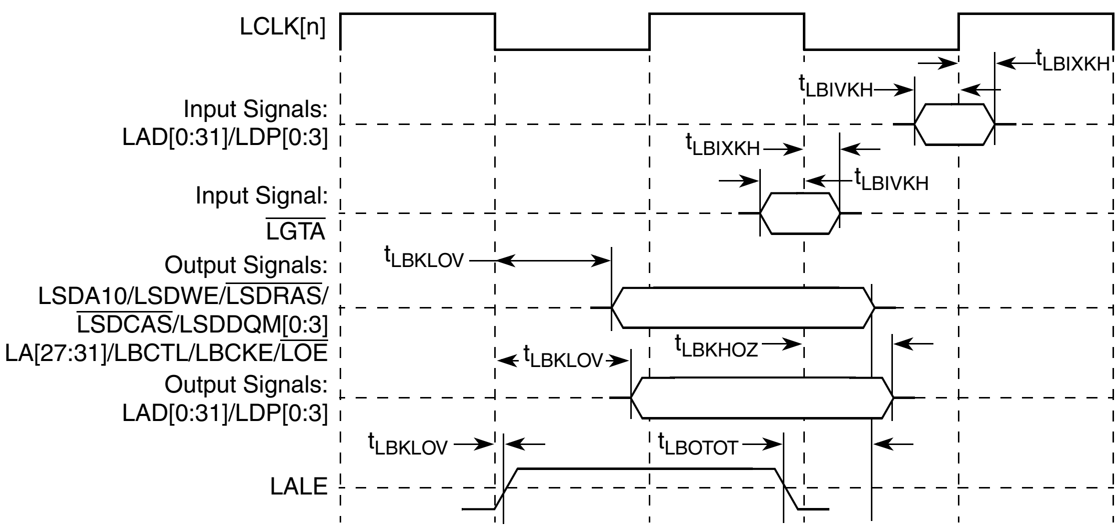

Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

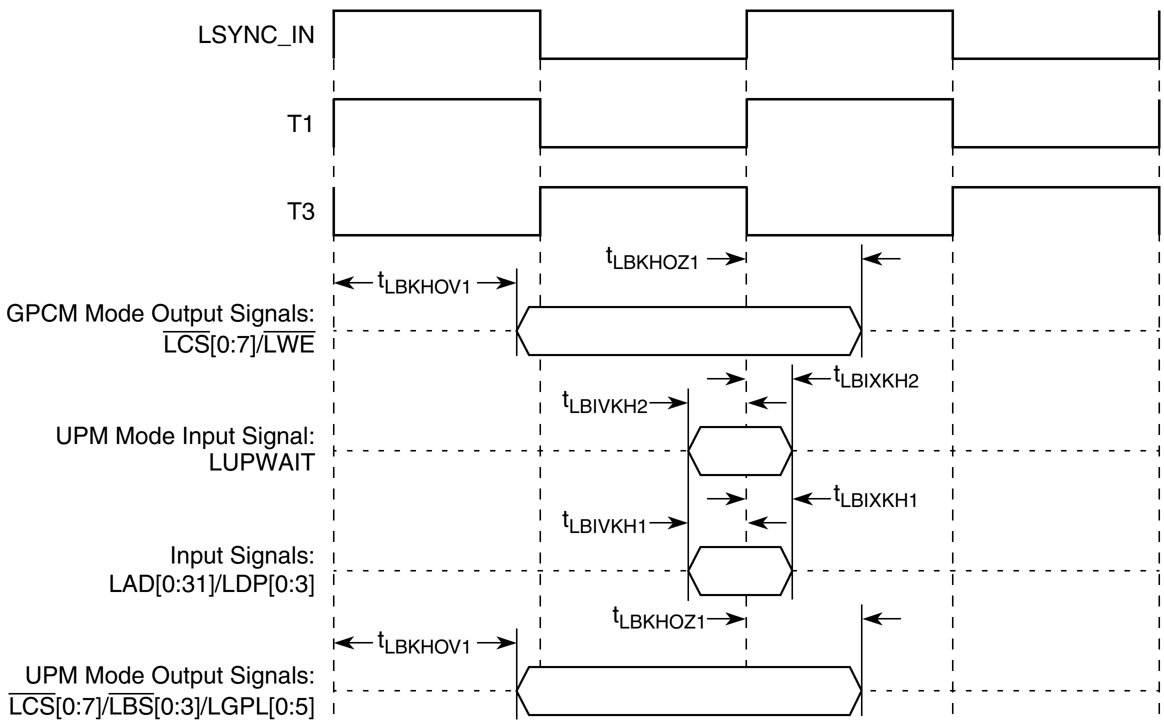

Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

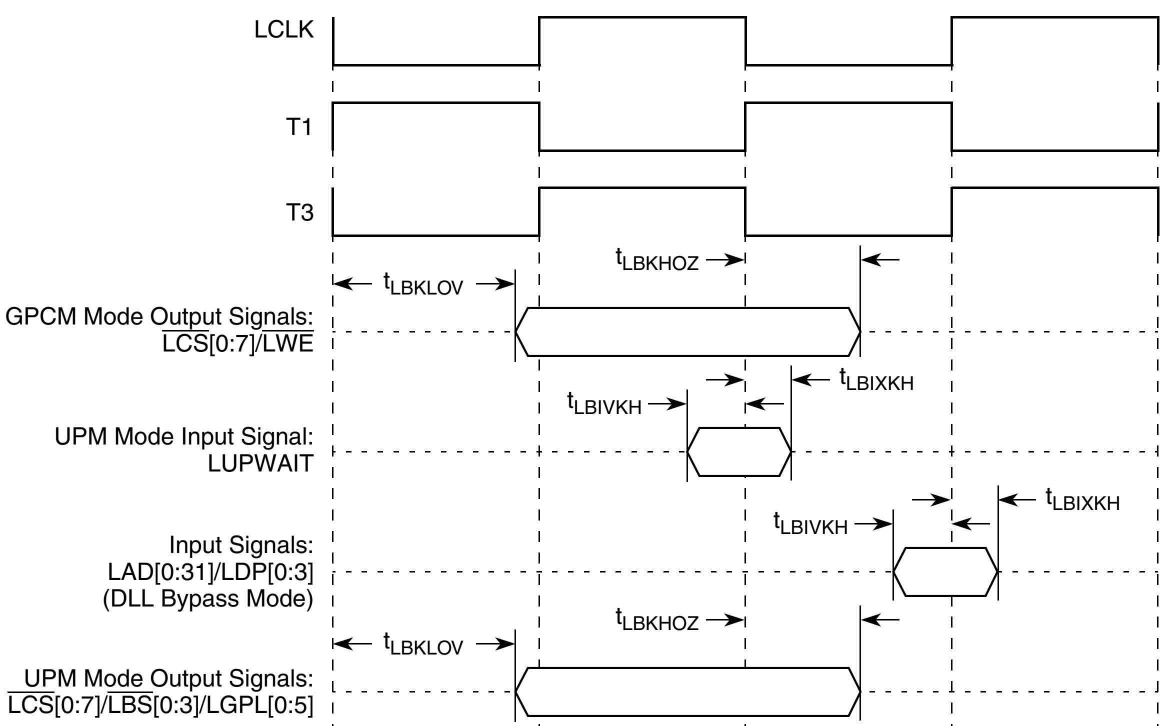

Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Table 45. PCI AC Timing Specifications at 66 MHz[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
$\overline{PORESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	6

Notes:
1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The setup and hold time is with respect to the rising edge of $\overline{PORESET}$.

Table 46 provides the PCI AC timing specifications at 33 MHz.

Table 46. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4
$\overline{REQ64}$ to $\overline{PORESET}$ setup time	t_{PCRVRH}	5	—	clocks	5
$\overline{PORESET}$ to $\overline{REQ64}$ hold time	t_{PCRHRX}	0	50	ns	5

Notes:
1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The setup and hold time is with respect to the rising edge of $\overline{PORESET}$.

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV_{DD}	—
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	O	OV_{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	O	OV_{DD}	—
MPH1_CLK/DR_CLK	B29	I	OV_{DD}	—
USB Port 0				
MPH0_D0_ENABLEN/ DR_D8_CHGVBUS	C29	I/O	OV_{DD}	—
MPH0_D1_SER_TXD/ DR_D9_DCHGVBUS	A30	I/O	OV_{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	E28	I/O	OV_{DD}	—
MPH0_D3_SPEED/DR_D11_DMMD	B30	I/O	OV_{DD}	—
MPH0_D4_DP/DR_D12_VBUS_VLD	C30	I/O	OV_{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	A31	I/O	OV_{DD}	—
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV_{DD}	—
MPH0_D7_DRVVBUS/ DR_D15_IDPULLUP	C31	I/O	OV_{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	B32	I	OV_{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	A32	I/O	OV_{DD}	—
MPH0_STP_SUSPEND/ DR_TX_READY	A33	I/O	OV_{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	C32	I	OV_{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	D31	I/O	OV_{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	E30	I/O	OV_{DD}	—
MPH0_CLK/DR_RX_VALID	B33	I	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	AN33	O	OV_{DD}	2
$\overline{\text{IRQ}}$0/$\overline{\text{MCP_IN}}$/GPIO2[12]	C19	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[6]/GPIO2[18]/$\overline{\text{CKSTOP\_OUT}}$	A21	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[7]/GPIO2[19]/$\overline{\text{CKSTOP\_IN}}$	C20	I/O	OV_{DD}	—
Ethernet Management Interface				
EC_MDC	A7	O	LV_{DD1}	—
EC_MDIO	E9	I/O	LV_{DD1}	11

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	B20	O	OV_{DD}	3
TMS	A20	I	OV_{DD}	4
$\overline{TRST}$	B19	I	OV_{DD}	4
Test				
TEST	D22	I	OV_{DD}	6
TEST_SEL	AL13	I	OV_{DD}	6
PMC				
$\overline{QUIESCE}$	A18	O	OV_{DD}	—
System Control				
$\overline{PORESET}$	C18	I	OV_{DD}	—
$\overline{HRESET}$	B18	I/O	OV_{DD}	1
$\overline{SRESET}$	D18	I/O	OV_{DD}	2
Thermal Management				
THERM0	K32	I	—	8
Power and Ground Signals				
$AV_{DD}1$	L31	Power for e300 PLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}1$	—
$AV_{DD}2$	AP12	Power for system PLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}2$	—
$AV_{DD}3$	AE1	Power for DDR DLL (1.2 V nominal, 1.3 V for 667 MHz)	—	—
$AV_{DD}4$	AJ13	Power for LBIU DLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}4$	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	—	—	—
GV_{DD}	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV_{DD}	—
LV_{DD1}	C9, D11	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV_{DD1}	—
LV_{DD2}	C6, D9	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV_{DD2}	—
V_{DD}	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V_{DD}	—
OV_{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	—
MVREF1	M3	I	DDR reference voltage	—

Table 62. Suggested PLL Configurations (continued)

Ref No.[1]	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
306	**0011**	**0000110**	—			—			66	200	600
405	**0100**	**0000101**	—			—			66	266	667
504	**0101**	**0000100**	—			—			66	333	667

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.
2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

20 Thermal

This section describes the thermal specifications of the MPC8349EA.

20.1 Thermal Characteristics

Table 63 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8349EA.

Table 63. Package Thermal Characteristics for TBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.7	°C/W	5

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, “Core PLL Configuration.”

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The AV_{DD} level should always equal to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four AV_{DD} pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV_{DD} pin being supplied. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.

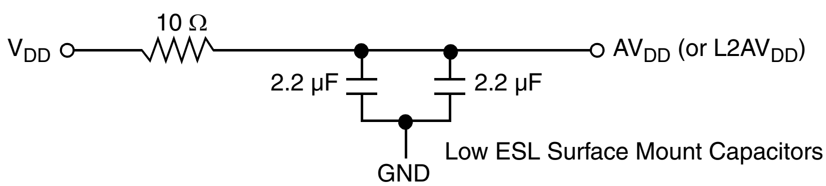

Figure 42. PLL Power Supply Filter Circuit

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8349EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8349EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

22.1 Part Numbers Fully Addressed by This Document

Table 66 shows an analysis of the Freescale part numbering nomenclature for the MPC8349EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 66. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature[1] Range**	**Package[2]**	**Processor Frequency[3]**	**Platform Frequency**	**Revision Level**
MPC	8349	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	ZU =TBGA VV = PB free TBGA	e300 core speed AG = 400 AJ = 533 AL = 667	D = 266 F = 333[4]	B = 3.1

Notes:
1. For temperature range = C, processor frequency is limited to with a platform frequency of 266 and up to 533 with a platform frequency of 333
2. See Section 18, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. ALF marked parts support DDR1 data rate up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 data rate up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 data rate up to 333 MHz (at a CSB of 333 MHz).

Table 67 shows the SVR settings by device and package type.

Table 67. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8349EA	TBGA	8050_0030
MPC8349A	TBGA	8051_0030

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